

FAT 249

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Hochspannungsverkopplung
in elektronischen Komponenten
und Steuergeräten

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High-voltage coupling in electronic devices and control units

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1 Revision History

Version	Changes	Date
V1	initial version	16.04.2012
V2	<ul style="list-style-type: none"> • Comparison of different ESD standard models (TLP, IEC, HBM etc) is added (Chapter 7.1) • TLP Testing Method on System-Level is added (Chapter 11.6) • Analysis of ISO-Rinne and identification of an equivalent TLP test method is added (Chapter 11.7) • General design rules are revised (Chapter 10.4) • Flow diagram for ESD robust PCB design is added (Chapter 10.4.7) • Flow diagram for ESD robust PCB and enclosure design is added (Annex C/ D) • Merit of published ESD guidelines and application of guidelines to the reported failure cases is added (Annex B) • Stronger link to the case studies and results is established. Design rules that could prevent observed failures are discussed (Annex B) • Conclusion/ Summary on analyzed field problems and investigations on ESD coupling is added (Chapter 12) • Lists of characterized protection elements are added (Annex A) 	19.09.2012

2 Introduction

High voltage pulses in vehicles can result from intentional switching, error sequences, when contacts are disconnected unintentionally, or Electrostatic Discharges (ESD). Higher voltage levels needed for electric drive systems will aggravate the problems. The pulse events can cause permanent or temporary malfunction of electronic components in vehicles. In this report ESD in vehicles will be discussed exemplarily as one important source for transient disturbances in vehicles.

The current shape and the transient fields are mainly influenced by the setup and material properties of all affected components. Ambiguous configurations are possible sources of different current and voltage shapes impressing various disturbance signals in victim devices. Because of lightweight construction requirements more and more synthetic materials will be used in the future increasing the probability of charging and discharging processes. Design improvements and corrective measure in case of ESD failure are more difficult to implement due to missing low impedance grounding in the vehicle. A classification of possible disturbance scenario and aligned testing methods can hardly be developed today.

In the past standardization of ESD testing methods was based on a prior definition of the disturbance sources. Especially for semiconductors many relevant ESD events were classified. Most important testing methods for semiconductors refer to the direct discharge of a human hand (via skin without metal tool) into an IC pin, the discharge of a charged IC into parts with low impedance, and the discharge of a charged tool or machine into a semiconductor. Moreover testing methods were defined considering the capability of ESD events to cause permanent failure. Transient fields or temporary malfunction are not considered.

During the 1980s ESD testing of electronic systems mainly was influenced by the computer industry where often only a single relevant source for ESD was defined. Humans who get in touch with electronic devices via metal pieces with good conducting properties (tools, keys, etc.) were defined as the most serious source for ESD. Besides hand-metal ESD the discharge of larger metallic objects was simulated by a "crossed-vane" simulator. This test method was mainly used by IBM for larger computer systems and was not accepted by the general ESD community. In the automotive community this method was never taken into account. Due to the undifferentiated definition of sources, only special ESD events are covered by typical system level testing methods.

For automotive ESD testing known system level methods were taken and partly adapted concerning pulse energy and pulse shape. The influence of the car body was included in automotive testing by a variation of the capacitance of the human body. The discharge resistor was increased to reproduce a discharge directly through the skin and not via a piece of metal. All adaptations seemed to be useful at the

beginning, but low impact on the testing results and increasing efforts finally led to more and more discussions how the number of special automotive ESD testing options can be reduced.

With reference to case studies where electronic devices were disturbed by the discharge of humans the scenario of a human discharge seems to be included well in today's testing methods. Only few problems are still known. All other ESD problems in practice can be hardly related to a discharge of a human body. Because of the large variation range of ESD events a definition of a unified testing strategy is difficult. Different attempts for improved testing methods in order to reproduce also non-human ESD events can be found. A simple approach is to increase the charging voltage of available ESD generators until malfunction of the tested device is detected. In this case the pulse shape and source impedance would not be adapted and the error pattern could be quite different in practice. Moreover an un-deliberate increase of charging voltage often leads to general over-testing followed by rising costs.

ESD failure can be caused also by transient fields coupling into conducting parts of systems. Different testing methods are known to address field problems but standardization nearly is impossible because variation range of field appearance is much larger than for conducted currents.

A highly targeted approach to testing electronic devices using only a single method which covers all ESD effects is not available. The compliance of formulated targets is made difficult by particular characteristics of electro mobility and an increasing use of non-conducting materials.

Assuming an intrinsic knowledge of the disruptive strength of semiconductor materials, basic testing methods could be defined on IC level. In a next step these methods could be extended by theoretic considerations and adapted to special system topologies to formulate applicable testing strategies in different situations. Here a classification of destructing and disturbing ESD events is required.

In practice only few cases of field returns can be referred to ESD where malfunction of electronic systems is observed. Although case studies are time consuming and expensive, failure mechanisms should be analyzed well to classify ESD critical configurations. Coupling mechanisms in electronic systems become more and more important with decreasing dimensions of devices. Better understanding of failure and coupling mechanisms can help to develop a step-wise and problem-oriented ESD testing and ESD protection concept.

3 Project Objectives

Beside the description of the state of the art and quantification of disturbances by high voltage pulses, methods for the step-wise ESD analysis and testing of electronic automotive devices are investigated.

First typical ESD threads reported by the FAT AK 23 are analyzed and documented. Characteristic parameters like coupling capacitance and inductance are defined to calculate coupling current, voltage and energy. Then the relation between coupling parameters and geometrical and electrical conditions is known and can be used to formulate critical cases.

Common IC destruction mechanisms are described and modeling methods are summarized. Here the main focal point is on modeling failures due to thermal destruction. IC soft errors and modeling of IC disturbances is considered in special cases.

Failure behavior of ICs can be investigated well by TLP analysis. Selected automotive ICs are characterized partially using a TLP testing system. A behavioral model for the IC pins is generated from the measurement data to simulate the thermal failure behavior. Models of standardized pulse sources and multi-conductor transmission lines are presented, discussed, and adapted to IC failure analysis. Possible coupling paths with parallel traces on PCBs or wires in a cable harness are modeled. The assembly area of ICs can be analyzed systematically by simulation of different critical topologies. ESD failure models of ICs allow developing individual ESD protection concepts considering different PCB configurations. The possible disturbance level by standardized ESD events is analyzed incorporating different ESD protection elements. Besides permanent destruction soft failures can occur due to ESD. The root cause of such failures is often difficult to determine. Soft failures are still an area of active research. This report provides an overview of the types of soft errors and gives insight into methods for finding the root cause within a system using susceptibility scanning.

Further, the impact of additional wiring, housing or assembly parameters on the ESD sensitivity is analyzed. Investigation of critical configurations helps to formulate individual and customized testing strategies. The requirement for alternative ESD testing methods like TLP or ESD scanning systems is analyzed considering possible special applications. Improved system level ESD testing methods are proposed. The report combines specific analysis of products with more general analysis of model structures and proposes methods for more powerful failure analysis and testing.

4 State of the Scientific and Technical Knowledge

Electrostatic discharge (ESD) can cause permanent physical damage or malfunction of electrical components. Electronic devices usually are equipped with special ESD protection circuits which are designed to withstand certain standardized ESD events. The ESD robustness of single ICs and electronic systems is performed using standardized pulse shapes generated by ESD pulse generators which represent discharges of humans, devices, or machines.

In the following sections reported case studies found in literature are divided into topics regarding ESD testing and ESD failure mechanisms. The following databases were used:

- Proceedings EOS/ESD Symposium (USA)
- Proceedings ESD Forum (Germany)
- Proceedings EMV Düsseldorf (Germany)
- Proceedings EMC Europe (Europe)
- IEEE Xplore (journals and conferences)
- INSPEC (journals and conferences)
- Scopus (journals and conferences)
- Scitopia.org (journals and conferences)
- TEMA „Technik und Management“ (journals and conferences)
- Web of Knowledge (journals and conferences)

4.1 ESD Testing

ESD testing is usually subdivided into IC testing and system testing. With the exception of the latch up test all IC testing is performed without powering up the IC and only testing for damage. In contrast to this, system level testing is performed having the system operational and testing for both soft failures and damage. However, the traditional separation between IC and system level is breaking up, as many ICs and modules are tested to system level standards, as more and more IC and module soft error characterization is performed, and, mainly, as one has learned that an optimal system design needs to be a compromise between IC level, module level, and system level ESD protection. The Industry Council on ESD Target Levels (www.esdindustrycouncil.org) has published two whitepapers on this general issue and is in the process of publishing a third white paper that addresses system level testing more.

On IC level, the sensitivity of semiconductors to the discharge from the fingertip of a typical human being is specified in the Human Body Model (HBM) standard [53]. ESD

events due to manufacturing machines are described in Machine Model (MM) standard [2]. The Charged Device Model (CDM) standard [3] assumes the discharge of a charged IC. All standards are used to test the IC robustness during the manufacturing process simulating carrying, holding or mounting of components. ESD testing of automotive electronic systems is standardized according to IEC 61000-4-2 and ISO 10605 simulating the discharge of human operators [4], [5]. On IC level the discharge from a human directly through the skin (Human Body Model (HBM, skin discharge)) and the discharge via a small piece of metal (Human Metal Model (HMM)) are differentiated. Further IC ESD testing is performed to test its robustness to latch-up.

4.1.1 System Level Testing Approaches

Most of today's ESD failures occurring during automotive manufacturing process or during application by the end-user cannot be associated with a human discharge. The attempt to handle the problem by increasing specified ESD testing levels can lead to overdesign and higher costs for protection circuits if characteristics of ESD events are completely neglected. E.g., electronic systems can be affected by Cable Discharge Events (CDE), which can occur during the automotive production process, when numerous cables are connected to electronic devices. Typical CDE in the automotive production environment were investigated and characterized in [6]. The initial point of CDE is a potential difference between the cable harness and the electronic component which is connected. In the moment of arc generation a fast transient discharge current pulse occurs, which can cause serious ESD damages. The measured rise time of the CDE is approximately 200 ps, this is about 5 times faster than the IEC discharge. Thus the cross-talk between PCB-traces is increased and a CDE can couple into local pins. Due to the fast rise time, standard filter structures might not be sufficient as ESD protection circuits. The inductance of circuit elements can cause reduced performance of protection elements. Charging voltages up to 2 kV of cables were measured in an automotive production line. In combination with the cable harness length up to several meters in a vehicle energies of CDE events are comparable to an 8 kV IEC discharge [6]. New strategies for ESD testing regarding CDE are currently discussed [7]. Several approaches using a charged transmission line were proposed. Different source impedances can be realized by the setups shown in Figure 4.2 and Figure 4.2.

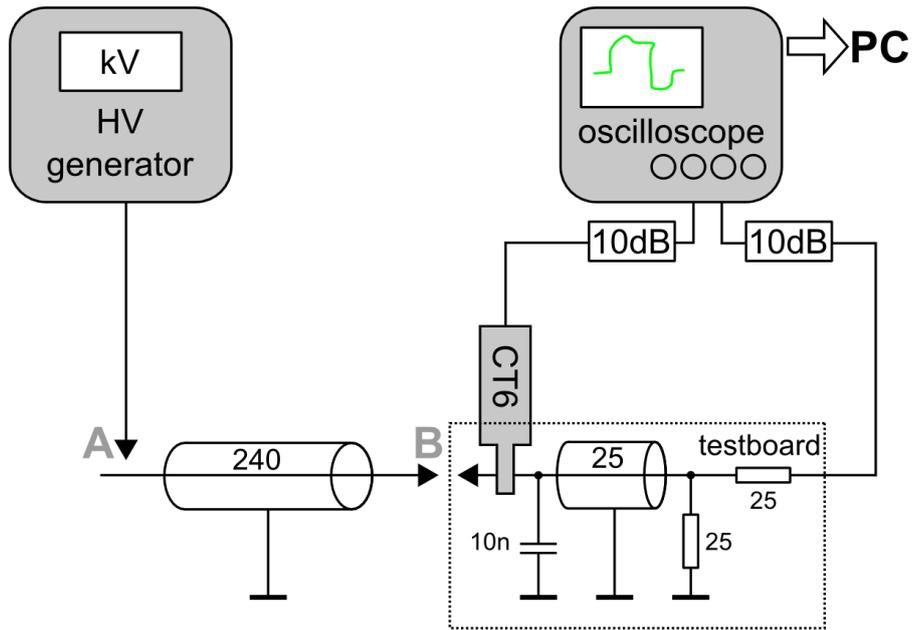
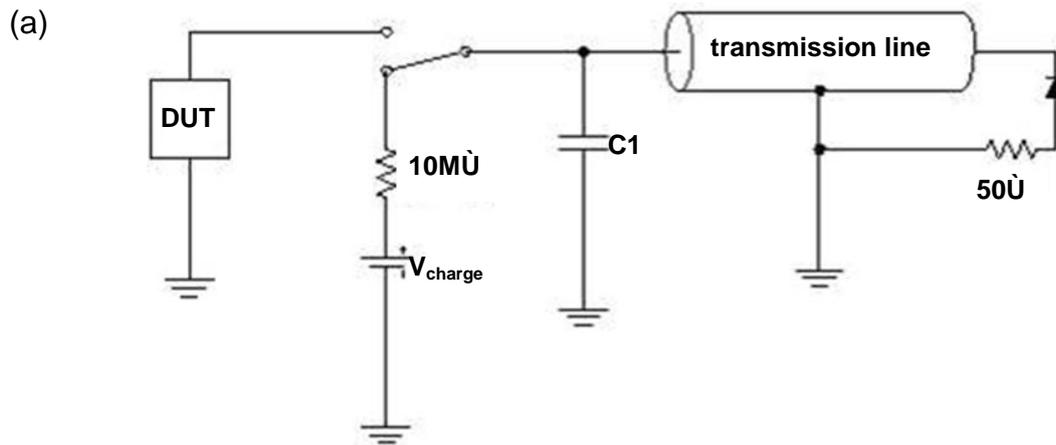


Figure 4.1: Cable discharge measurement setup [6]



(b)

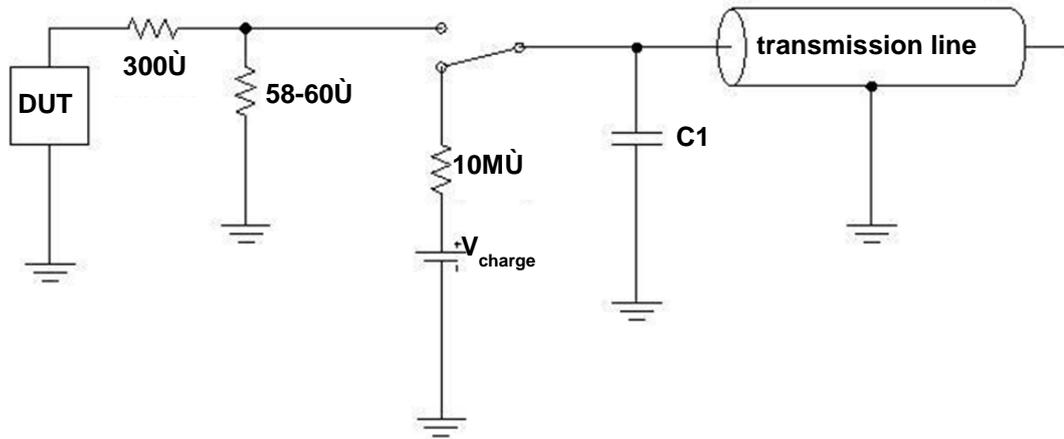


Figure 4.2: Examples of low impedance (a) and high impedance (b) transmission line generators [7]

ICs that are robust to ESD at the component-level may be damaged by ESD at the board-level. In [8] ESD of charged PCBs so called charged board event (CBE) was investigated. It was shown that CBE can be more severe than HBM or CDM specified by the ESD Association. Since the PCB capacitance is much higher than IC package capacitance CBE pulse energies are higher and rise times are faster compared to CDM events. In Figure 4.3 an approach for a CBE setup is shown. The evaluation board capacitance of about 1.6 nF was measured between ground plane and a charging plate. During the test the IC pins are connected to PCB testing pads. The charging plate is raised to charging voltage level. Then a selected PCB test pad is connected to ground and a discharge current is conducted through the IC pin.

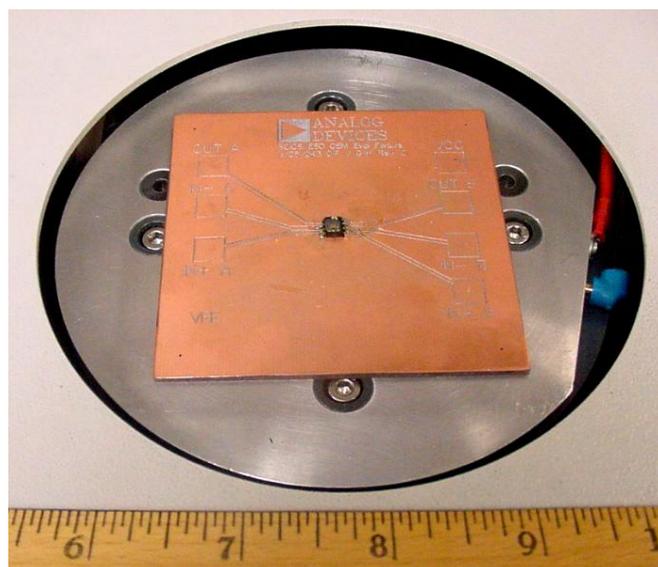


Figure 4.3: CBE test board on charging plate [8]

To illustrate the simulation of a CBE event we only look at the discharge of the ground plane of the PCB to the ground reference plane. This would be the case if a charged board is connected to a cable having a connector that ensures ground contact first. In this case the only non-linear element of the discharge would be the arc itself. The linear part can be modeled by looking at the impedance between the PCB ground and the ground reference. This impedance can be obtained from full wave simulations or measurements and then be approximated by an equivalent circuit or other linear circuit's descriptions. Next an arc model needs to be added to obtain the current. The methodology and simulation examples are given in [61].

If the discharge is not to the ground of the PCB, but to nets on the PCB a net description and a description of the ESD protection network needs to be included into the model. As outlined in this report, the net description can be extracted from the geometry and the component description from VI-curve tracing. While in SEED [22] analysis usually TLP models are used for ESD testing one has to change the source for CBE analysis: The source needs to describe the impulse created by the overall board geometry relative to a ground reference plane. Again, this is obtained by simulating or measuring the impedance between the ground plane of the PCB and the ground reference plane and then adding the SEED description of the net such that it is reference to the ground of the PCB. Further information on CBE can be found in the following references [62] - [75].

4.1.2 IC Failure Mechanisms and IC Level Testing Approaches

IC- or system-level ESD robustness against damage can be classified in terms of charging voltage levels of the pulse generators specified according to ESD testing standards mentioned above. The diversity of ESD events can cause different IC failure mechanisms. Three main destruction mechanisms are most important:

- Thermal breakdown is the prime damage mechanism in bipolar technology. The ESD current can cause a local overheating in the depletion region. This leads to a shortening of p-n junction and to melted silicon filaments.
- Gate-oxide-punch-through is the prime damage mechanism in MOS technology. Through a high voltage pulse the potential difference over the dielectric region can exceed the breakdown voltage.
- Metallization melting happens due to increased device temperature caused by an ESD pulse. Metal wires or bond wires can melt.
- Transient latch up: A NPNP structure latches up and causes a short circuit between Vdd and Vss leading to over current damage.

A correlation between the number of shipped ICs with a certain HBM and CDM stress level and the field return rate is described in white papers of an industry council of IC manufacturers [9], [10]. A total quantity of 21 billion parts with known HBM level and nearly 12 billion devices with known CDM qualification level is included in the

statistics. In Figure 3.4 the statistic of failure-rate versus CDM robustness are dominated by 15 designs out of 949 specified with 500 V CDM with very high dpm rate. If these devices are excluded a constant distribution over the CDM robustness level would be obtained. The authors assume that the correlation between the HBM/CDM robustness level and dpm rate is low. Both automotive and consumer devices were included in the statistics.

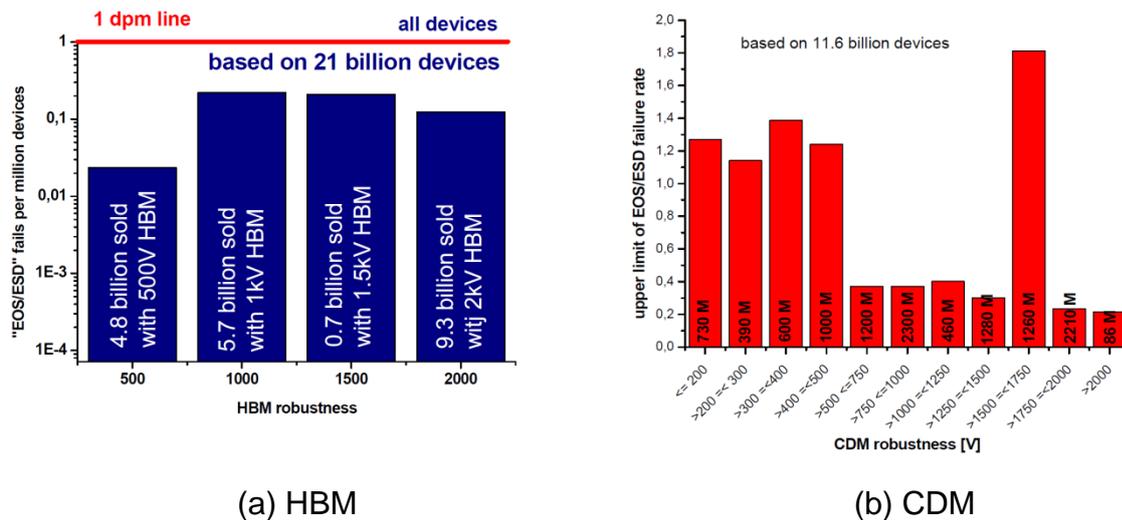


Figure 4.4: EOS/ESD fails returned to IC supplier versus the achieved (a) HBM, (b) CDM qualification level [1]

Most of the reported failures are based on permanent IC malfunction. Numerous ESD failures of single ICs were reported by IC manufacturers and can be found in literature [11] - [16]. On the other hand ESD soft-errors, where the system functionality is temporarily affected, are likely to appear more frequently. Neither IC nor system level ESD testing results give appropriate information about sensitivity to soft-failures of a device. Due to the huge diversity a general test specification or modeling approach to describe soft errors does not exist.

One of the widely discussed failure mechanism is the latch-up effect which also can cause temporary and permanent malfunction of a device. Some preventive strategies and design rules on IC level can be found in literature [17]. A standardized latch-up test for ICs is specified in EIA/JEDEC JESD 78 [18]. Because of different rise times from 5 μ s up to 5 ms and long pulse duration of up to 1 s the specified test can be understood as "static". A testing setup, considering the IC latch-up behavior with transients characterized by short pulse duration and rise times in the range from hundreds of ps to several ns (transient latch-up TLU), is not specified. Approaches for dynamic latch-up testing setups were presented in [19] and [20]. Presently an effort to develop such a standard is started at MST. A bipolar damped sinusoidal trigger voltage of CMOS ICs in system level ESD tests can cause TLU failures. In the testing setup shown in Figure 4.5 an IEC ESD generator is discharged via the horizontal

coupling plane causing TLU trigger signals at IC pins. The method was proposed in [21].

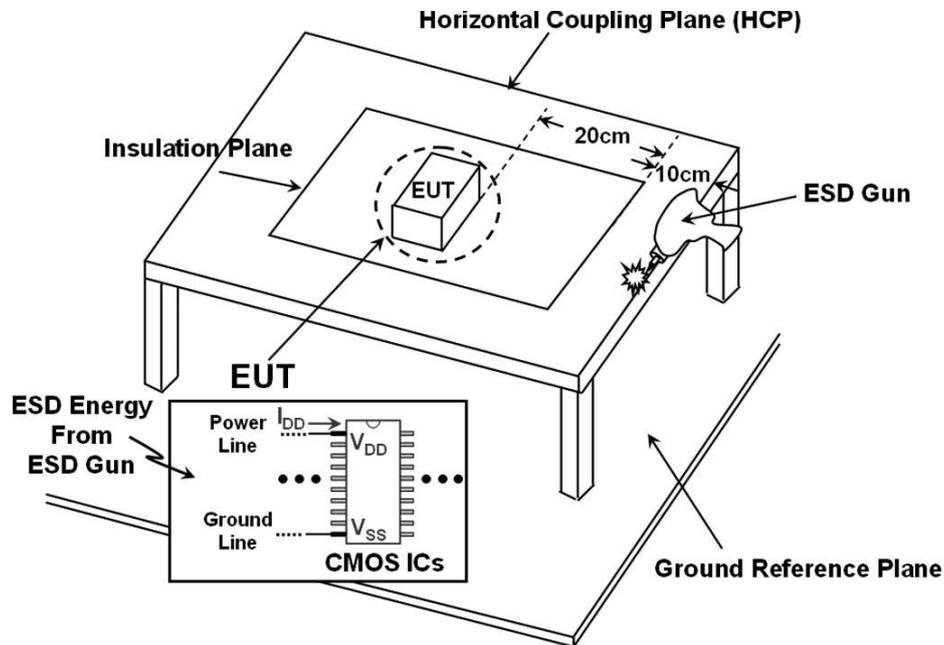


Figure 4.5: TLU system level testing setup with indirect contact discharge test mode [21]

4.2 New Test Concepts Discussed in Literature

4.2.1 Arbitrary Waveform Generator with Power Amplification

A wide variety of noise pulses can disturb an electronic system. This has led to a set of different standardized noise wave forms, e.g., ESD, modulated sine wave signals, etc. Further, the coupling within a system will disturb the waveform of the external field. For example, the coupling can be of resonant nature. Consequently, a wide variety of noise waveforms can reach ICs and lead to disturbances.

It is inefficient to use a multitude of noise generators to cover this wide variety of noise signals. A logical step is using an arbitrary waveform generator for the pulse creation. This approach has to overcome the difficulty of achieving sufficient voltage and currents, but it opens up the possibility for a variety of improvements in test method, such as:

- Pre-compensation of the effects of coupling methods (e.g. when using a capacitor to couple energy into a circuit, high frequency components are coupled better than low frequency components)
- Precise pulse shaping (e.g., creating only positive pulses to avoid forward biasing the negative ESD protection diodes)
- Injecting pulses synchronous to internal timing (Many ICs are susceptible only during very narrow times during their operation)

- Directional injection (see next chapter)

IC soft error data obtained by this method will enhance the understanding of the mechanisms that cause these errors and will allow simulation of soft-error mitigation techniques.

Using arbitrary waveforms [97] as a signal source has application to far field radiated, near field coupled and conducted immunity testing. Due to limits of power amplifiers, however, the signal from an arbitrary waveform generator is not strong and the method is most suitable for local injection techniques, like near field susceptibility scanning, GTEM cell testing and direct injection.

The system concept shown in Figure 4.6 illustrates an implementation for IC susceptibility evaluation. A dual channel arbitrary waveform generator creates two pulses which are injected into the same net, but at different locations. As demonstrated via simulation in the later sections, this allows directional injection that can target either the transmitter or the receiver side.

Four measurement ports provide the information needed for the automatic adoption of the pulse shape and timing. The injected current is measured using current clamps and the voltages at the ICs are measured using standard probing techniques. All four measurement channels connect to an oscilloscope. This data is used to adopt the pulse shape and timing to optimize the waveform of the injected noise and for directional injection. While injecting the noise, the functionality of the ICs is monitored using appropriate software (e.g. read/ write data and error checking, use of USB protocol analyzer while injecting into a USB link, etc.).

Without an arbitrary wave form generator it is not possible to obtain the desired noise waveform at the input of an IC due to its response and the distortion by coupling networks. Further, it is not possible to distinguish between transmitting or receiving IC responses, only the directional injection using a dual channel arbitrary waveform generator arrangement can achieve this.

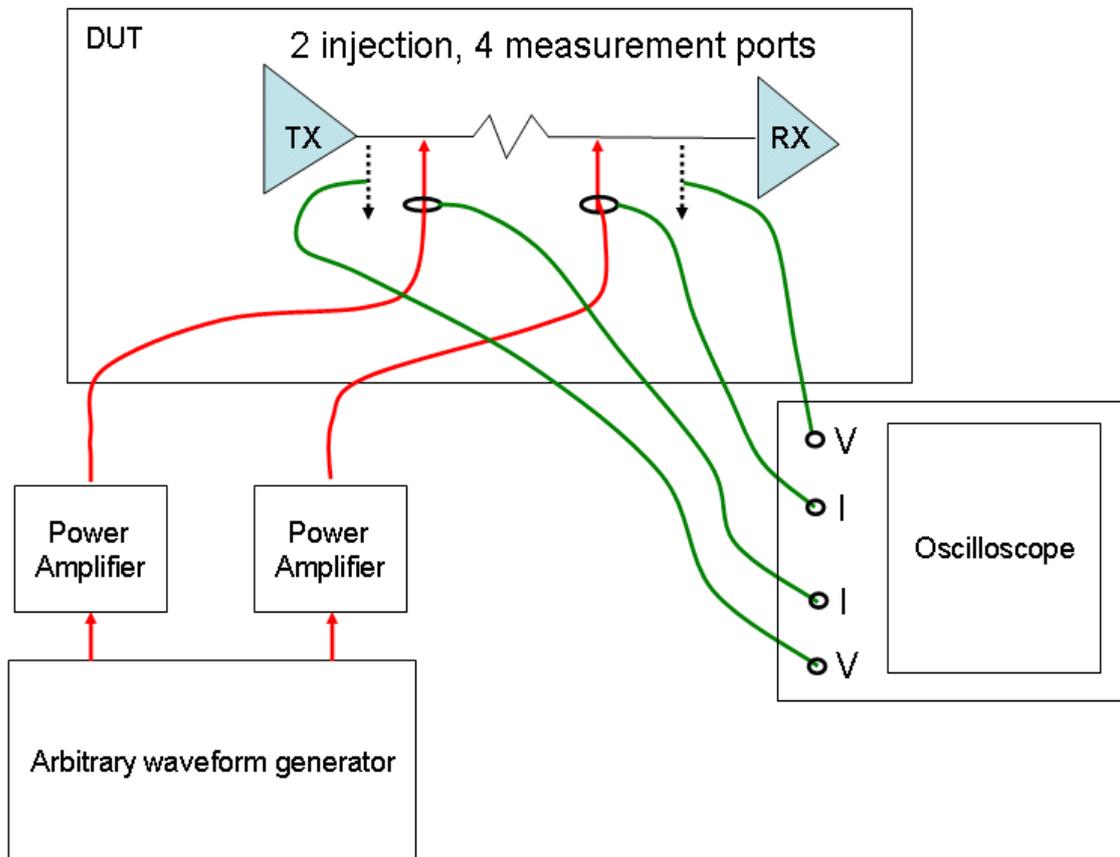


Figure 4.6: Directional injection targeting the transmitting (TX) or receiving (RX) IC using an arbitrary waveform based immunity evaluation. For other injection points, like Vdd or Vss, the basic principle would be maintained but the injection method and injection points would be varied.

4.2.1.1 Proof of Concept

Most electrical nets begin and terminate in an IC. For characterizing the noise susceptibility of just one IC, e.g. the receiving IC, one cannot just inject signals onto the net, as these signals will reach both the transmitting and the receiving IC. As suggested earlier, using a two channel arbitrary waveform generator allows directional injection, as will be illustrated at first for a simple case where a series resistor is placed in the connecting trace, and secondly for a direct connection. Both examples are based on simulations.

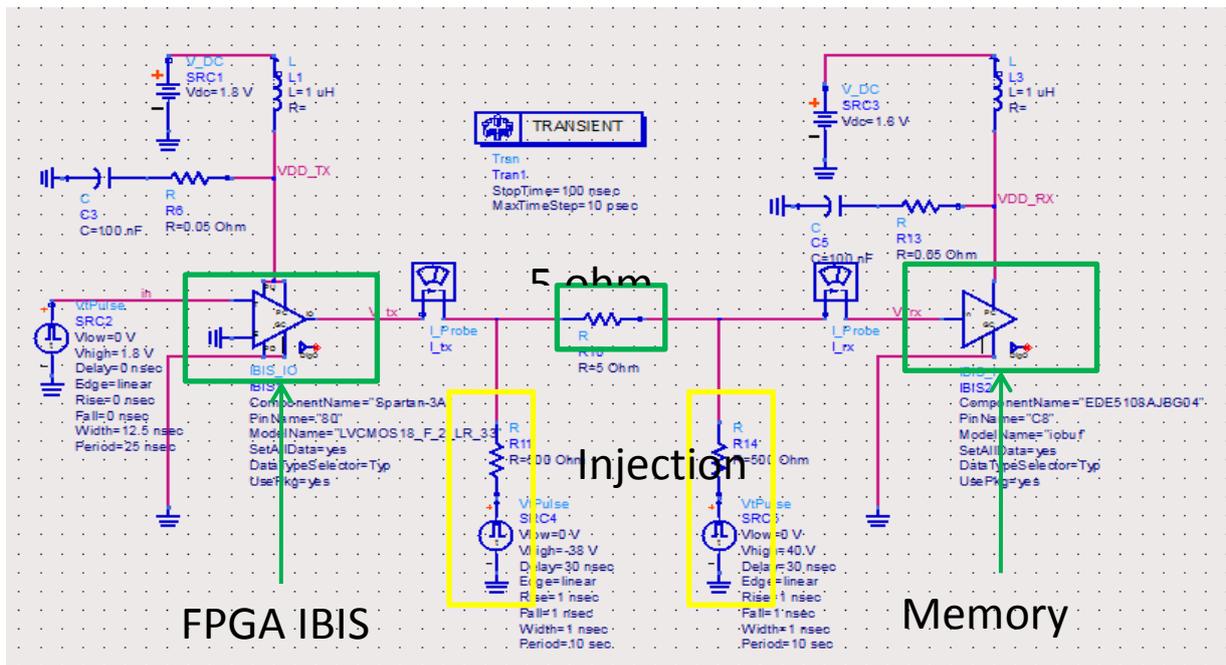


Figure 4.7: Simulation model for a two ICs connected via a 5-Ohm series resistor

The circuit in Figure 4.7 simulates the injection of signals into a connection between a transmitting and a receiving IC. The ICs are connected via a 5-Ohm series resistor. To achieve realistic results, both ICs are modeled using their IBIS models. Using an IBIS model allows the voltages and currents to be accurately modeled at their inputs and outputs.

Two channels of an arbitrary waveform signals are injected via 500 Ohm resistors (represented in the yellow boxes). The injection waveforms are adjusted for receive side injection, thus, the noise levels at the transmitters are minimized. The voltages are shown in Figure 4.8. A narrow pulse is injected such that it mainly reaches the receive side. The associated currents are shown in Figure 4.9. Figure 4.8 and Figure 4.9 show that a directional injection is possible for the simple case where a series resistor is present between the transmitter and receiver. Such resistors are often used as a series termination for achieving good signal integrity in high speed interfaces.

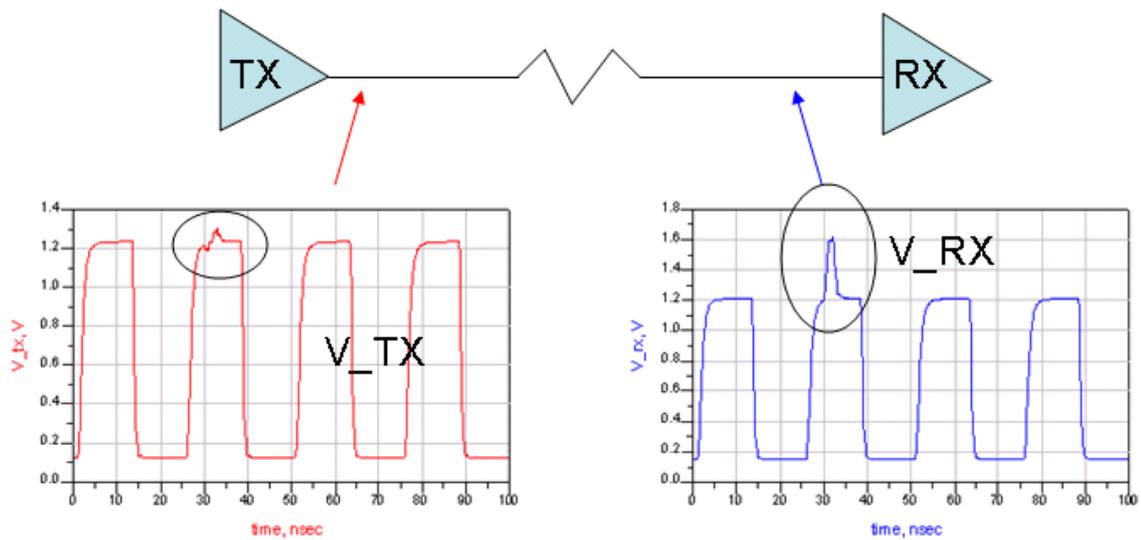


Figure 4.8: Voltage at transmit and the receive side during an injection.

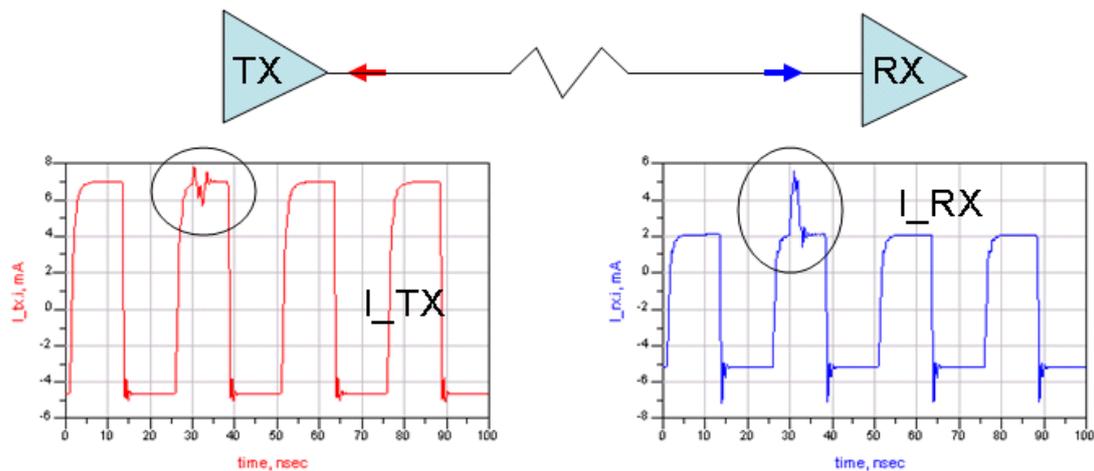


Figure 4.9: Currents flowing into the transmitter and into the receiver (the difference in the data signal current is caused by the injection probes)

Series resistors, however, are not used in other circuit topologies. Instead, many topologies connect receiving and transmitting ICs directly. The next simulation results are presented to show that the dual arbitrary waveform method is able to perform directional injection even if no series resistor is present.

The simulated circuit is shown in Figure 4.10. The transmitting and receiving ICs are connected via a trace having an electrical delay of 1 ns (green box). As in the previous simulation, IBIS models are used and a dual injection is performed. The waveforms injected at the receiver and at the transmitter are adjusted to achieve directional injection. In contrast to the previous example, we are directing the energy into the transmitting IC, and minimize the injection into the receiving IC.

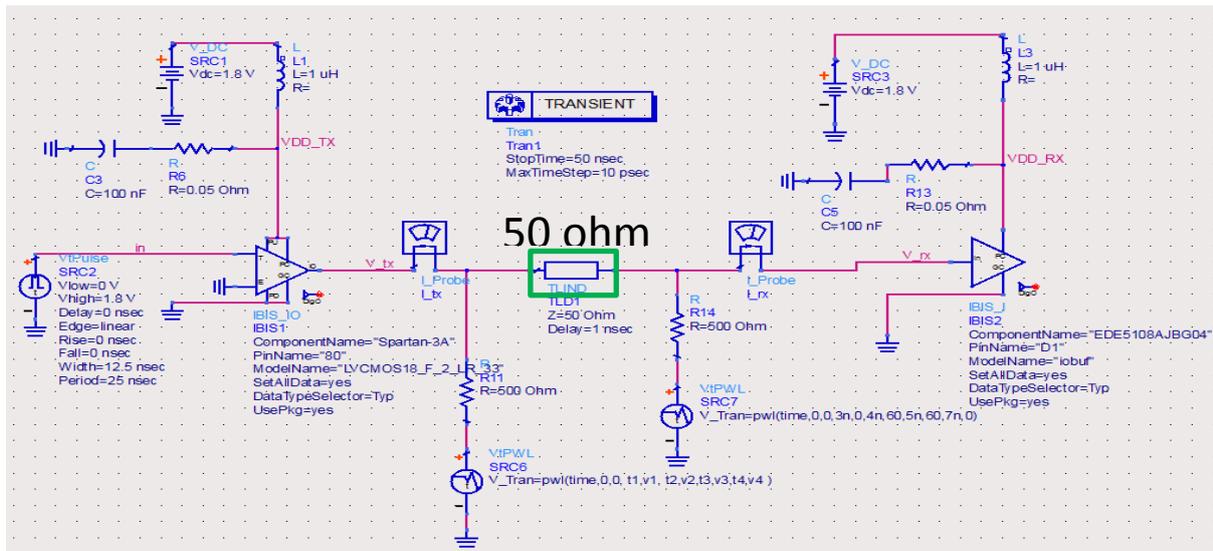


Figure 4.10: Simulation model for direct connection between receiver and transmitter.

Figure 4.11 shows the resulting voltages and currents. As shown in this figure, both voltage and current can be injected directionally in spite of having highly non linear input and outputs and a direct trace connecting the transmitter and receiver. Establishing directional injection allows one to characterize the soft-error behavior of an individual IC in a system.

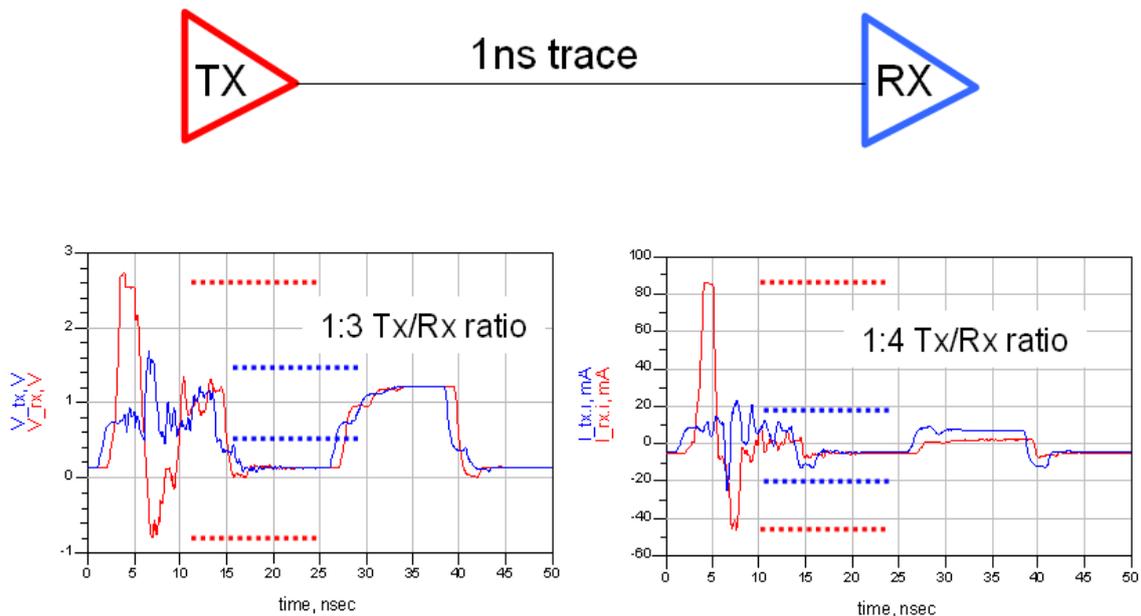


Figure 4.11: Simulation results demonstrating directional injection for two ICs directly connected with a trace.

An arbitrary wave form generator combined with a power amplifier can cover a wide variety of noise sources waveforms for immunity testing. Further, it allows directional injection and the synchronization to system events.

Its main limitations are the available voltage and current. If a 100W amplifier (1-1000MHz) is used the maximal voltage into 50 Ohm is about 100V peak. The maximal current is about 2A. Using 1:4 transformations the current or the voltage can be doubled. The rise time will be about 400 ps. This is certainly sufficient for soft-error investigations on IC and module level providing that the signals are directly injected into PINs. Further, it is sufficient for a large range of VI curve characterization. But it cannot substitute a TLP for high current VI curve characterization or a TLP which is often used for field coupled susceptibility scanning.

4.2.2 Susceptibility Scanning

Once a system fails due to a system level ESD event, isolating the root cause can follow different paths. For soft errors the most promising tool is local injection using susceptibility scanning. This can be performed by hand as previously mentioned but it is very difficult to obtain significant precision or generate a visual picture of the boards' sensitive locations. When done automatically these difficulties are removed.

The objective of susceptibility scanning is to identify locations, ICs, modules and electrical nets that exhibit the same failure symptoms that were observed during system level testing. If those locations are found within the system, it is likely that during system level testing energy is being coupled from the outside to those locations, thereby causing the failure.

To identify these sensitive locations a locally strong field needs to be created that resembles the noise that might be coupled from the outside ESD generator to suspect board or circuit. The methods are detailed in [95]. In brief, a transmission line pulser having rise times of <1 ns is connected to magnetic and/or electric field probes. These field probes are moved close to the ICs, nets or modules in question and pulses are applied via the field. The system reaction is observed. By varying the probe type, size and applied voltage, locally sensitive regions can be identified. Further, the results can be visualized as susceptibility sensitivity maps as shown below in Figure 4.12 and Figure 4.13.

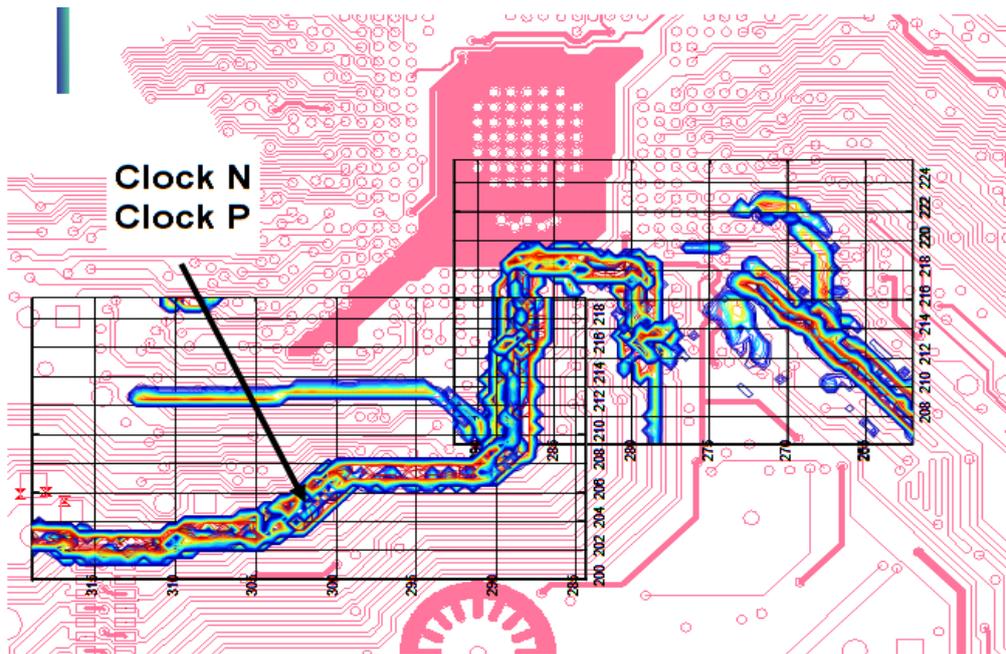


Figure 4.12: Result of susceptibility scanning: Sensitive differential clock on a PC motherboard

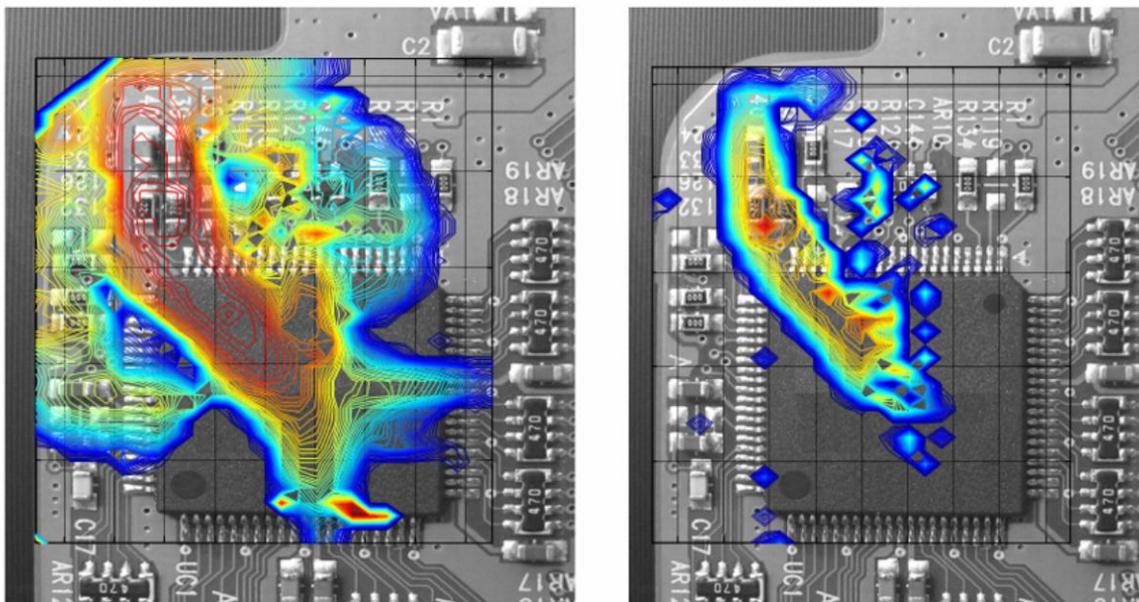


Figure 4.13: Result of susceptibility scanning: Comparison of two functional identical ICs from different vendors. The color grade indicates the TLP charge voltage with blue being 4 kV, red being 1 kV.

Beside field coupling, one can inject current directly into the traces. In this case the injected current can be measured, for example using a small current transducer such as a CT-2. For directly injecting current into a trace the scanning system is equipped with a probe that either contains a small capacitor, such as 1pF or a higher value

resistor, such as 1kOhm. This component allows connecting the TLP output to the trace. The return current can be achieved by displacement current from the local ground of the probe to the ground of the PCB for high frequencies and by a wire connection to the PCB for the lower frequencies. Now the system can touch the probe to different nets and increase the injected pulse until an error is observed. The current at which this error occurred and the observed failure phenomenon should be recorded.

4.2.3 Rule Checker for Enclosures

Many ESD soft failure and damage countermeasures depend on shielding, or on guiding the discharge current such that the current and associated fields do not cause unexpected coupling. While full wave simulation allows to determine the current paths and fields, it is still a rather complicated method and requires very many model verification runs. A rule checking tool might be able to import mechanical geometry files and estimate currents for flagging weaknesses, such as instable connector shell to enclosure contacts without the need of a full wave simulation.

The rules to be checked would be:

- Connector shells should be connected to the enclosure as good as possible, as even small connection inductances, such as 1nH will all the ESD current to cause large transient voltages between the shell and the enclosure, this voltages will drive currents on the PCBs and they will drive transient fields inside the enclosure.
- Plastic enclosures can usually not be penetrated by high voltage, even a very thin plastic of 0.1mm will withstand 25kV for a brief period of time. However, any small hole will allow penetration.
- Sparks will travel thru very narrow slots, a slot as small as 10um will allow sparks to pass. Thus any two-half plastic enclosure may allow direct ESD discharge to PCBs. As a rule of thumb: Up to 10kV 1mm/kV and above 10kV 1.3mm/kV will prevent ESD discharges.
- The rule checker needs a database that describes the ability of connecting devices to confine the fields. For example, a single layer flexible circuit provides a strong current entry path, as it does not confine the fields of the signals well. The current paths which are estimated inside the system then need to be checked up which of them are close to, or even on structures that confine fields badly. These regions will need special attention, a re-routing of the ESD current might be warranted.
- Avoiding secondary discharges is an important test. Secondary discharges are discharges that are caused by a primary discharge to the system. The primary discharge is usually charging up a not contacted metallic part. If the voltage on this metallic part is high enough relative to close by conductors a secondary ESD will occur. The secondary ESD can have rise times which are much

shorter than the primary discharge, and they can have peak values much larger than the primary discharge, as local capacitances are discharged via gaps which can be highly overvoltaged [97]. The rule checker would identify all floating conductors, then identify if distances to charge carrying conductors are large enough to avoid secondary ESD or not.

4.2.4 Rule Checker for PCB for Susceptibility

Knowing the sensitivity of certain IC pins and using a matrix that connects the pins sensitivity with the likelihood of noise coupling (from external IO, board to board connecting traces, long on board traces, and short on board traces) it should be possible to estimate the coupling to each pin. Additional information can be extracted from the general enclosure structure and from the partitioning in different PCBs and their connections. Existing tools can extract electromagnetic PCB characteristics such that models can be created that include conducted coupling and estimate field coupling. The later might require a data base that estimates the field to net coupling by the field confinement of the structure (for example a single layer flex has a very low field confinement). The needed field strength information can be taken from a full wave simulation at a highly simplified level or by the enclosure rule checker mentioned above. At best this will estimate the sensitivity and at least it can flag risky design choices.

4.3 Reported ESD Failures in Literature

Reported failure mechanisms in literature correspond to interaction of components of systems or describe the impact of ESD on single IC structures. Any ESD failure can be divided into hard or soft-failure depending on permanent or temporary failure is detected. Especially for soft-failures the investigation of the coupling path is very time consuming and information usually is confidential so that detailed descriptions of ESD failure can hardly be found in literature. In Table 4.1 ESD problems of automotive and consumer electronic devices which were available in literature are listed. On system level case studies about hard failures of automotive components considering communication electronics, sensors, and airbags are described in section 4.3.1. For consumer electronics many ESD problems with GMR heads were reported. Most information can be found about hard errors on IC level of devices related to consumer electronics. Usually the specified ESD robustness is lower than for automotive devices. In some cases a classification of ICs according to application area is not possible but failure mechanisms are assumed to be similar for automotive and consumer ICs.

Case studies for soft errors on IC level have been published for example for LCD driver ICs. Other investigations on soft errors treat disturbances in keypads. On system level four cases are described in section 4.3.2 where ESD leads to temporary malfunction of a device.

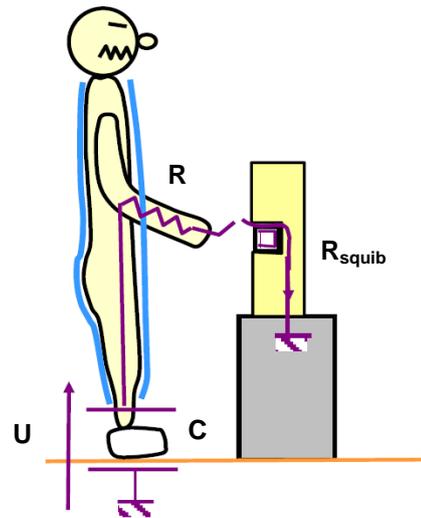
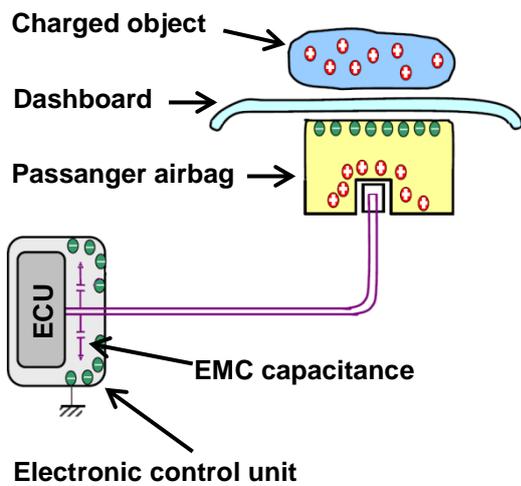
	Hard failure		Soft failure	
	Automotive	Consumer	Automotive	Consumer
System level	K-bus and CAN-bus transceiver	GMR heads	Infrared car key	Slide type mobile phone
	Sensors		TLU on CMOS interface chip	LCD displays
	Airbags			Unwanted keypad response
IC level	Semiconductors	Semiconductors	No information available	Input of a power circuit reacts to <1ns wide pulses
		MEMS, micromirrors		
		USB interfaces		

Table 4.1: Automotive and consumer ESD failure studies

4.3.1 Reported ESD Hard-Failure

One of the well-studied, documented automotive field returns caused by ESD over the last years was published by Renault. More than 1 million vehicles have been recalled because of risk of an unwanted airbag deployment due to ESD [23]. Also other motor vehicle manufacturers like Audi and Ford had quite similar problems with airbags [24]. However a detailed documentation is not available. As an outcome of investigations Renault developed a technical policy to manage ESD risks in airbags.

Two types of ESD sources in automotive environment were identified by Renault. An airbag activation could be initiated by a charged human or a charged garment which was placed on the car dashboard.



(a)

(b)

Figure 4.14: ESD mechanisms for induction charging (a) and human source (b) [23]

In case of a human body as ESD source charging voltages up to 23 kV, a capacitance between 120 pF and 350 pF, and a resistance between 100 Ω and several kΩ were obtained. The stored energy in the capacitor is dissipated in different resistive elements and the energy dissipated in the device under test (DUT) is:

$$E_{DUT} = \frac{1}{2} C_{GEN} U_{GEN}^2 \cdot \frac{R_{DUT}}{R_{GEN} + R_{DUT}} \quad 1$$

R_{GEN} , U_{GEN} and C_{GEN} are the ESD source parameters and R_{DUT} is the DUT resistance. The squib as a DUT has a serial resistance of about 2 Ω. The calculated worst case energy was 1.8 mJ. In the second case strong field coupling between the squib cables and garment caused an activation of the airbag. In comparison to a human discharge the serial resistance of air breakdown is very low. The worst case value that was recorded for the energy through the squib was about 2 mJ. While the worst case energy is similar to human discharge, the required voltage level is according to equation 1 much lower. This type of discharge was reproduced in laboratory environment by shortening a network with serial resistance of a common ESD generator (“0 Ω” discharge). The critical energy of both studied ESD sources was similar. In the developed policy only the “0 Ω” discharges are used, because higher energies can be transferred to the DUT by means of a common ESD generator. The sensitivity of the tested squibs to “0 Ω” discharges ranged between 0.4 mJ and 1.5 mJ depending on the squib type.

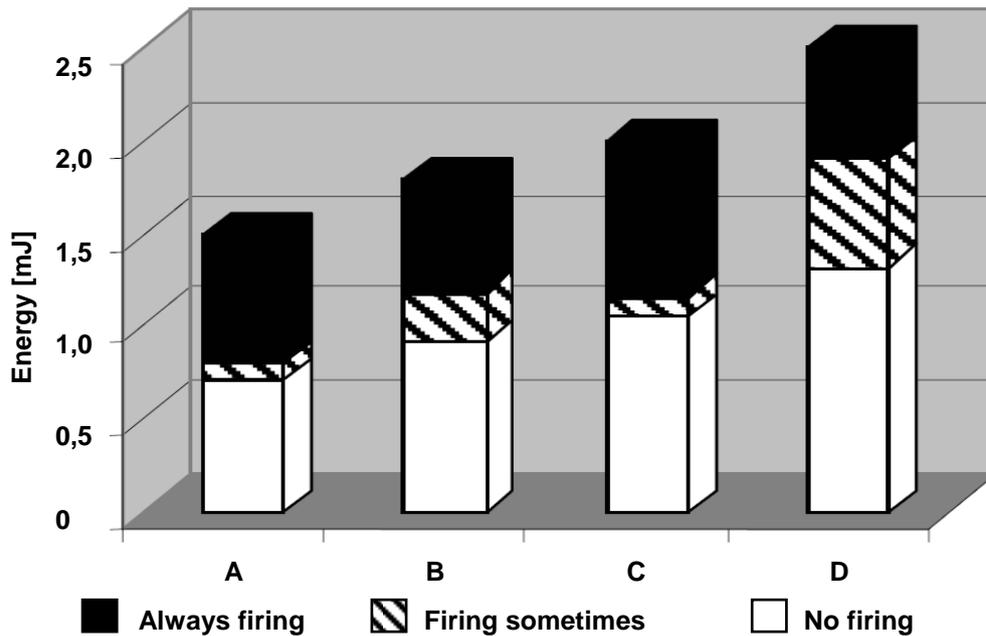


Figure 4.15: Results on ESD tests on different squib types (A, B, C, D) [23]

Nevertheless all of this squibs will withstand 8 kV ANSI/ESD HBM pulse [53], hence the energy calculated with equation 1 through a 2Ω squib would be $4.3 \mu\text{J}$. The policy prescribes an ESD testing level of 9 mJ for a squib and 2 mJ for the ECU. The discharge capacitance 330 pF and a circuit resistance below 30Ω for the ESD generator were defined.

ESD failures with K-Bus transceivers were reported in [25]. Hard failures occurred during the automotive production process, when the cable harness is connected to the electronic control unit (ECU). No problems occurred at any time in the field. A capacitance to ground of about 50 pF is a typical value for a standard ECU. In the reported case a higher capacitance of 300 pF was measured. During assembly the electro-statically charged ECU was discharged via the connector and cable harness, which could lead to a destruction of the bus transceivers. In Figure 4.16 a sketch of a possible discharge current path is given.

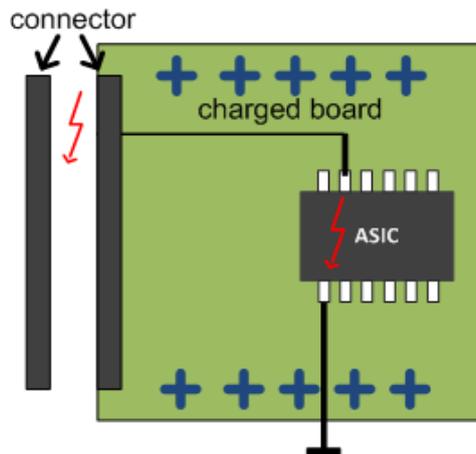
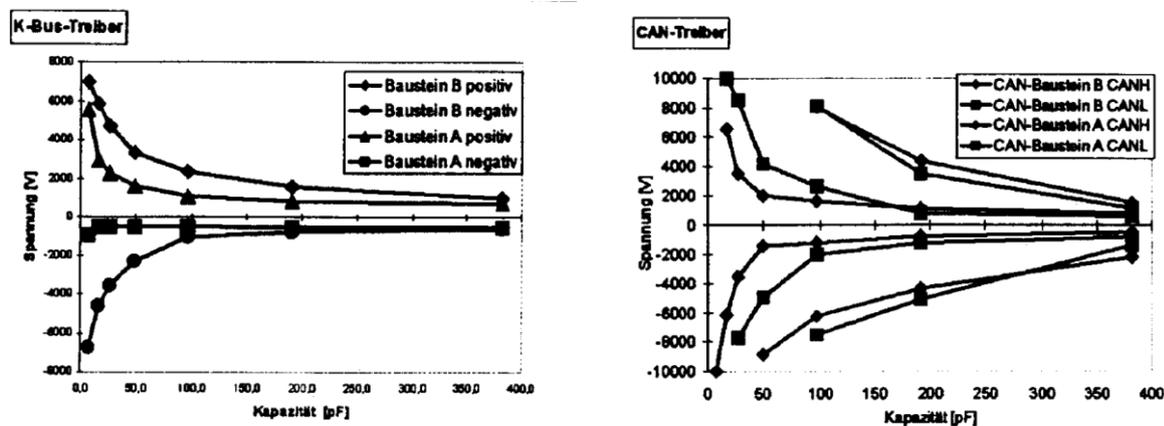


Figure 4.16: Discharge of board capacitance by connecting a cable harness during assembly

As a result a setup and a process for charged board event (CBE) immunity tests were proposed. K-bus-drivers and CAN-transceivers from different semiconductor manufacturers were qualified with the developed methodology. In Figure 4.17 the charging voltage, leading to a destruction of the bus transceivers, is related to different board capacitance. It has been shown that a 2 kV CBE event for a board with 300 pF can cause physical damages on both IC types.

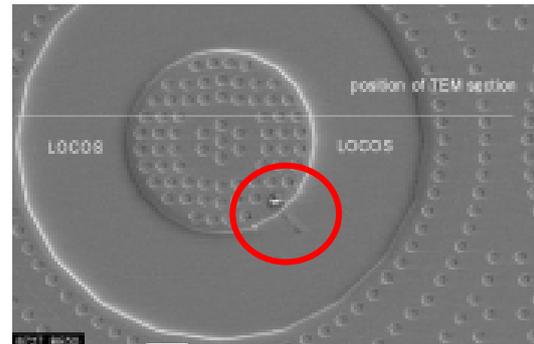
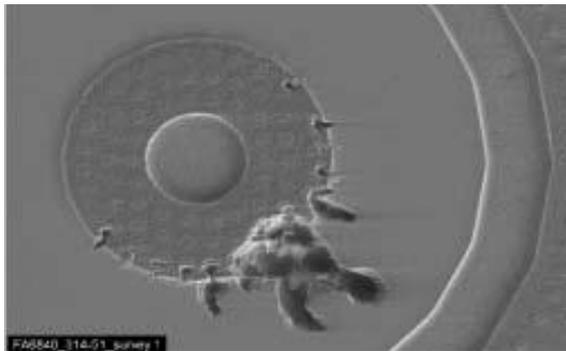


(a) K-transceiver

(b) CAN transceiver

Figure 4.17: Destruction voltage level and PCB capacitance for different bus-transceivers [25]

In [26] a damage on a sensor was reported by Siemens VDO. A sensor was connected to the control unit by a long cable of about 2 m. The sensor IC was specified with 4 kV HBM and 400 V MM. The connection of the ECU during assembly process was identified as the main failure mechanism. Single cable discharge events with charging voltage of about 200 V were responsible for IC destruction. In Figure 4.18 different destruction patterns were observed in during the production process and in the laboratory.



(a) After 15 kV IEC test in the lab

(b) Destruction in assembly

Figure 4.18: Investigation of hard failure of programmable ASIC [26]

The affected IC has an internal protection circuit with breakdown voltage of about 63 V. In the circuit a capacitor (>1 nF) is connected to the affected pin as shown in Figure 4.19.

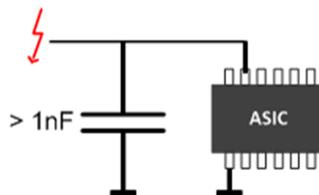


Figure 4.19: External capacitor connected to ASIC

If the transients are too fast, the ESD protection circuit is not triggered. Then multiple low voltage discharges can charge the capacitor up to 63 V. In case of a charged capacitor of about 30 V the ESD protection circuit was triggered by an additional single discharge leading to a possible damage of the IC. Multiple discharges can occur by connecting the cable harness to the sensor. Figure 4.20 shows the current waveform which was measured during investigation.

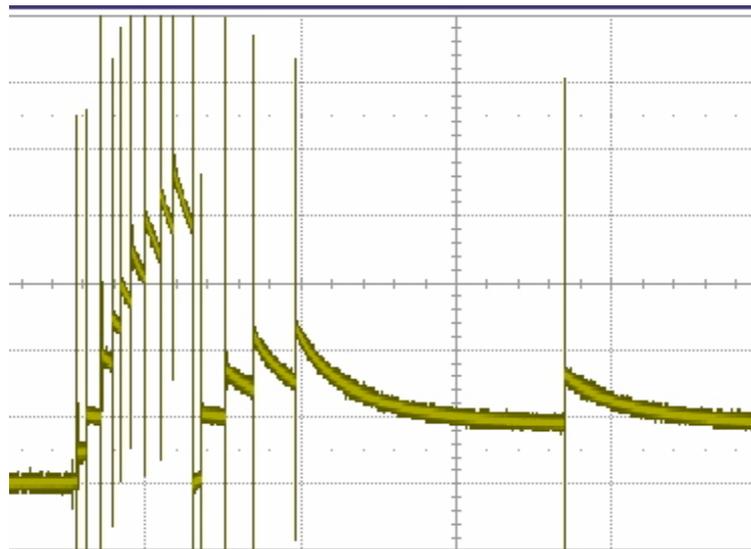


Figure 4.20: Multiple discharges after connecting the cable harness [26]

The isolating connector material contains conductive particles (carbon). Different charging in multiple regions within the plastic connector enforces multiple discharges. The author assumes that the multiple discharges can be related to charging and discharging processes of these regions.

In [27] ESD hard failures occurred in USB communication interfaces. During investigations the failure could be referred to a defect USB cable where the ground pin was not connected. In a testing setup measured CDE current amplitudes exceeded the onboard ESD protection capability.

Two hard failures on IC level due to CBE were reported in [8]. High failure rate (6,7 %) was obtained with a CMOS amplifier during board level testing. The peak current during a CBM discharge was much higher than during a CDM discharge. All devices passed 2000 V HBM and 1000 V CDM levels, but failed 375 V CBE test. CBE current peaks with 375 V charging voltage were 3 times higher than in the case of a CDM discharge.

The second example was a CMOS DSP IC. A high failure rate was obtained during system level production testing. The required charging voltage to damage the DSP at board level was 250 V, which is about 10 % of the required voltage at component level.

In [28] several techniques to improve ESD robustness for high voltage I/O designs in automotive applications were proposed on IC level by a semiconductor manufacturer. In a case study an automotive chip with 40 V I/O pins of a current-voltage monitor using Hall effect for an ignition system was analyzed. In the schematic shown in Figure 4.21 the IC is protected by a 40 V ESD clamping circuit. However, the integration with a specific HV diode consistently generated weak HBM performance.

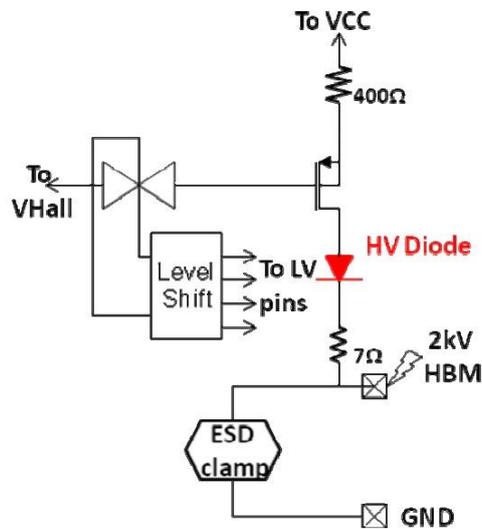


Figure 4.21: Schematic of the VHall I/O block including a HV diode [28]

During ESD testing the IC pin failed at 2 kV HBM. After optical inspection of the silicon surface, damages could be clearly identified on the cathodes of the HV diodes while the ESD clamps were intact. The damage is shown in Figure 4.22.

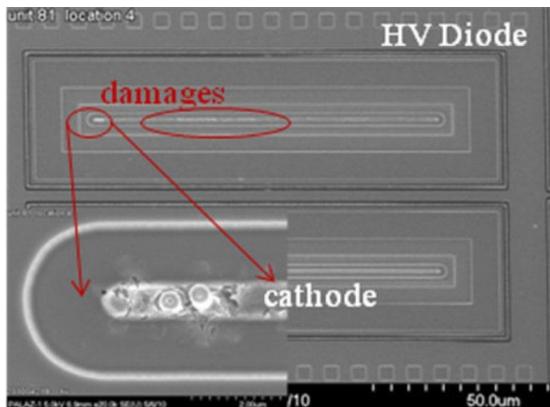


Figure 4.22: Damages on the cathodes of the HV diodes [28]

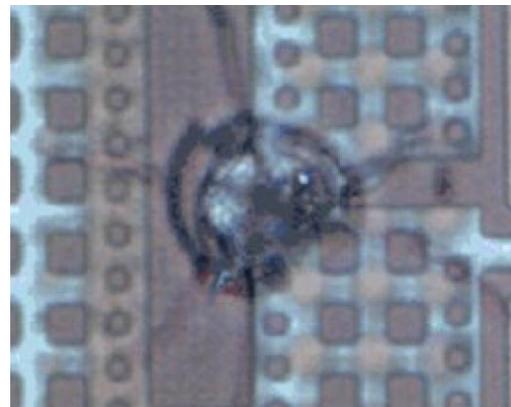


Figure 4.23: Discharge through the inter metal dielectric layer towards a grounded structure [29]

Often ESD damages are reported that happened during manufacturing process of semiconductors. In [29] a charge induced damage (CID) into a metal interconnects is reported. The damage is caused by the build-up of charges on a resistive surface during a water rinsing step. This charging induces a mirror charge on the interconnect circuitry and results in a discharge through the inter-metal dielectric layer (IMD) towards a grounded structure. This CID can lead to direct severe yield loss. The observed damage is shown in Figure 4.23.

Many ESD errors on IC level are reported for micro electro mechanical systems (MEMS). In [30] the ESD robustness of MEMS used as switching element in optical networks was analyzed. A very low failure level of 40 V HBM on 5x5 8µm micro-mirrors with SiGe interconnects was obtained. The high sensitivity of MEMS to ESD is influenced by their high impedance as well as by the resistivity of the substrate material. Layout of the device design and choice of material is crucial for the ESD failure level of MEMS. Figure 4.24 shows that single mirrors are damaged after 40 V HBM testing.

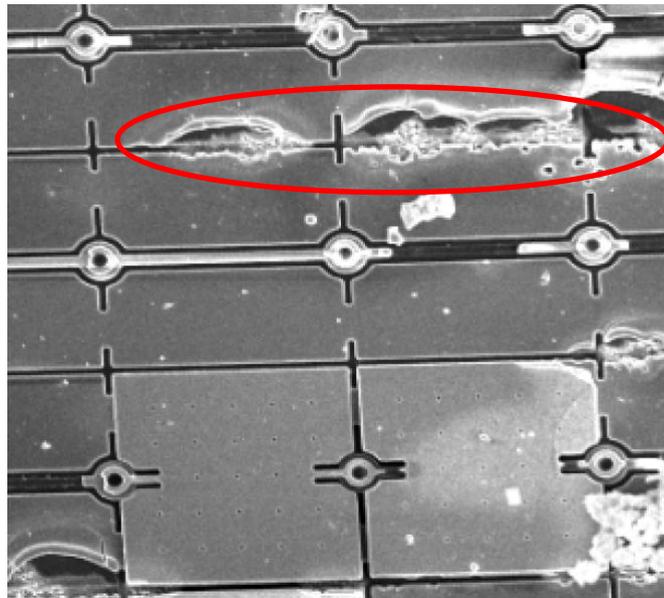


Figure 4.24: Failure levels of 40 V HBM on 5x5 8µm micro-mirrors with SiGe interconnects [30]

Similar to MEMS giant magneto resistive (GMR) heads of hard disks can be damaged by very low ESD events. ESD problems with giant magneto resistive (GMR) heads were reported from consumer electronics industry. In [31] a classification was proposed where different error types can be deduced from HBM charging voltage levels. In a case study hard ESD damage was obtained for charging voltage levels not much higher than 10 V and soft ESD damage is caused at 6–10 V. A hard error is obtained for mechanical destruction of the semiconductor material. In Figure 4.25 pictures of the semiconductor before and after ESD stress are shown. The inter-layer diffusion-type hard ESD damage occurs by metal contact with a shunting metallic fixture and the read element circuit. The magneto resistive ratio is reduced from its normal value. The process was improved by replacing the metallic fixture with conductive ceramic. Soft ESD damage is obtained if magnetic destruction (defect of the permanent magnet) or defects in free layers are detected.

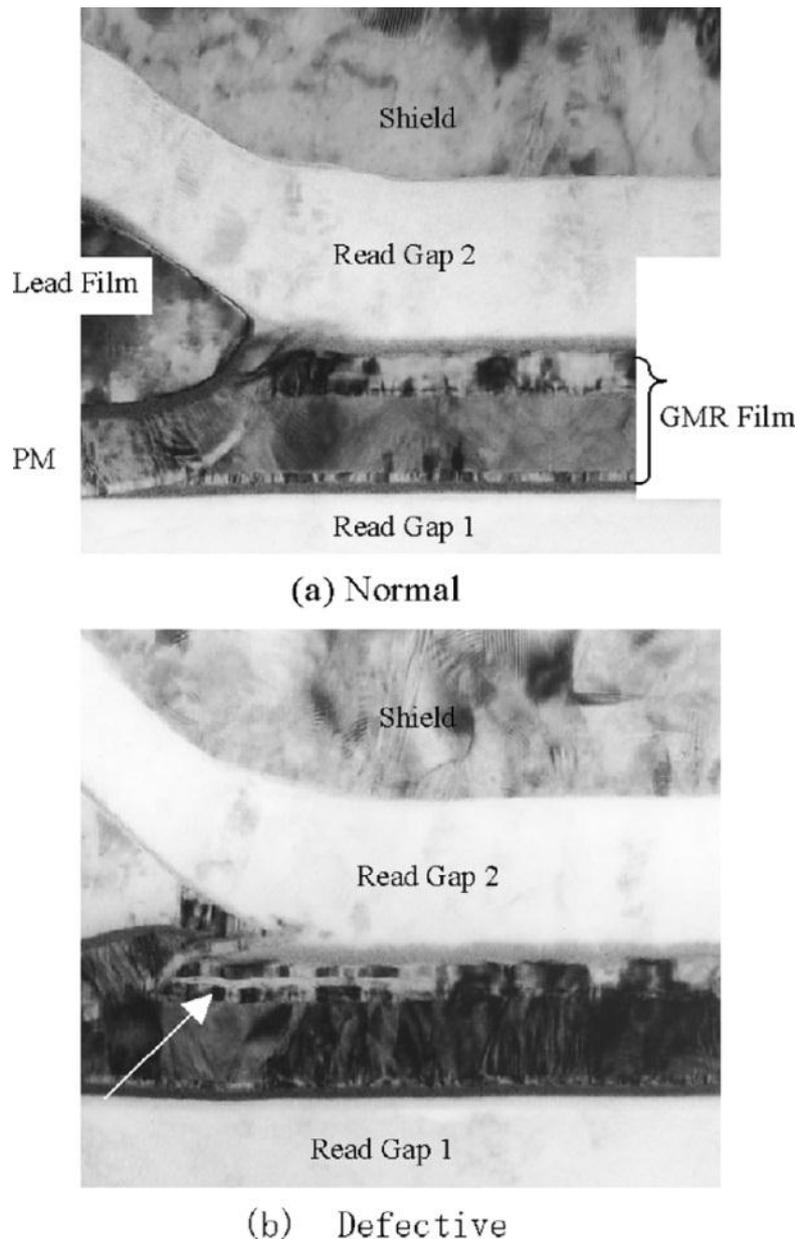
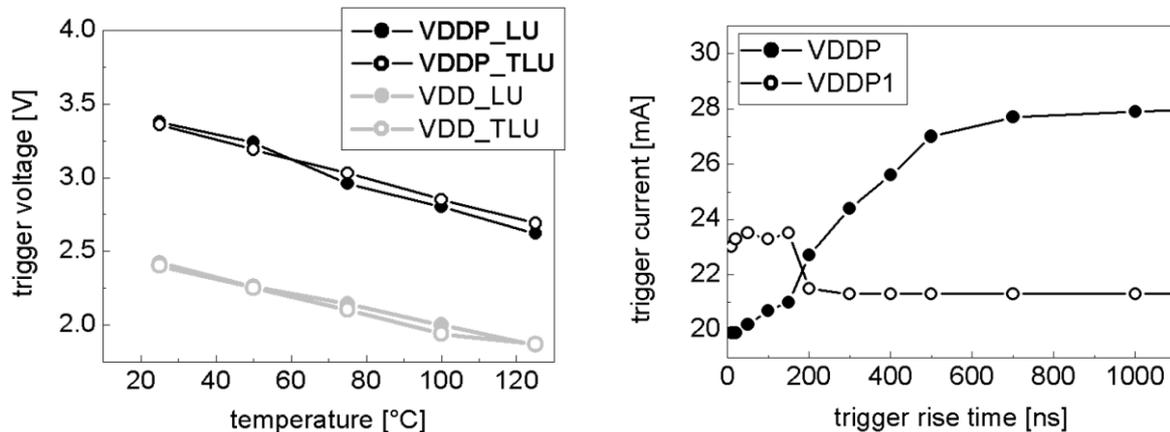


Figure 4.25: Interlayer diffusion in GMR heads before (a) and after ESD (b) [31]

4.3.2 Reported ESD Soft-Failure

The transient latch-up (TLU) has been investigated and compared to “static” latch-up in [32]. Particularly the influences of parameters like temperature and trigger characteristics on the threshold of TLU have been addressed. To represent a real system level ESD stress, cable discharges and discharges from transmission line pulser (TLP) were used as a trigger. The authors have shown that the ambient temperature is the most critical parameter for both transient and “static” latch-up. In Figure 4.26 the increasing device temperature up to 100 °C can lead to a smaller latch-up trigger voltage (factor 2 – 3) in comparison to lower temperatures. As a conclusion the worst-case testing level should be specified at maximum temperature

of the application of the IC. Influences of rise times of the trigger current were found to be less than a factor 2 during experiments. It has been shown that CDE can trigger a TLU and the CDE can be reproduced with a TLP, since the initial peak of cable discharge has less influence of trigger behavior. The results are shown in Figure 4.26.



Temperature dependency of LU and TLU V-supply test on VDDP and VDD of TC1

TLU threshold trigger current (negative polarity) of TC2_IO1 versus rise time of the trigger pulse ($t_d = 100 \mu s$) at 100 °C ambient temperature

Figure 4.26: TLU dependency on temperature and rise time [32]

Currently the industry council on ESD target levels is publishing white paper III which provides a larger section to fast transient latch up. The paper should be available by the end of the year 2012.

Another soft-error was reported by Siemens VDO in [26]. After transport of a remote car key over large distances internal batteries were discharged. A static electrical field as a reason could be excluded. The DUT shows no reaction for 200 kV/m field strength. The measured impedances of about 10 kΩ of the key IC supported this result. Investigations on transient fields by friction of the key over plastic surface have shown that sequences of micro discharge pulses due to continuous friction can be responsible for the malfunction. A current was induced by E-field coupling into the trace of about 2,5 cm length shown in the sketch in Figure 4.27. Specific environmental conditions have increased repetition frequency of the pulses so that a valid signal was detected by the IC initiating a testing mode with high current consumption.

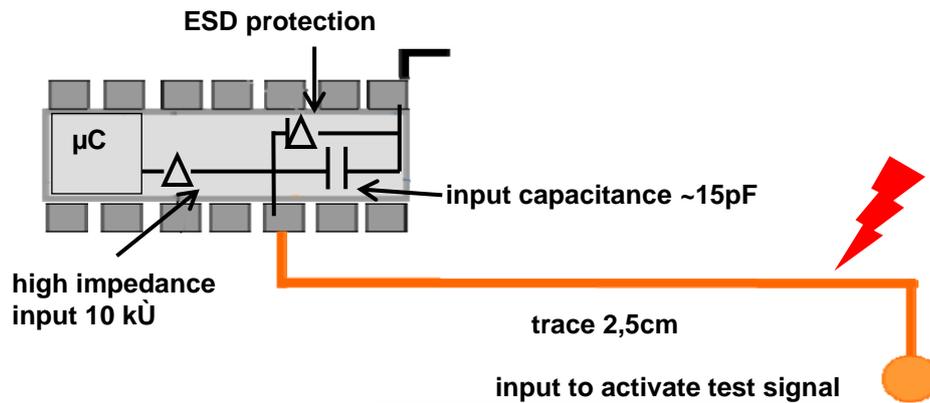


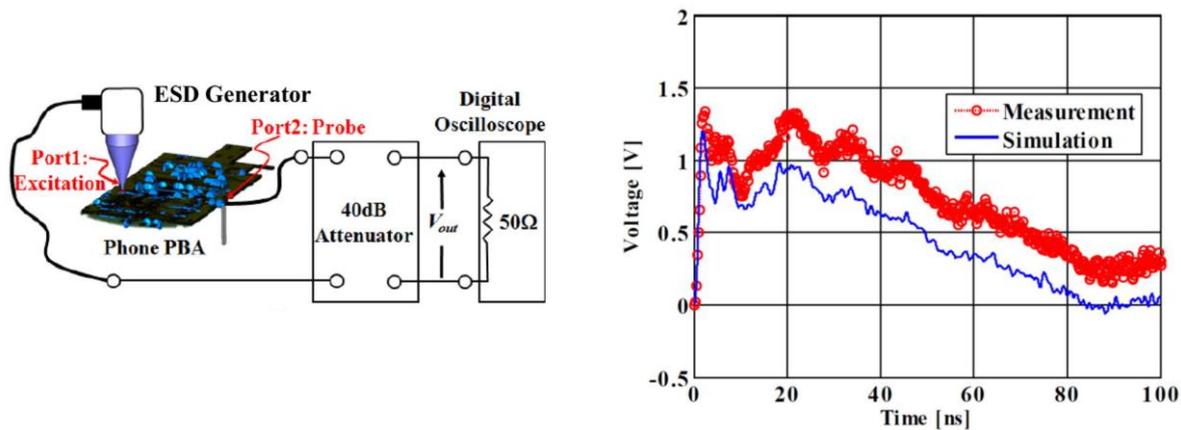
Figure 4.27: Schematic representation of the component [26]

Some further reported examples for soft errors can be found for consumer electronics. Nondestructive ESD problems like stripes on the display or display's optical parameters changes can be observed with any LCD device. A methodology to identify and model the upset is presented in [33] and proposes four steps:

- The sensitivity area causing the failure is located by ESD scanning
- Behavioral SPICE model is developed to simulate ESD failure, using the local injection measurement currents
- A full wave block level model is used to extract the current densities at the sensitive area
- Current densities are imported into the SPICE behavioral model to predict ESD upset level

The proposed model has shown a good correlation between measured and predicted upset level using four different conditions for system level testing. Complexity of the method is high.

In [34] soft-failures of a slide type Samsung mobile phone has been analyzed and a systematic analysis methodology has been proposed. The process consists of ESD simulation and characterization of the mobile phone. The soft-failure is visible by a freezing of the device when discharging the ESD-gun on its metallic case. A setup and current waveforms are shown in Figure 4.28. As a protection circuit RC low-pass filters were designed. In ESD simulation, improved immunity and increased voltage-level of signals, which can cause the soft failures, could be found. The modified mobile phone was characterized again and no more soft failures were detected.



(a) Schematics of measurement setup.

(b) Measured and simulated time-domain waveforms cell phone case

Figure 4.28: Experimental verification of simulation models [34]

Also LCD screens can be sensitive to ESD. Discharges can change the register values of the LCDs leading to picture distortion, change in brightness etc. Methods such as shielding (using a conductive glass), diverting the currents away from the connecting flex circuit cables, and a variety of other methods are used to avoid soft error disturbances of LCD screens. This includes detecting ESD events and triggering a refresh of registers, IC design changes etc. The authors of the papers listed below treat LCD soft error problems in detail [76] - [81].

5 Reported Case Studies from FAT AK 23

5.1 Trailer ECU

A trailer ECU shows malfunction after ESD via the trailer wiring harness. The trailer body is often electrically isolated from the vehicle by special trailer hitches. Even a ground wire connection of the trailer cable harness to the chassis might not be available. According to different physical effects and environmental conditions an electrostatic charge of trailer body can be observed. A discharge between the trailer chassis and single wires of the cable harness is possible.

Different malfunction were reported such as permanently activated brake lights. As subsequent failure of vehicles automatic transmission gear shifting does not work and a trip may not be continued.

Investigation has shown that a diode of the brake light switch (BLS) circuit of the trailer ECU can be destroyed by high voltage pulses [52]. A suspected failure path is a discharge between trailer socket and hitch which causes a field coupling into the cable harness or BLS wire.

Two versions of the ECU are available. Version A is equipped with and version B without an additional 68 nF capacitor parallel to ground at the affected diode pin. No malfunction was reported for the version A. Details are presented in chapter 8.

5.2 LED Rear Light

A LED rear light shows malfunction due to electrostatic induction. When removing a protection foil from the front plastic surface, it could become electrostatically charged. The generated electrostatic field causes induction charging in a floating conducting plane. An ESD event may take place and destroy sensitive electronics on the device. Modification of constructional could help to prevent failures. Details are presented in chapter 8.

5.3 Knock Sensor

Charging effects due to heating and cooling were investigated on a knock sensor. ESD failures can occur when screwing the knock sensor on the motor block during assembly and then plugging an ECU via a cable harness to the sensor. Investigation results are presented in section 8.7.

6 Demonstrator PCB and PCBs for IC Characterization

A special test-board [53] was used considering different PCB-trace configurations. Different types of automotive IC pins can be selected as terminations of the traces. The ESD behavior of LIN-, CAN-transceivers and an 8-bit μ C can be investigated. More information about ICs and the IC sections of the demonstrator can be found in chapters 6.1.3, 6.1.4 and 6.1.5.

In order to create IC failure models, different characteristic datasets of each IC pin have to be measured with a TLP setup for modeling. To ensure a high level of accuracy two special PCBs were designed. The layout for LIN and CAN-transceivers is shown in section 7.6.4. Selected pins of an 8-bit μ C are characterized using the second board described in the same section.

All PCBs are designed double-sided and were manufactured on FR4 material (thickness: 1.55 mm). The thickness of the copper traces is 35 μ m.

6.1 ESD Demonstrator PCB

The demonstrator PCB was designed to investigate the disturbance of automotive systems by on-PCB coupling effects caused by ESD. As a second item the potential failure of ICs with lower ESD robustness is analyzed. The allover layout is shown in Figure 6.1. It can be divided into 4 main sections:

- Voltage regulator
- Cross-talk section with long parallel traces
- Section for investigations with μ C (XC-864)
- Section for investigations with LIN transceivers
- Section for investigations with CAN transceivers

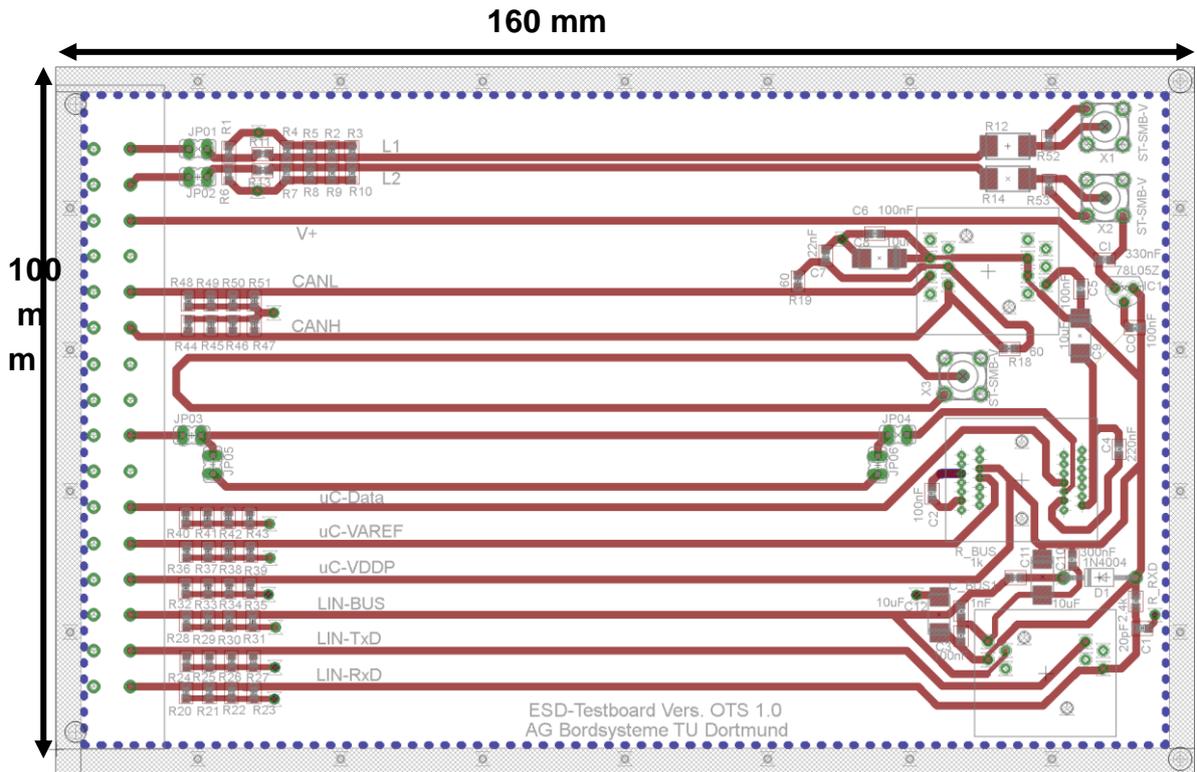


Figure 6.1: ESD demonstrator PCB layout

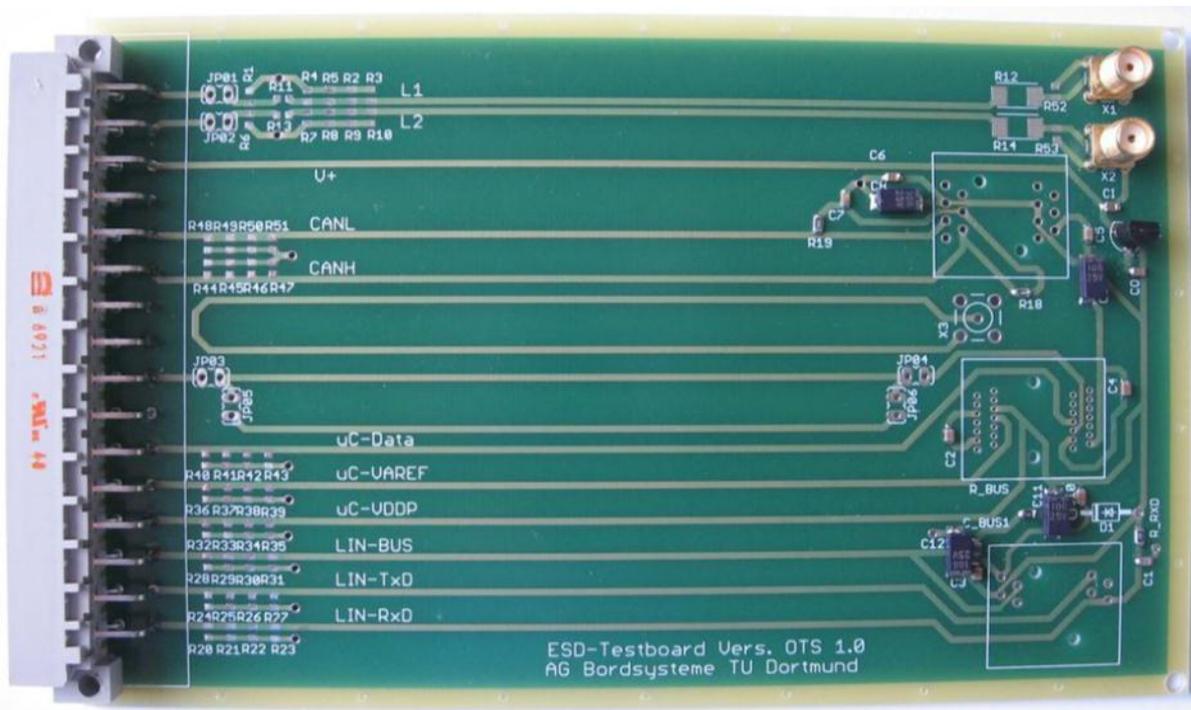


Figure 6.2: ESD demonstrator PCB with connector

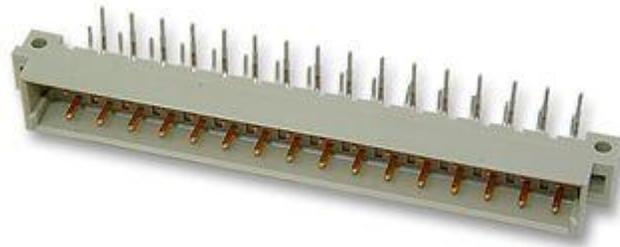


Figure 6.3: Connector of demonstrator

A 2-row “Harting 09 04 132 6921” connector with 32 pins was chosen for the demonstrator. It is similar to typical automotive connectors. The allover width is 88.9 mm. The connector is suitable for a 5.08 mm grid.

6.1.1 Voltage Regulator

A “Texas Instruments LP2950” voltage regulator was considered in the layout to provide a 5 V supply to the ICs, if powered tests are required. The functional block diagram is shown in Figure 6.4. Basic characteristics of the element are listed below:

- Wide input voltage range: up to 30 V
- Stable with low ESR ($>12 \text{ m}\Omega$) capacitors
- Rated output current of 100 mA
- Current- and thermal-limiting features
- Low dropout: 380 mV (typ.) at 100 mA
- Low quiescent current: 75 μA (typ.)

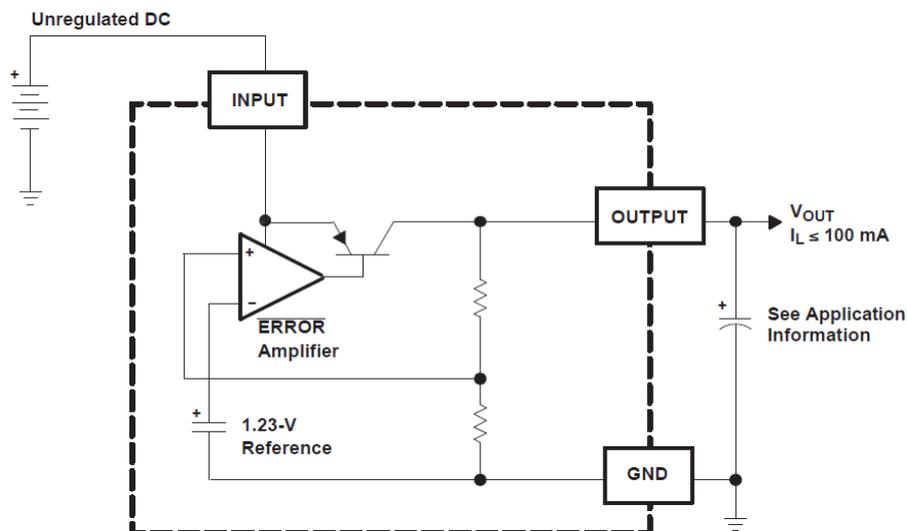


Figure 6.4: Functional block diagram of voltage regulator

In the layout the voltage regulator is connected to a 330 nF and 100 nF capacitor on the input and output pins (Figure 6.5). Larger blocking capacitors are not used as influence on ESD pulse propagation is low.

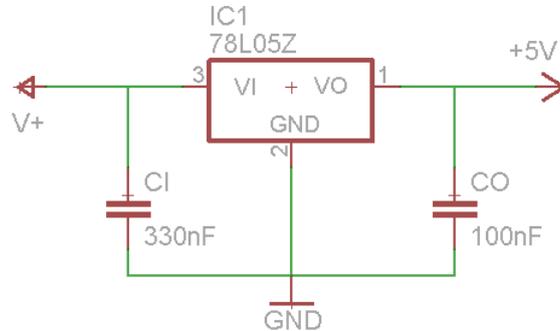


Figure 6.5: Circuit of voltage regulator

6.1.2 Coupling between Parallel PCB Traces

Basic coupling effects can be investigated by two parallel PCB traces. The layout of the coupling (cross-talk) section is shown in Figure 6.6. A charged structure can be discharged into the upper conductor and the coupled signal can be measured on the lower conductor. Two traces of 1 mm width are placed in 0.5 mm distance to each other. Each trace can be terminated by several serial and parallel elements at both ends. Jumpers allow including the connector in the setup if additional loads or wires should be connected or the influence of the connector should be part of the investigation. The signals on both lines can be measured with an oscilloscope via SMA-connectors or by using small current sensors like Tektronix CT1 or CT6.

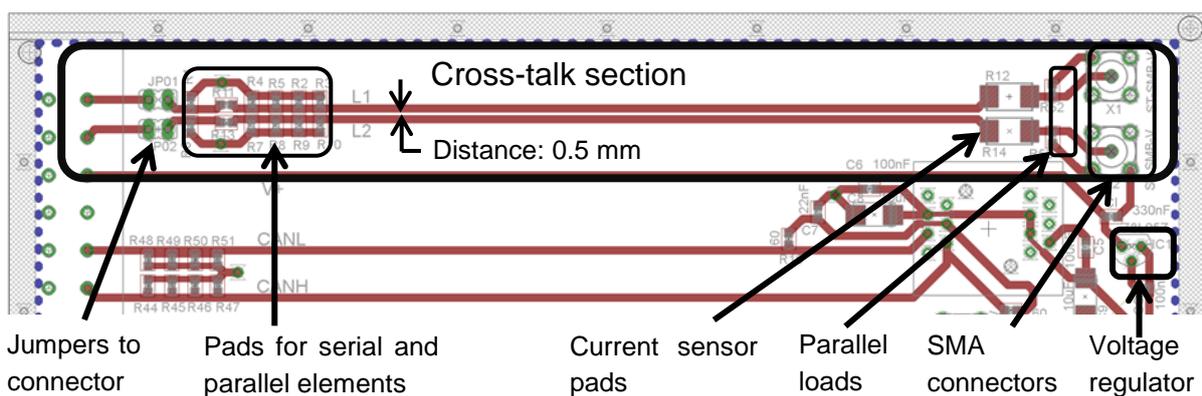


Figure 6.6: Cross-talk section of demonstrator

Field coupling on PCBs can occur if conducting loops are part of a design. On the demonstrator board two loops were designed to investigate the potential disturbance of ICs by this effect. If a network is discharged into a conductor close to the loop the induced current can be measured via a SMA connector with an oscilloscope. A

second loop configuration can be chosen with jumpers. The discharge current can be impressed into the connector pin and the loop trace can be terminated with an IC pin.

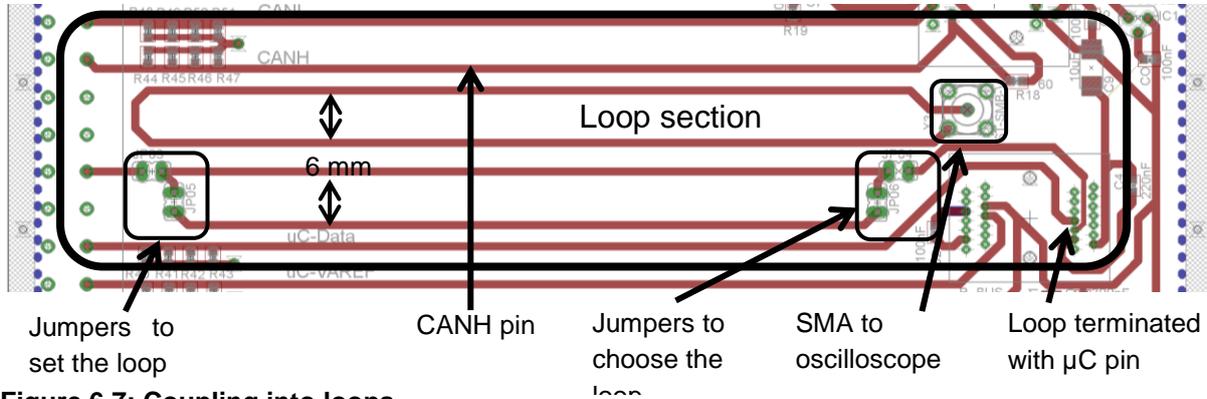


Figure 6.7: Coupling into loops

6.1.3 μC

The main functionality of automotive electronic control units (ECU) is implemented with programmable microcontrollers. The complex ICs contain different types of elementary circuits. To increase the variety of test options on the demonstrator board several pins of an Infineon 8-bit XC864 μC are considered for testing in the layout.

Two multipurpose I/O pins and two supply pins (“I/O port supply”, “core supply monitor”) were selected for testing. The μC pin out is shown in Figure 6.8.

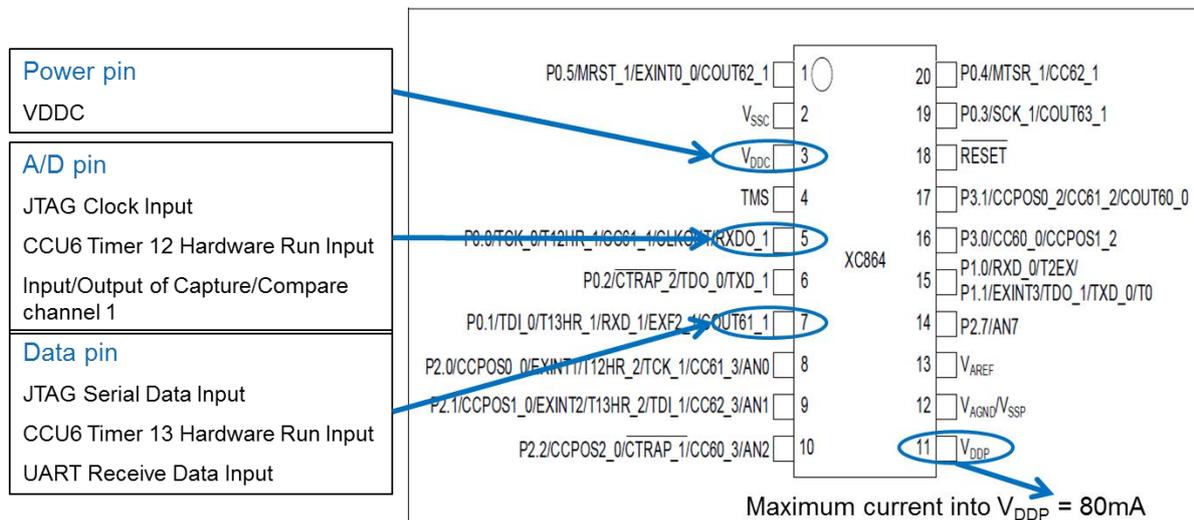


Figure 6.8: Selected pins of μC for investigation on demonstrator PCB

In the circuit diagram in Figure 6.9 all connections to the μC-IC are drawn. A 10 μF and a 300 nF capacitor are connected at VDDP pin. 100 nF are connected to reset input and 220 nF are soldered between VDDC and supply ground pins.

The layout of the demonstrator in the μC section is shown in Figure 6.10. Because of a better availability a TSSOP28 socket is used in the design so that 8 pins of the

socket are left open on the IC side. The data pin, VREF pin, VDDP pin and AD pin are connected to the connector and can be tested with different testing devices. In case of VDDP, VAREF and Data input ESD protection elements can be added parallel to ground.

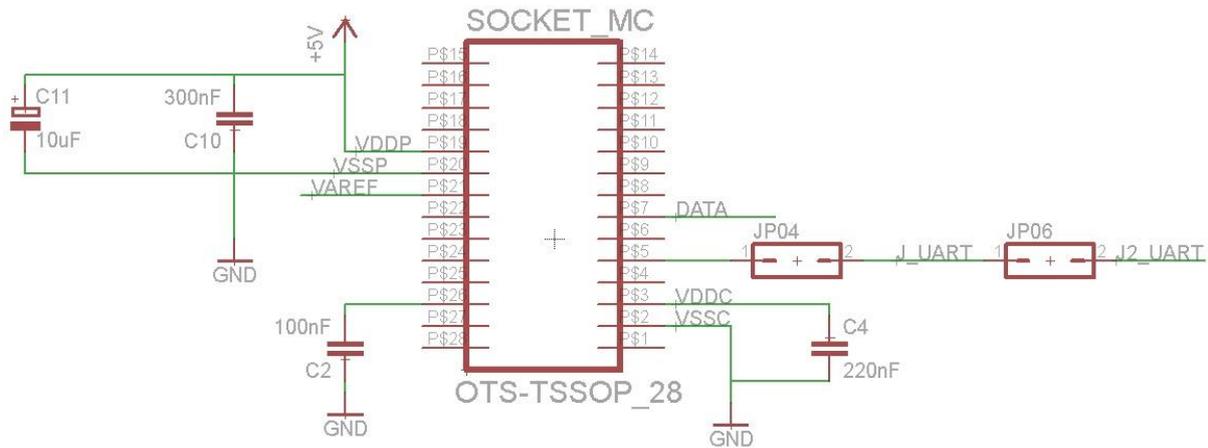


Figure 6.9: Circuit connected to µC on demonstrator

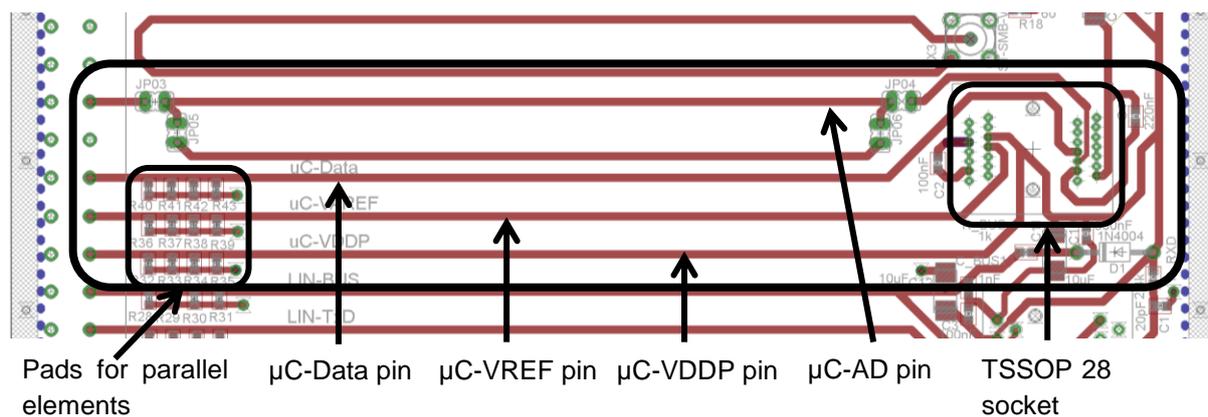


Figure 6.10: µC section on demonstrator PCB

6.1.4 LIN Transceivers

Three different LIN transceivers were selected for testing. The LIN-bus, LIN-RxD and LIN-TxD pin are connected to the connector on the demonstrator board. For protection parallel elements can be soldered in the current path of each pin. ESD-tests should be done with 100 nF capacitors at LIN-RxD and LIN-Bus pins. The circuit and layout section for LIN transceivers is shown in Figure 6.11 and Figure 6.12.

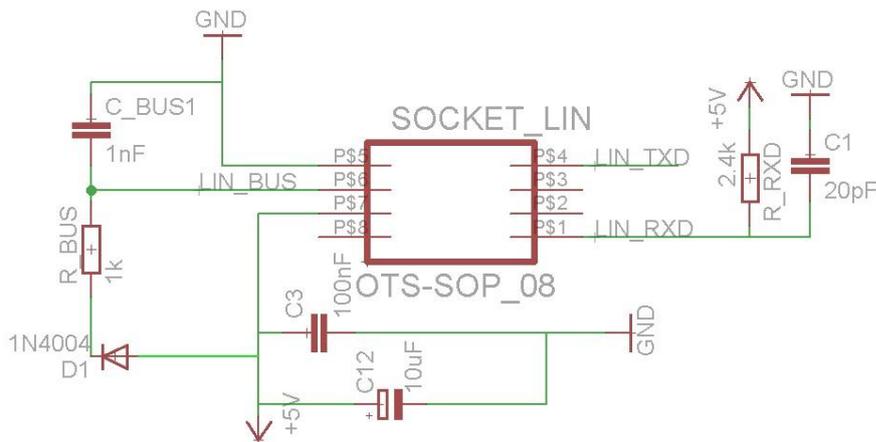


Figure 6.11: Circuit for LIN transceivers on demonstrator PCB

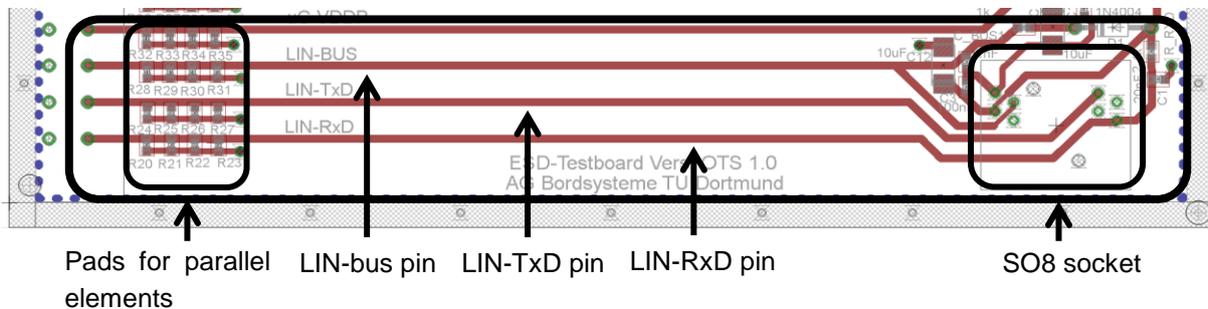


Figure 6.12: LIN section on demonstrator PCB

6.1.5 CAN Transceivers

Similar to LIN transceivers often CAN transceivers are part of automotive electronic control units. The layout is shown in Figure 6.14. The CANH- and CANL-pins are connected to the demonstrator connector and can be tested in different configurations with optional parallel elements. For ESD testing SPLIT termination and 100 nF at V_{CC} , $V_{\mu C}$ and V_s pins can be also considered as can be seen in the circuit diagram in Figure 6.13.

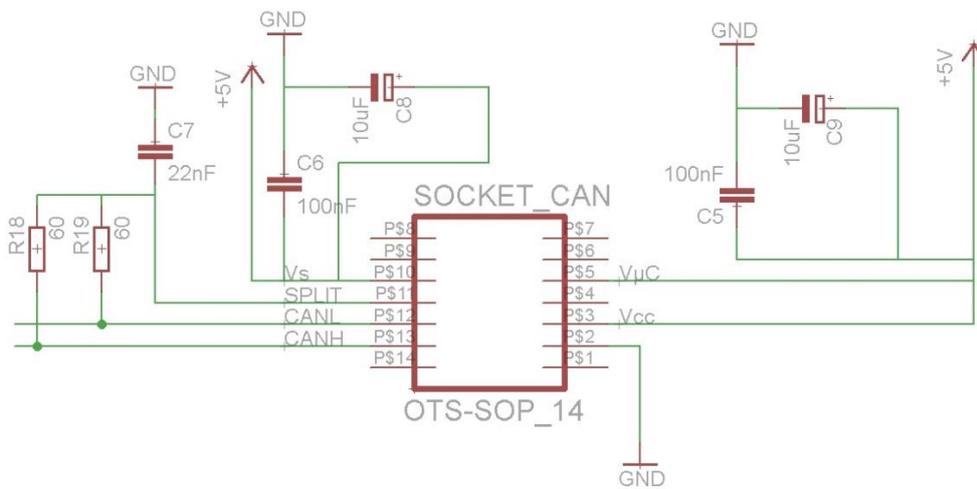


Figure 6.13: Circuit for CAN transceivers on demonstrator PCB

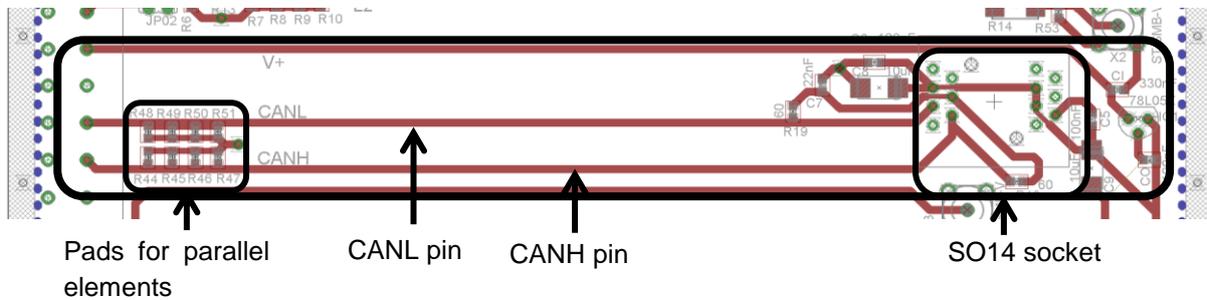


Figure 6.14: CAN section on demonstrator PCB

7 Modeling

7.1 Comparison of ESD Models Used in Different Test Standards

All ESD test methods try to reproduce an ESD scenario that the DUT can be subjected to. Generally, they distinguish between “production environment” and “user environment” where user environment is often referred to as system level. The production environment is usually ESD controlled, consequently the charge levels are lower, and however, the ESDs can hit components or other structures inside the system.

A second important difference is the type of effect that is observed. Most IC level testing is only observing for physical damage to the IC, while system level is observing both upset errors and physical damage of a product or sub-assembly. Only latch-up testing on ICs is observing for non-destructive latch up conditions, as the test is performed with power attached, while CDM, MM and HBM testing are all performed without applying power to the IC.

The third differentiation is related to the coupling path. Tests that observe upset type errors also need to take coupling via transient fields into account, while damaging effects can mainly be achieved by directly conducting large currents or applying large voltages to pins directly.

In general, there is a tendency to create an ESD test for every type of ESD scenario, which will lead to an ever increasing number of ESD tests. Instead it is better to observe at the DUT level the voltages, currents, fields and upset mechanisms and to identify which present test, under which set of parameters will reproduce this situation best. A good alternative method is the usage of arbitrary waveform generators coupled to power amplifiers to set disturbance levels and waveforms via software and then to couple these noise waveforms to the DUT for testing. This creates, within the limits of the amplifiers a very flexible methodology for investigating the robustness of DUTs and ICs. Details can be found in section “Arbitrary Waveform Generator with Power Amplification”.

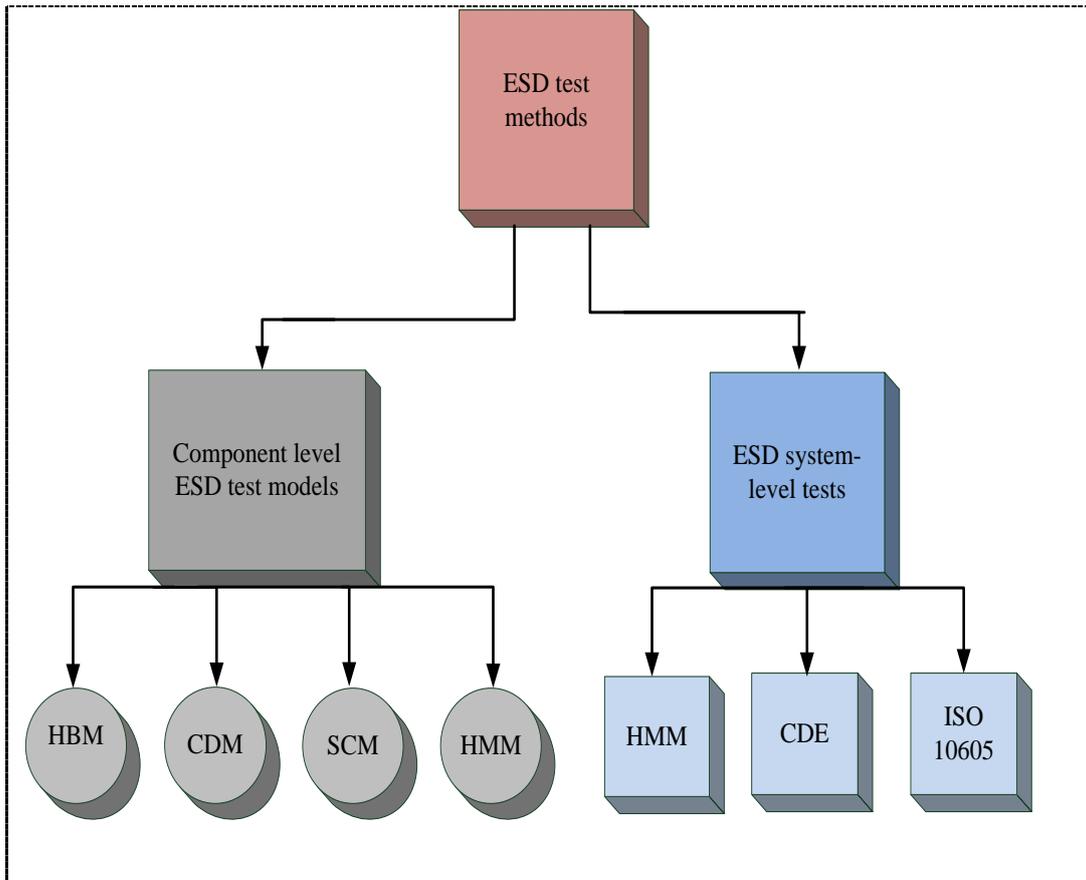
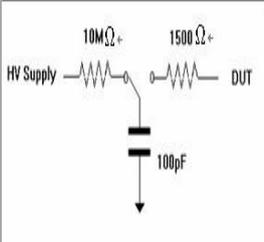
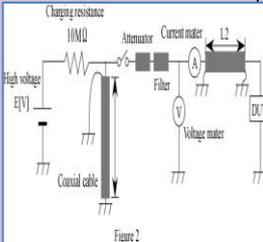


Figure 7.1: Classification of component level ESD test models and system-level tests [104]

7.1.1 Comparison of Different ESD Models:

The main idea behind an ESD model is to replicate the real ESD events. Due to the plurality of real ESD events there are different types of ESD models available. For example HBM (Human Body model) simulates the ESD from a human finger to an IC; CDM simulates the discharge that occurs when a charged IC touches a grounded metal. Hence it is important to compare and contrast all the ESD models so that an appropriate choice of model can be made depending on the type of application. Comparisons of different ESD models are shown in Table 7.1, Table 7.2 and Table 7.3

Parameter	MODEL			
	HBM	CDM	TLP (test method)	CDE
ESD type	Simulates the ESD from the skin of the finger to an IC	Simulates the discharge that occurs if a charged IC is touching a grounded metal surface	Used to determine VI curves, destruction thresholds on IC and systems, and for susceptibility soft error scanning.	Emulates the transient currents and voltages that occur when a charged cable is connected to a DUT.
Qualification levels	1kV (reduced from 2kV)	250V (reduced from 500V)		In general levels of 3000V are considered to be sufficient to replicate discharges of cables, such as LAN and USB cables. Care must be taken as cables can be charged in common mode (= all wires are charged to the same voltage), differential mode (=one wire is charged against another), outside charges (=charges on the outside of the jacket induce polarization on wires). Further, if multiple pins contact in at different times, conversion from one mode of wave propagation to another can occur. The example of the knock sensor is a good case to show common mode and differential mode cable discharge.
Environment	Production (ESD controlled)	Production (ESD controlled)		User (system level) also during production

DUT condition	Powered Off	Powered Off	TLP is a test method, not an ESD scenario	Both possibilities. For upset and latch-up errors the DUT must be on.
Pulse width	150ns	2n	Typically 10-100ns	Typically >10 – 100ns
Rise time	2 - 10ns	100-500ps	100-500ps, high voltage low passes can be used to test for the response at longer rise times	100-500ps, low pass filters can be used to increase the rise time
Peak current	1.33A	1 - 16A (depends on the size of the IC)		The peak current into a short depends on the impedance of the system. System impedances vary usually from 50-300 Ohm
Equivalent circuit parameters	 <p>$R_c = 25\Omega$; $C_D = 15pF$; $L_D = 10nH$</p> <p>The parameters depend on the size of the IC</p>		 <p>$R_c = 10M\Omega$;</p> <p>Other TLP configurations are possible. The voltage and current can also be measured by observing the forward and the reflected wave form</p>	In most cases a transmission line pulser waveform is similar to CDE. In a multi-wire cable that is not shielded, such as unshielded LAN one has to be careful as the different contacts will not contact at the same time, thus, a charge on the outside of the jacked can be converted into a differential mode current by a sequence of pin contacts.
ESD energy	50uJ for 1kV	7.5uJ for 1kV Depends on the size of the IC	Depends on the cable length used	Depends on the cable length used

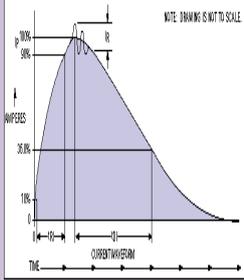
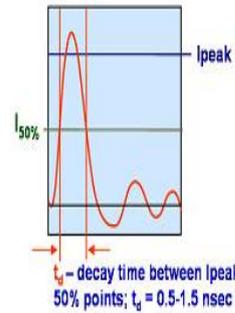
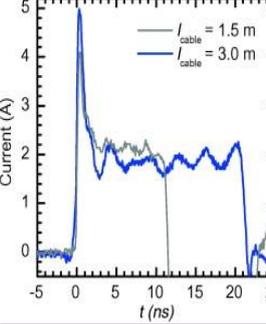
<p>Waveforms</p>				 <p>Typical CDE of a wire of 1.5 m and 3.0 m length, VCDE = 1 kV.</p>
<p>Number of discharges per pin</p>	<p>Variable; function of pin-out</p>	<p>6 (3 positive & 3 negative)</p>		
<p>Package dependency</p>	<p>No</p>	<p>The smaller the IC, the lower the capacitance will be.</p>		<p>CDE is increasing in its importance in field failure according to the experience of the authors of this study.</p>
<p>Relevance to system level ESD</p>	<p>Moderate decreasing but</p>	<p>Not relevant to system level ESD</p>	<p>TLP is a test method</p>	<p>Growing importance as faster I/O are harder to protect. A TLP can reproduce the waveforms from CDM well.</p>

Table 7.1: Comparison between HBM, CDM, TLP and CDE models

7.1.2 Differences Between HBM, HMM and TLP:

Parameter	HBM	HMM (IEC 61000-4-2)	TLP
ESD type	Simulates the ESD from the skin of the finger to an IC	Simulates the ESD current of a person holding a metal object such as a screw driver or key touching a grounded electrical system. Having the current flow via a piece of metal, relative to through the skin will reduce the resistance close to the spark, allowing for a much faster ionization, thus a shorter rise time. The shorter rise time allows the charges on the metal part and on the hand surface to dominate the initial nanoseconds, thus, leading to a much higher peak current relative the human skin discharge.	Used to determine VI curves, destruction thresholds on IC and systems, and for susceptibility soft error scanning.
Qualification levels	1kV - 2kV	8 – 15 kV (contact)	8 – 15 kV (contact)
Environment	Production environment	User environment (system level) but the IEC 61000-4-2 waveform is also injected on to the IC pins directly to emulate the situation in which a charged person touches a pin of a connector in a system. The person is holding a piece of metal.	User environment (system level) but the IEC 61000-4-2 waveform is injected on to the IC pins directly
DUT condition	Powered OFF	Powered ON and OFF	TLP is a test method, not an ESD scenario
Pulse width	150 ns	0.8 ns +/- 25%	Typically 10-100 ns
Rise time	2-10 ns	0.8 ns +/- 25%	100- 500 ps
Peak current	0.7 A/kV	3.75 A/kV	The source impedances of TLPs vary from 50-300 Ohm. Most TLP systems are 50 Ohm systems
Equivalent circuit parameters	100 pF, 1500 Ω	150 pF, 330 Ω	

Correlation	No direct correlation with HMM because the test environments are different.	For the same current flowing into a low impedance DUT the HMM (330 Ω) and the TLP (50 Ω) voltages are directly related to their source impedances. Hence the ratio becomes $V_{HMM}/V_{TLP} \sim 6.6$. The rise time of most lower voltage (<3 kV) CDE ESD is faster than the 0.85 ns stated in the IEC 61000-4-2 standard. For devices that are sensitive to the rise time of the pulse, for example if the pulse is transduced by a small inductance between a shield and a connector shell, then correlation factors between 1...5 (TLP/HMM) are to be expected.
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Table 7.2: Comparison between HBM, HMM and TLP

7.1.3 Differences Between ISO 10605 and HMM:

Parameter	ISO 10605		HMM (IEC 61000-4-2)	
	Contact	Air	Contact	Air
Output Voltage	2- 15 kV	2 - 25 kV	2 - 8 kV	2 - 15kV
Interval Time	Minimum 1s		Minimum 1s	
Polarity at each stress voltage level	Positive and negative		Positive and negative	
Network Capacitance	150pF/ 330 pF		150 pF	
Network Resistance	330 Ω/ 200 Ω		330Ω	
Number of Discharge pulses	Minimum 3		Minimum 10	
ESD Generator Ground reference	Battery ground		Earth	
Test conditions	Unpowered/Powered with battery		Powered	

Table 7.3: Comparison between ISO 10605 and IEC 61000-4-2

7.1.4 Correlation:

Transmission line pulsing (TLP) has been widely used to characterize the ESD protection devices because of its simple setup and easy data interpretation. When using the TLP for predicting ESD passing levels, however, it is necessary to correlate the TLP data with results measured from the system level testing (HMM current pulse and transient fields). If the comparison is limited to current levels or to current rise times a correlation can be established. However, if transient field induced soft failures are also considered it will be too complex to create a correlation factor. Besides correlating HMM to TLP it is possible to correlate HMM to CDE (Cable Model). Here again one needs to limit the correlation to currents, avoiding the difficulty of describing the field creation and coupling which is fundamentally different between an ESD generator and a transmission line pulser.

There is a choice of parameters that can be chosen to compare different test methods. For example, if we consider the current into the DUT to be the same although two different types of ESD are used, different charge voltage need to be used. Thus, a current equivalent charge voltage correlation factor can be established. If the load impedance of the DUT is much lower than the source impedance a simple comparison of the approximate source impedances of the two ESD events will lead to such a correlation factor. The tables above show $V_{HMM}/V_{TLP} = 6.6$; $V_{HBM}/V_{HMM} = 4.5$, here a source impedance of the TLP of 50 Ohm was assumed. The test method proposed in section 8.1.2 uses a meandered line above ground having an impedance of about 180 Ohm, which would relate to 330 Ohm by a factor of 1.8.

Another way is to correlate is to calculate the stored energy associated with one particular ESD test (for example HMM). A charge voltage ratio having the same stored energy can be found. Here one has to be careful that the stored energy is related to the energy that is dissipated in the DUT by the source and the load impedance. During a transient event reflections occur, thus the analysis of the energy dissipated in a DUT requires detailed knowledge of the source, coupling path and load.

A more difficult comparison relates the energy dissipated in the victim. Usually, only a small portion of the electrostatically stored energy is dissipated in the victim. According to [4] a 2m long 50 ohm cable will dissipate the same energy in a 50 Ohm load as an 8kV HMM. The reason for the large difference lies in the impedance mismatch of the HMM and the cable discharge.

7.2 ESD Generator Models - Overview

The ESD generator simulation models in the literature can be broadly divided into SPICE-based network models and Maxwell-based models. The SPICE based models are based on KVL/KCL laws and models generally describe ESD by voltages and currents. The fields induced due to ESD discharge are not modeled, so transient field coupling effects cannot be obtained directly from using these models. Whereas, Maxwell-based models describe the physical geometry of the generator, and also may include lumped elements if it is reasonable to assume that the fields are confined in a small region. So by using the Maxwell-based models, the fields can also be obtained in addition to voltages and currents. The generator models can also be classified depending upon the discharge mode: as contact mode models and air-discharge models including a non-linear arc model.

The ESD generator models are needed to predict the currents and fields of the ESD simulator which can be used to calculate the coupling into the electronic system. Furthermore, the simulator design can be optimized and the effect of changes can be predicted. Also the behavior of the ESD protection devices and structures can be simulated and studied.

The broad classification of models from literature using the above criteria is as shown below.

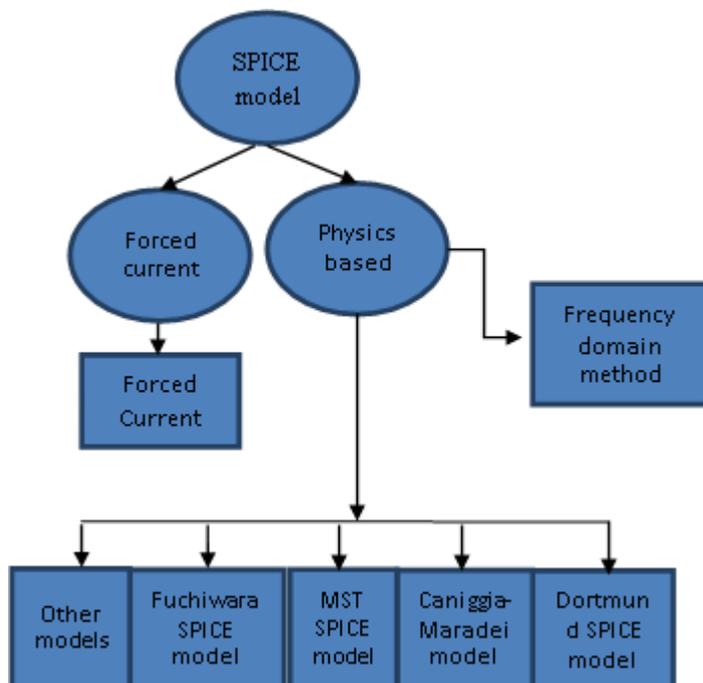


Figure 7.2: Classification of SPICE based ESD generator models

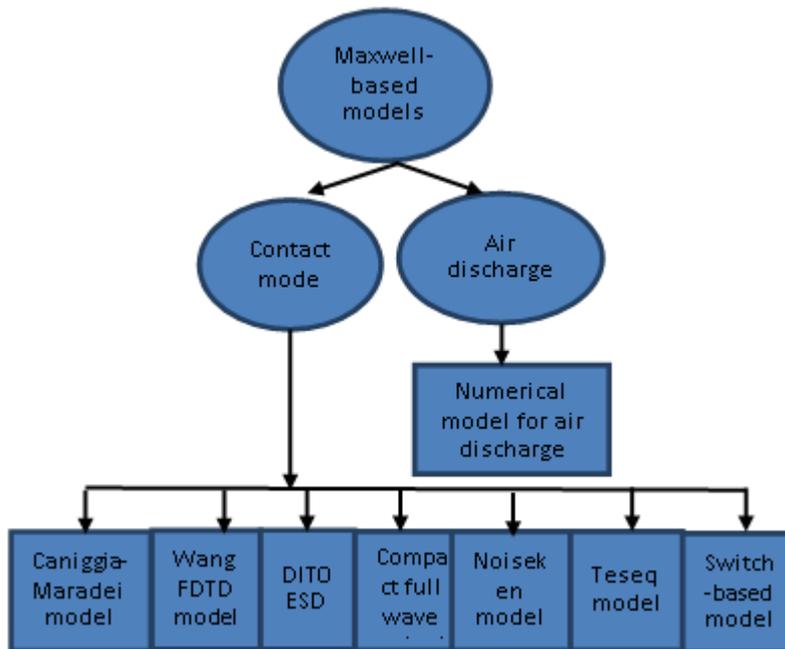


Figure 7.3: Classification of Full-wave ESD generator models

7.2.1 SPICE (KVL/KCL) Models

7.2.1.1 Forced Current Model (IEC 61000-4-2)

In this model the current waveform (taken from ESD standard) is forced from a current source into a target (contact mode). This model is acceptable for human metal discharge in a large ground plane. Other waveforms from the standard can also be used.

In this model the load and source impedances are not taken into account and fields can also not be simulated. If the load is just a small capacitance then the load will be charged up by the forced current to a voltage much higher than the ESD generator's charging voltage.

7.2.1.2 Caniggia-Maradei SPICE Model

The generator model somewhat reproduces a human-metal ESD. It models the discharge current in contact mode and takes into consideration load effect of generator. It is a lumped element equivalent circuit and can be easily implemented in any circuit simulator. The main limitation of the model is that the field cannot be simulated in the model. Also the inductance loop formed by ESD gun and metallic planes is too small and the ground strap modeled as transmission line is too short.

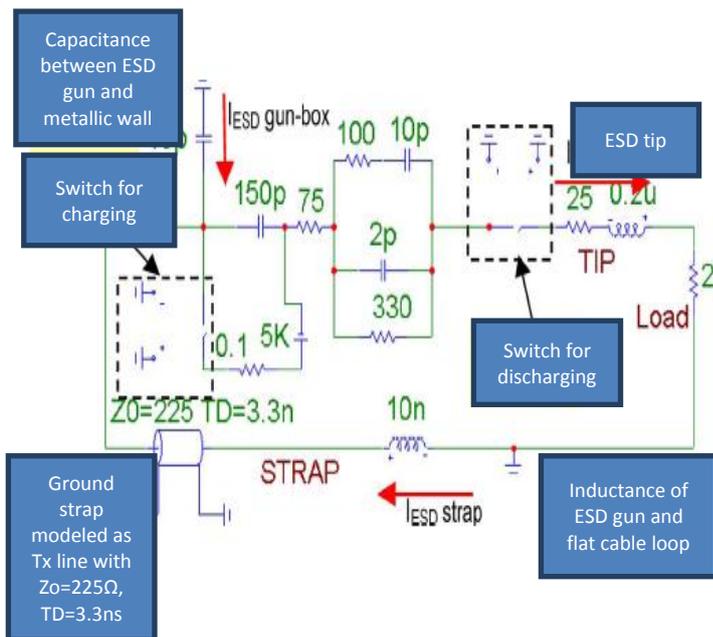


Figure 7.4: Caniggia-Maradei SPICE model

7.2.1.3 Tanaka-Fujiwara-Yamanaka SPICE Model

This model is used for simulating HMM discharge current in contact mode using an equivalent circuit. The current is calibrated by injecting it in to a Pellegrini target. The limitation of this model is that it cannot simulate the fields. Also the value of L for the model was used from the measured data as the actual geometry is not simulated. The arrangement of the structure of ESD gun with Pelligrini target and the numerical values of circuit parameters are as shown below.

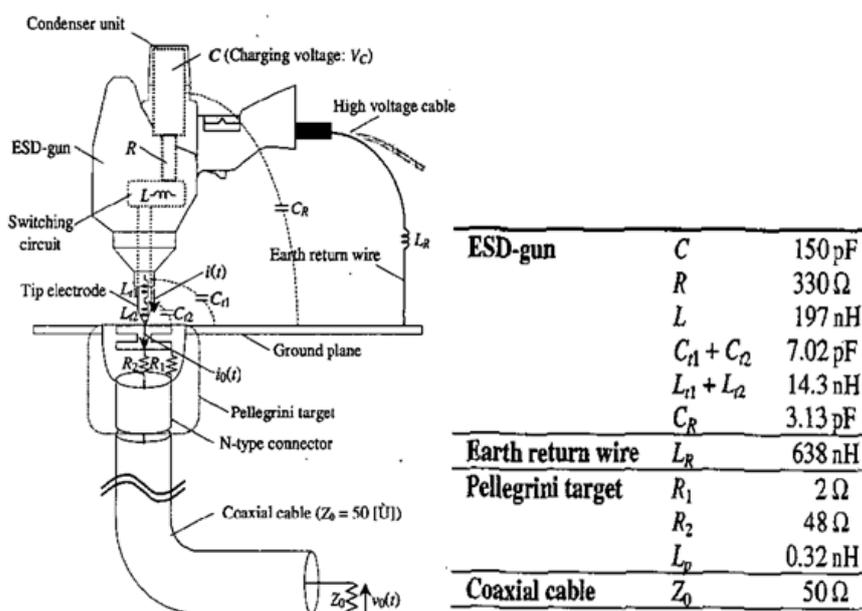


Figure 7.5: Structure of Pelligrini target and numerical values of circuit parameters

7.2.1.4 MST SPICE Model

The model developed at MST is applicable for simulating the HMM discharge in contact mode. It takes the effect of load impedance into account. The main limitation like other SPICE models is that it cannot model the fields associated.

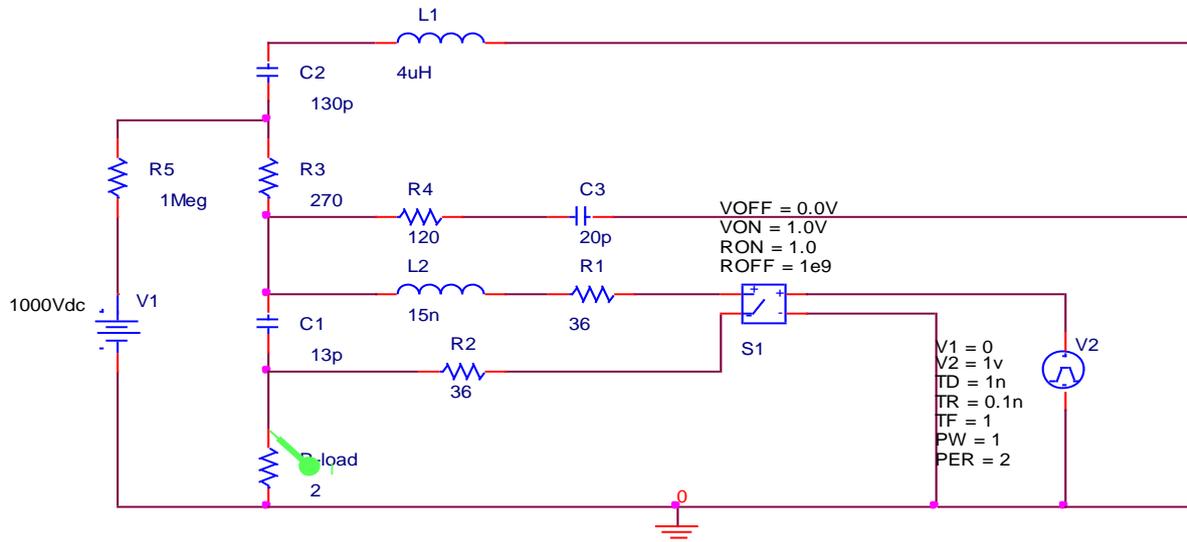


Figure 7.6: MST Spice model

7.2.1.5 Frequency Domain MST SPICE Model

It models the ESD generator discharge current and pulse forming network to correctly reproduce field components which are >1GHz in contact mode. The model is tested up to 2GHz. It uses a network analyzer in place of relay as the dynamic range of network analyzer is much larger than an oscilloscope. It can be used for simulation of contact mode only. The main limitation of the model is that it can model the current spread but not the TVS response.

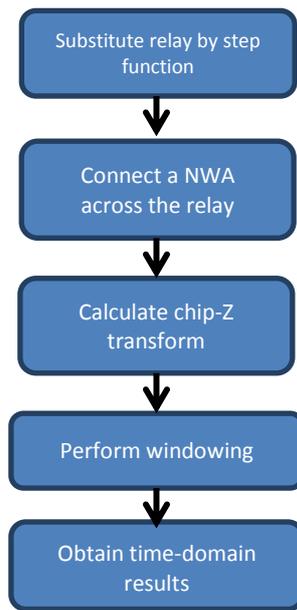


Figure 7.7: Method to obtain frequency domain model

7.2.2 Full Wave Models

7.2.2.1 Caniggia-MST-MWS Full-Wave Model

The Caniggia-MST-MWS model is a full wave model using Microwave Studio (MWS) based on finite-integration technique. The model was designed at MST in cooperation with Caniggia. It models the discharge current in contact mode and takes into account load effects of the generator. The model simulates the human-metal discharge using dielectric parts, metallic parts and lumped circuit elements. The model is applicable when the conducted and radiated interferences on a cable need to be considered. Figure below shows the lumped element network and port excitation.

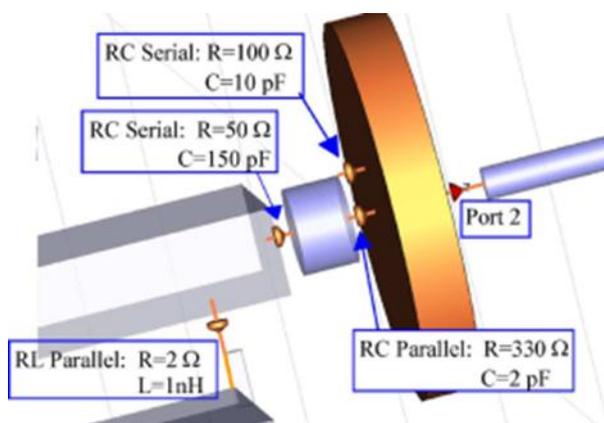


Figure 7.8: Lumped element network and port excitation

Model uses 1 ns step function as excitation with 300 MHz BW. Real ESD generators have higher frequency components which are created by the very rapid (< 100 ps)

voltage collapse within the relay which is then radiated from the metallic structure of the ESD generator. This is not modeled in the Caniggia model.

The results for the Caniggia model for the strap current and tip current are as shown below.

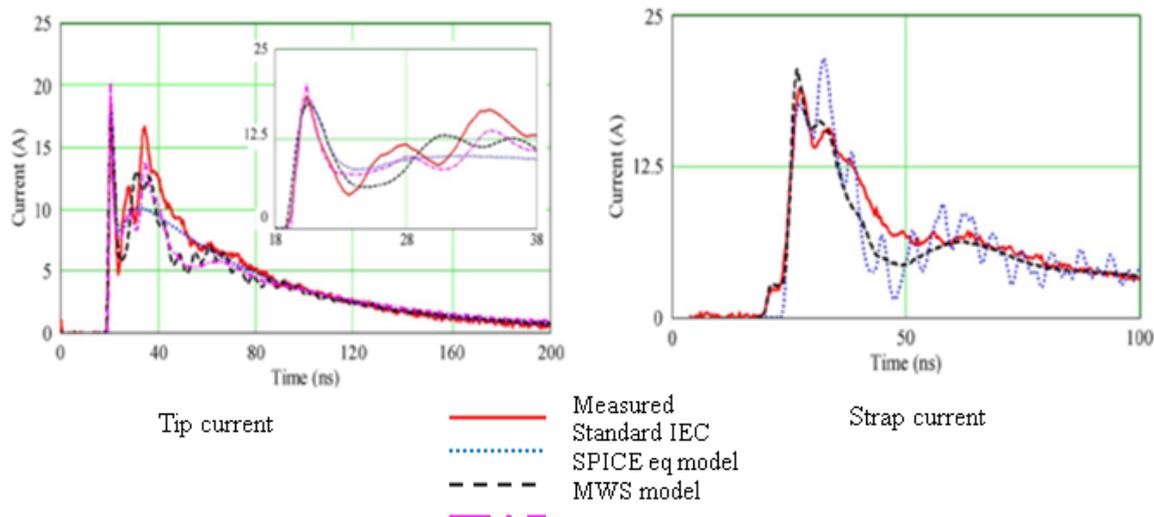


Figure 7.9: Caniggia-MST results for the strap current and tip current

7.2.2.2 Compact Full Wave Model

This compact full wave ESD generator model together with block model can be used to perform board level ESD simulation. It reduces the model size of a full wave model by using more lumped elements. This reduces the domain size but reduces the accuracy of field modeling.

The concept here is to model the general current densities at first, and then to use this as input for more detailed simulation of the voltages induced in electrical nets.

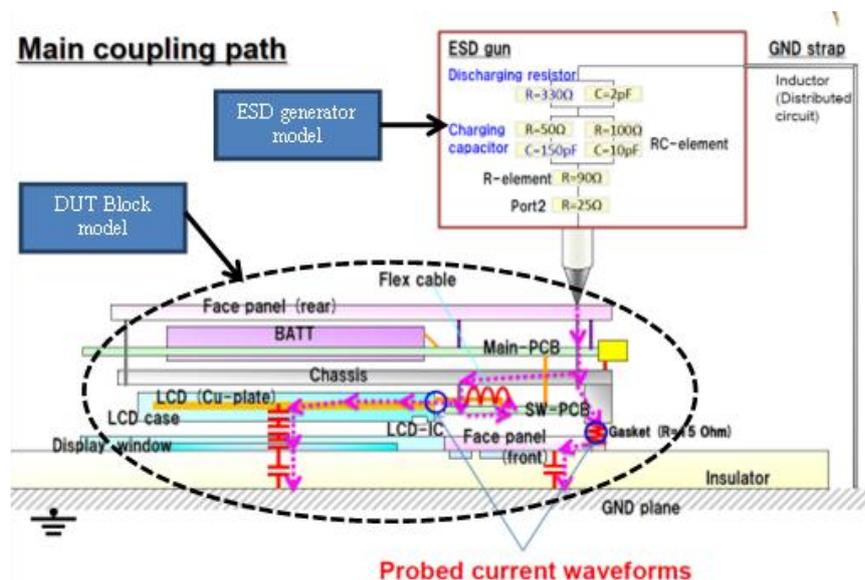


Figure 7.10: Compact full-wave model

7.2.2.3 Numerical Models Based on the FDTD Method

In this model the currents and fields are simulated using geometry and charge voltage in contact mode using FDTD. It models the physical geometry, the relay, pulse forming filter, ground strap and lumped elements.

The ability of the model to handle time-dependent materials allows accurate modeling of charging and discharging process. The model is evaluated up to 1 GHz.

The limitations are that the model does not simulate with any EUT and long calculation times. The structure of a model is shown below.

7.2.2.4 EM Test DITO ESD Generator Model

The DITO ESD generator model simulates discharge current and into a DUT in contact mode. It can also be used to determine the field coupling which can be used for soft-error prediction. It models the voltage source, LPF, main RC elements, discharge tip, ground strap and structural elements as blocks. The model is evaluated up to 2 GHz.

The model is mainly applicable to predict the current on a cable and voltage inside a small handheld device. The model does not simulate the second peak and the ringing of the current waveform quite well. Falling edge of the current in cable attached to handheld device is not well modeled.

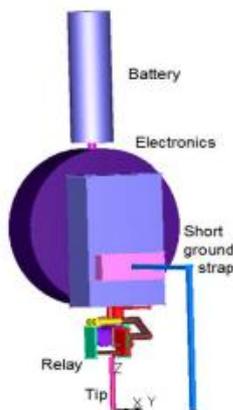


Figure 7.11: EM test DITO model

7.2.2.5 Noiseken ESD Generator Full Wave Model

This model simulates the discharge current and the transient EM field around the ESD generator and inside a product for a HM discharge in contact mode. The model works up to 3 GHz. It models the relay, capacitor, coil, ferrite rings and polyethylene disks of Noiseken ESD generator. The possible frequency dependence of Polyethylene disk is not taken into consideration.

This model is validated with respect to discharge current and induced loop voltage both in time and frequency domain. The full-wave model of the Noiseken generator is as shown below.

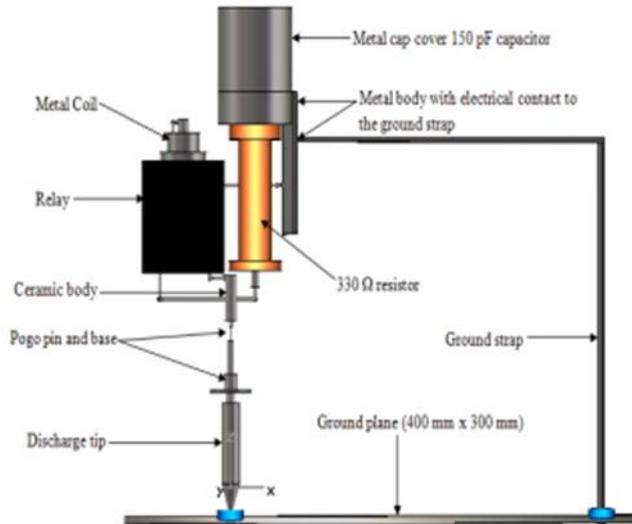


Figure 7.12: Noiseken model

7.2.2.6 Numerical Model for Air Discharge

The numerical model combines the arc model and Noiseken full wave model so that the currents and fields in air discharge mode can be simulated. It uses the Rompe and Weizel law to model the arc. The model is verified by simulating the discharge current into a ground plane and then discharge into a small product. It takes into account the effect of load impedance. The linear part of simulation is simulated in a full-wave simulation and nonlinear arc in SPICE.

The model is applicable for simulation of ESD to products and for simulating grounding conditions of products on the arc. The model can also be extended to perform secondary breakdown simulations. The model has a limited ability to simulate all physical details. Also it is difficult to provide arc length for arc length resistance calculation. Another limitation of the model is the stability of TD SPICE simulation.

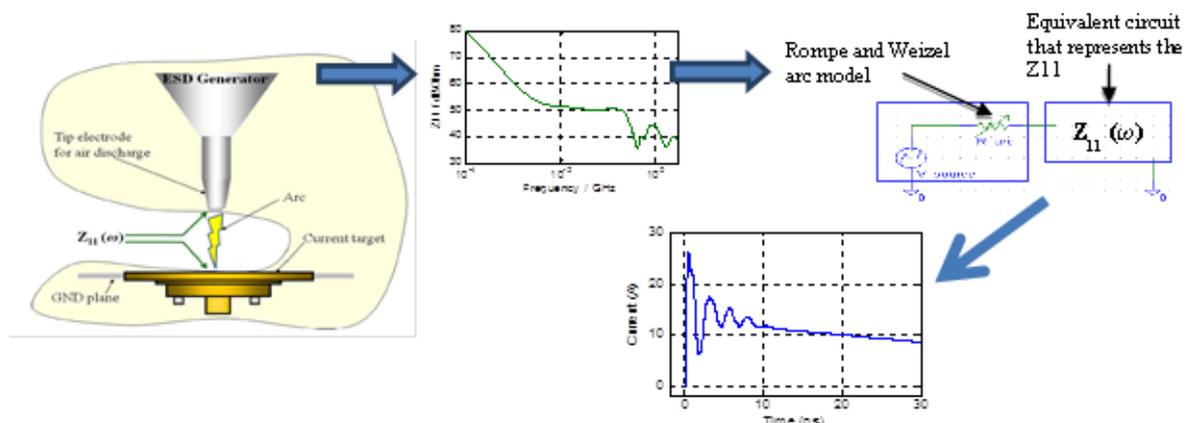


Figure 7.13: Method to model air discharge

7.2.2.7 Modeling of Teseq ESD Generator

It models the Teseq ESD generator NSG 438 as a full wave model with equivalent circuit of long ground strap, coil and ferrite. The model works up to 2 GHz.

The main advantage of the model is that due to equivalent elements the size of model is relatively small. The full-wave model of the Teseq generator is shown below.

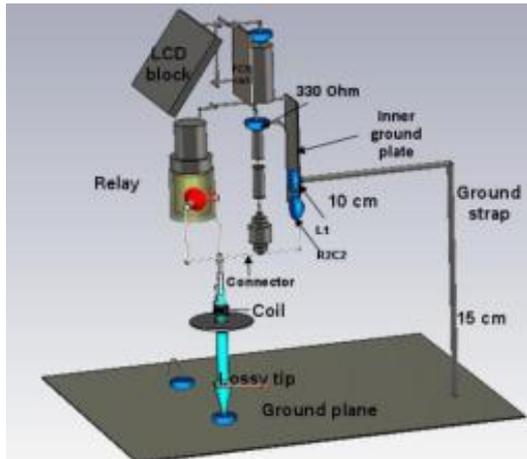


Figure 7.14: Teseq ESD generator model

7.2.2.8 Switch-Based Full Wave Model

The non-linear components are modeled as a switch. When the voltage over the switch is higher than the material breakthrough voltage, a breakthrough occurs with a defined channel resistance; else the switch remains in high impedance state.

The method can be modified by using the numerical values of measured currents and voltages to characterize material with dynamic breakthrough resistance. The model can also be potentially used to find potential breakthrough locations from 3-D CAD files. An assembled ESD material characterization tester is as shown below.

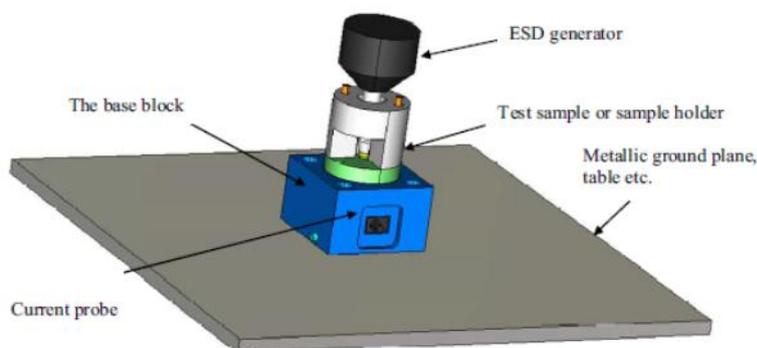


Figure 7.15: Assembled ESD material characterization tester

7.2.2.9 Secondary ESD Discharge Model

A hybrid method to model the secondary discharge has been implemented combining the full-wave simulation and circuit simulation with a non-linear spark-arc model. The S-parameters obtained from the full-wave model are transformed into equivalent circuit in SPICE and combined with the SPICE spark-arc model. The model has been extended to include the statistical time lag and the breakdown voltage threshold.

The arc resistance drops rapidly in a short time, so there might be convergence issues with the SPICE simulation. The model is mainly applicable to predict the currents and secondary discharge in portable products

Several well-functioning ESD generator models have been published. For current/voltage simulation, SPICE based models are suitable. For simulation of fields, full wave models are suitable. For air discharge mode, using full wave model port impedance is calculated. Then it is combined with arc model in time domain and the resulting current is used as an excitation source in Full wave to determine fields. Secondary discharge can be modeled similarly to air discharge, but the models are more complicated. Details of this investigation can be found in [81].

7.3 ESD Generator Models - Used in this Project

Different standardized pulse generators are used to specify the ESD robustness of electronic systems on component and system level. The models of HBM, IEC and TLP pulse generators are described in the following sections.

7.3.1 HBM Model

The Human Body Model (HBM) is traditionally used for basic ESD-characterization of integrated circuits. The waveform is defined e.g. in the non-automotive JEDEC JESD22-A114F standard [35]. In [36] a proposal for a HBM generator model is described. The equivalent circuit is shown in Figure 7.16. Differing from the literature approach the inductor L_s has been changed to 5 μH .

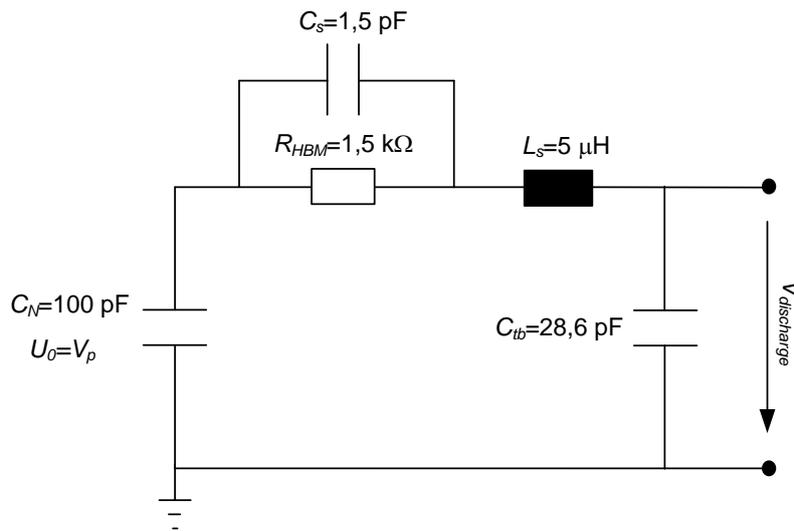


Figure 7.16: General equivalent circuit of basic HBM generator model

For waveform verification the currents flowing through a 500 Ω resistor and shorted circuit is measured. The simulated discharge of the HBM model through a 1 Ω resistor is shown in Figure 7.17.

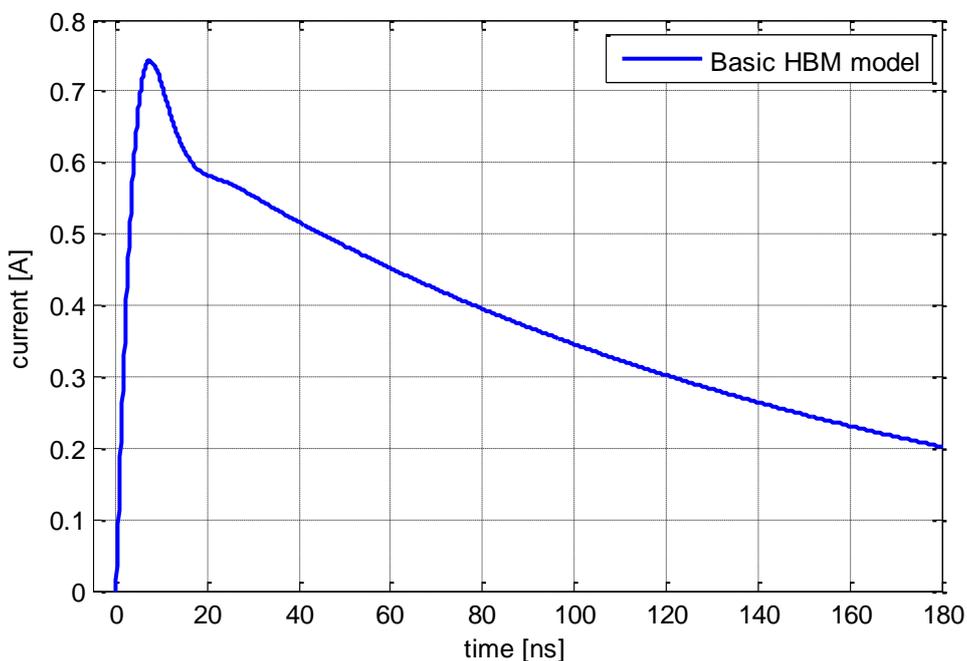


Figure 7.17: Discharge of basic HBM generator model with 1 Ω load and 1 kV charging voltage

For verification with the short circuit load a pulse rise time of 2-10 ns and peak amplitude of 0,6 to 0,74 A is required if the capacitor is charged with 1000 V.

According to the standard a rise time of 5-25 ns and peak current amplitude of 0,37 to 0,55 A has to be measured for the same charging voltage if the generator is connected to 500 Ω. The simulated waveform is shown in Figure 7.18.

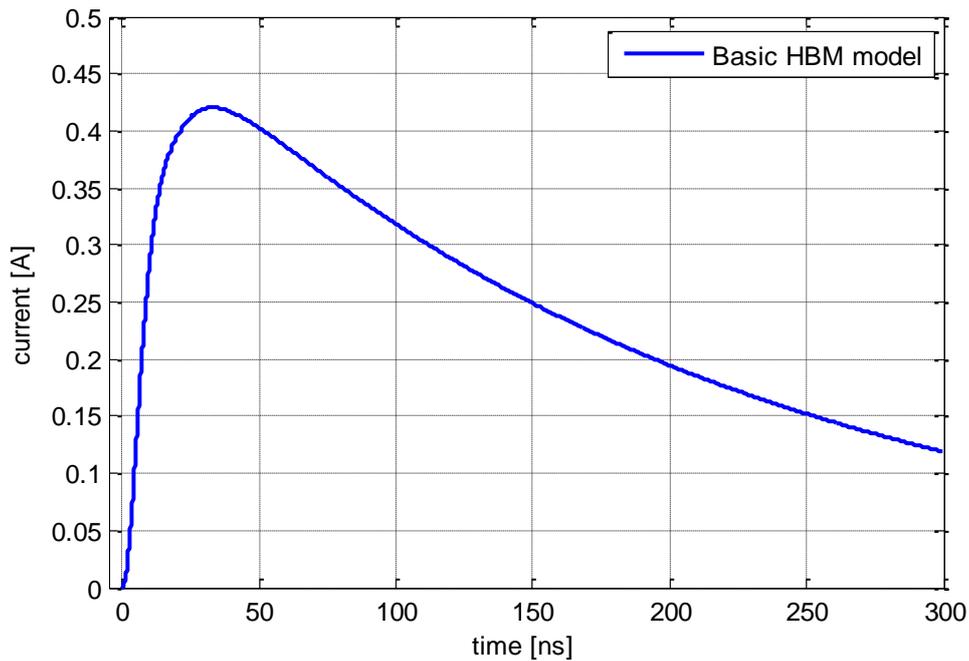


Figure 7.18: Discharge of basic HBM generator model with 500 Ω load and 1 kV charging voltage

7.3.2 Basic IEC Generator Model

As a general approach the current waveform which is specified in to the standards IEC 61000-4-2 and ISO 10605 [4][5] and can be simulated by two parallel R, L, C circuits with charged capacitors. The general equivalent circuit is shown in Figure 7.19. Here the standardized network elements of the ESD-generator are represented by R_1 and C_1 . The inductor L_1 is considered to be the obligatory ground strap with the length of about 2 m.

Physically the first peak of the pulse is shaped by additional lumped and parasitic elements around and in the tip of the ESD-generator.

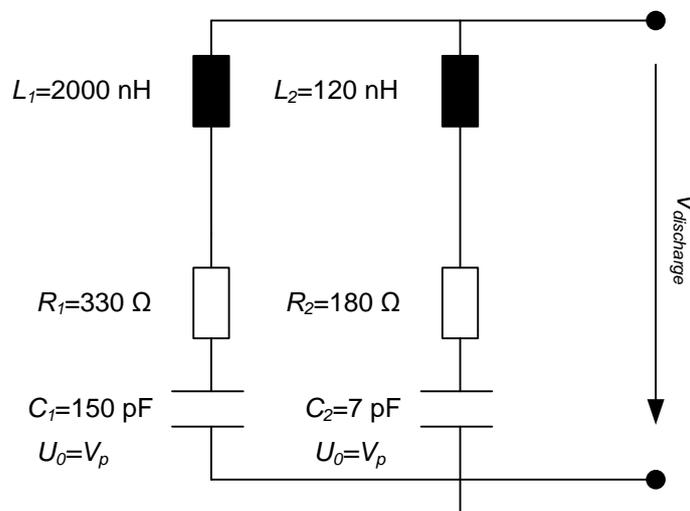


Figure 7.19: General equivalent circuit of basic ESD-generator model

According to the IEC 61000-4-2 standard the current waveform has to be verified with a low ohmic current sensor. The resulting current shape is shown in Figure 7.20. The first peak and accurate rise-time can be seen in detail in Figure 7.21.

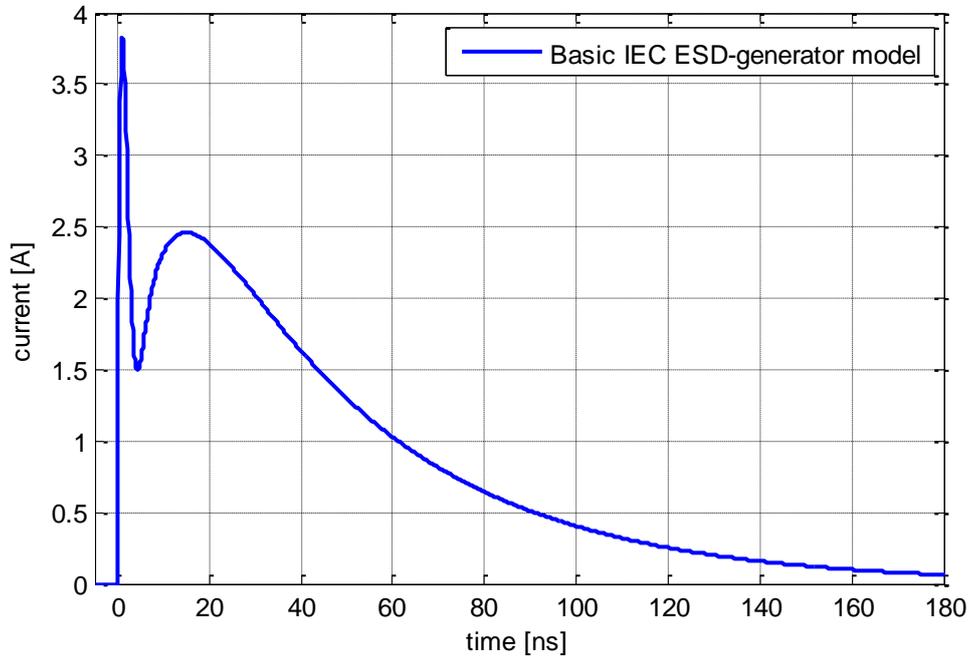


Figure 7.20: Discharge of basic IEC ESD-generator model at 2 Ω load with 1 kV charging voltage

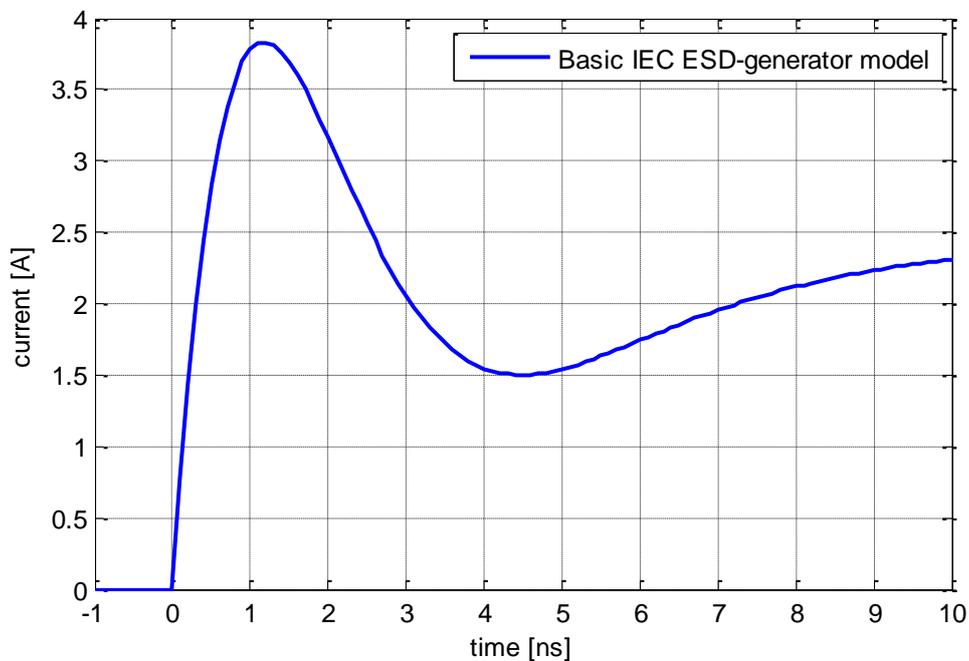


Figure 7.21: First peak current of basic IEC ESD-generator model at 2 Ω load with 1 kV charging voltage

7.3.3 IEC NoiseKen Model

An advanced circuit simulating the discharge of a NoiseKen IEC generator is given in Figure 7.22. The model has been verified by measurement on different low and high-ohmic loads. More detailed information can be found in [37] and [38].

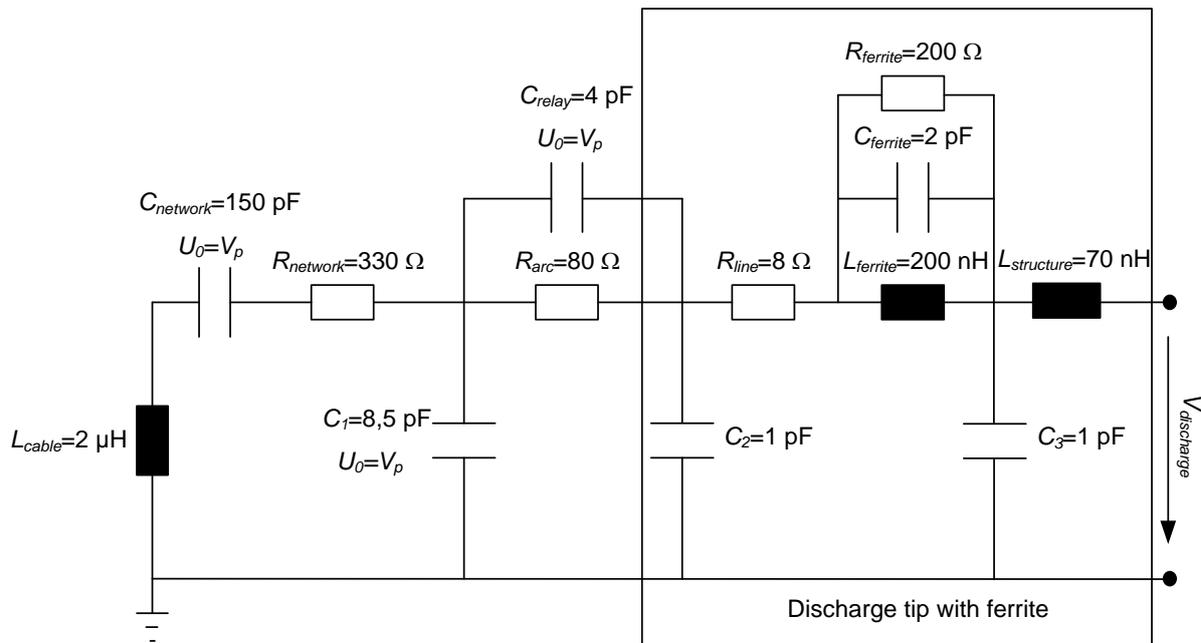


Figure 7.22: General equivalent circuit of NoiseKen ESD-generator

The resulting current shape is shown in Figure 7.23. The first peak and accurate rise-time can be seen in detail in Figure 7.24.

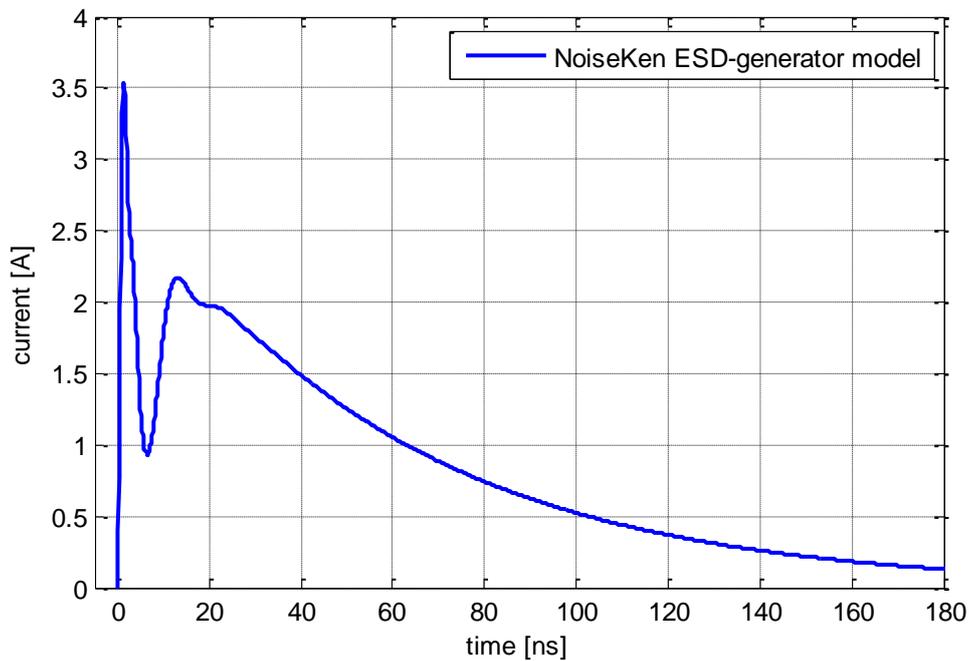


Figure 7.23: Discharge of NoiseKen ESD-generator model with 2 Ω load and 1 kV charging voltage

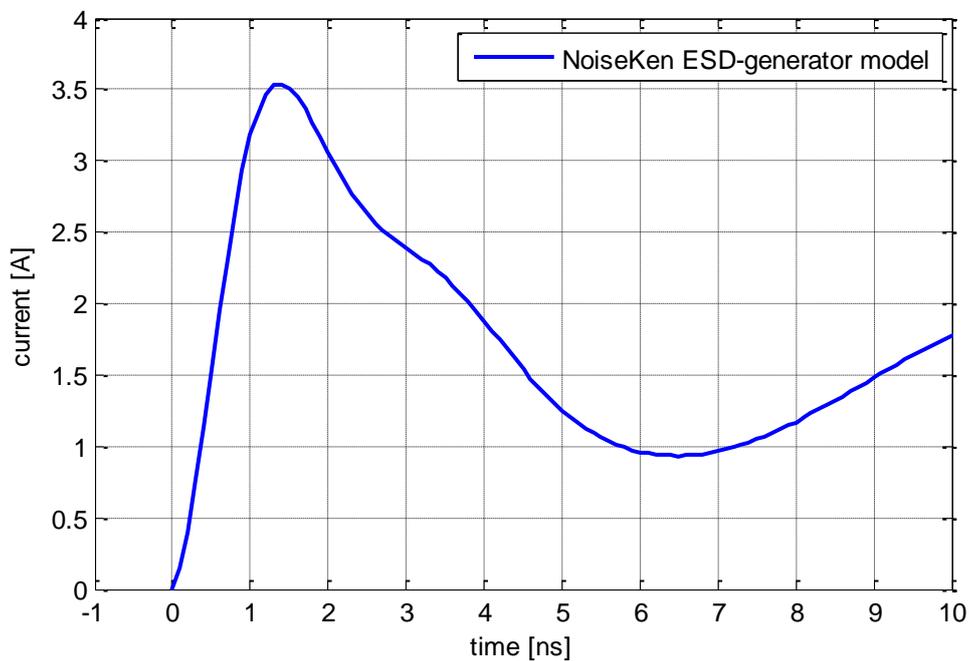


Figure 7.24: First peak current of NoiseKen ESD-generator model with 2 Ω load and 1 kV charging voltage

7.3.4 TLP Model

A transmission line pulser (TLP) can be used for high power characterization of ICs. In some approaches the TLP can also be applied as testing device for ESD

robustness. To achieve reliable simulation results an exact modeling of the TLP is required. In comparison to the modeling of ESD-generators, some components of the used TLP [39] can be directly mapped to model components. A part of the equivalent circuit is shown in Figure 7.25. The model has been verified by measurement on different low and high-ohmic loads. More information can be found in [40].

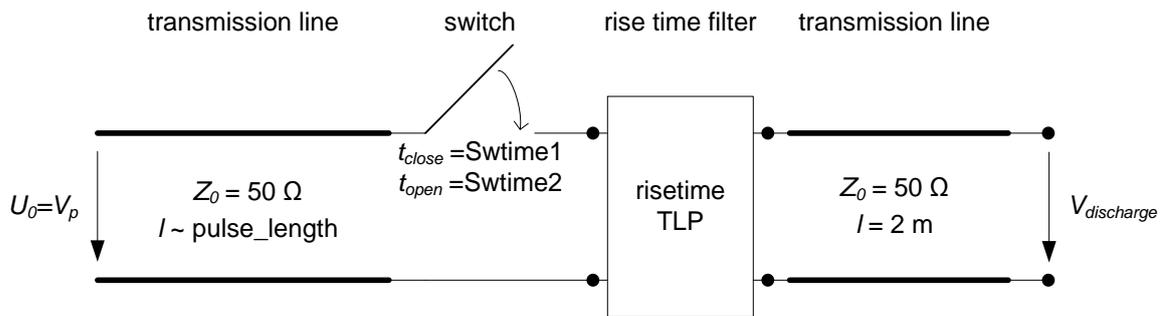


Figure 7.25: Diagram of TLP model

The pulse amplitude and the pulse length are mainly affected by the first transmission line. For simulation a lossless VHDL-AMS transmission line model is used, where the line charge V_p can be set as an initial condition. The pulse length is adjusted defining the length of the charged line according to the following equation:

$$length = \frac{pulse_length}{10 \text{ ns}} \quad 2$$

The wave impedance Z_0 is set to 50Ω . The propagation velocity of the line is set to $v_0 \approx 2,0 \cdot 10^8 \text{ m/s}$.

The line is discharged via a relay which is considered to be an ideal switch. The rising and falling edges can be controlled by the connected rise time filter. A detailed description can be found in [41]. Three different rise times (1,2 ns, 2,0 ns or 5,0 ns) are implemented.

Finally the pulse propagates through a second 50Ω transmission line to the DUT. In this case a VHDL-AMS model including losses is used to improve the accuracy of the simulated pulse shapes.

The model impedance mainly is determined by the rise time filter and the wave impedance of the transmission lines. Simulated current and voltage shapes are shown in Figure 7.26 and Figure 7.27 for a charging voltage of 1000 V and a 1,2 ns rise time filter.

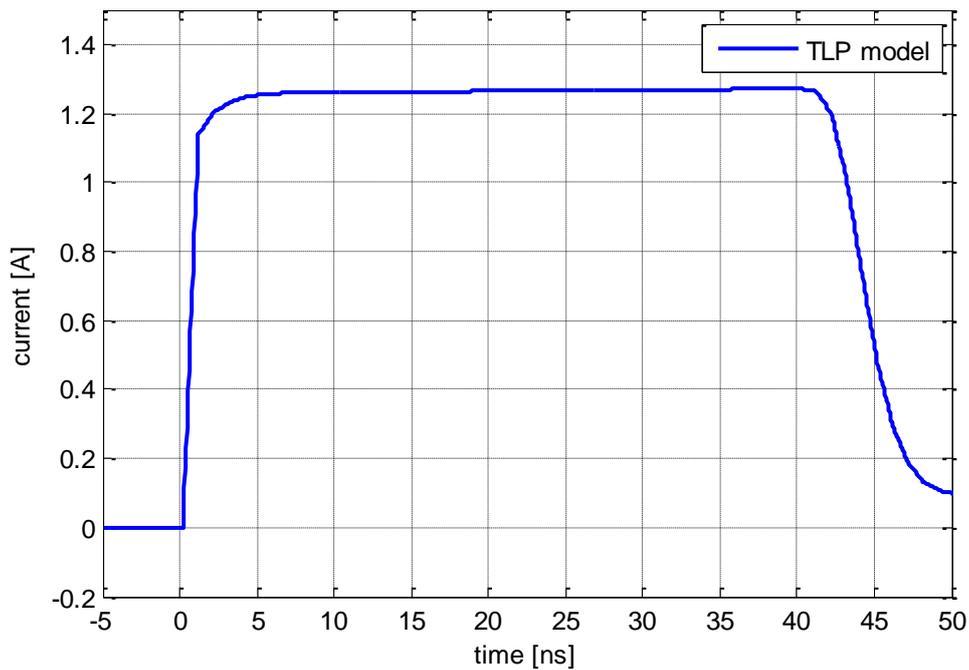


Figure 7.26: Simulated current of discharge of the TLP model into 50Ω with 40 ns pulse width, 1,2 ns rise time and 1 kV charging voltage

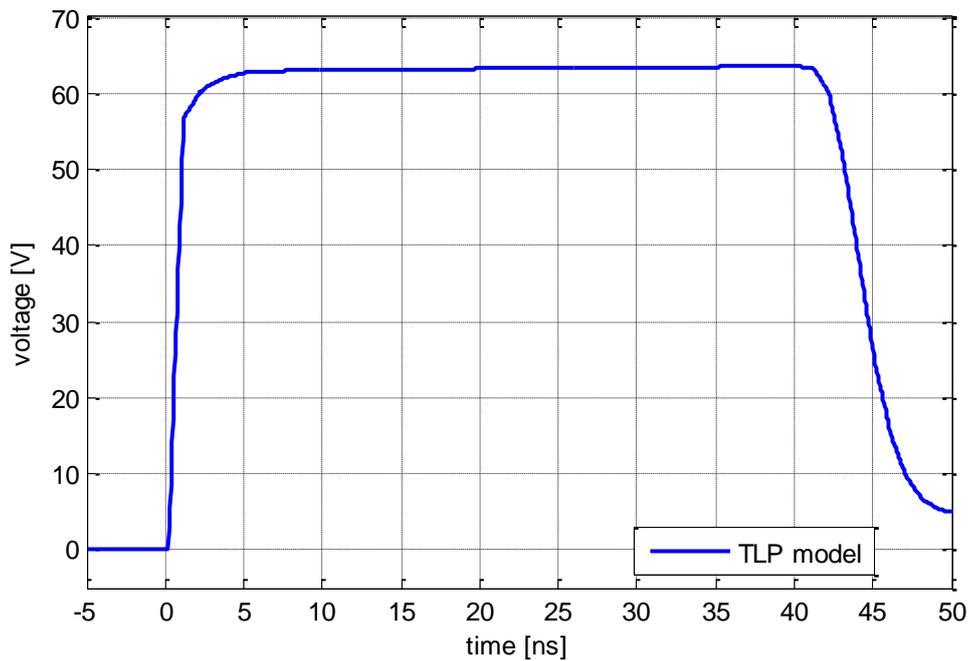


Figure 7.27: Simulated voltage of discharge of the TLP model into 50Ω with 40 ns pulse width, 1,2 ns rise time and 1 kV charging voltage

7.4 Multi Conductor Transmission Line Model

The transmission line models used for simulation of PCB structures and parallel conductors are described in this section. Multi conductor transmission line models can be applied for cross-talk simulation on PCBs. Detailed information on used

models can be found in [42]. The simulation of coupling effects is verified by a comparison to full wave simulation results. Figure 7.28 shows the equivalent circuit with two parallel conductors of equal length. A source is connected to one end of line 1. All wire endings are terminated with a 1 kΩ resistor. The source impedance is set to 50 Ω.

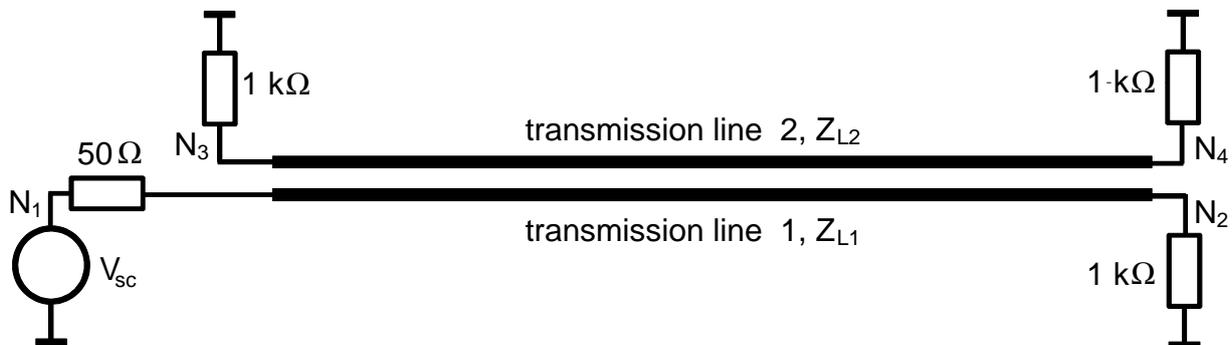


Figure 7.28: Setup for verification of transmission line models

In Figure 7.29 the 3D full-wave model is shown. Probes were set at nodes N₁, N₂, N₃ and N₄ as indicated in Figure 7.28. The distance between lines is 3 mm. The length of the conductors with radius 0,3 mm is 0,2 m and height above coupling plane is 3 mm.

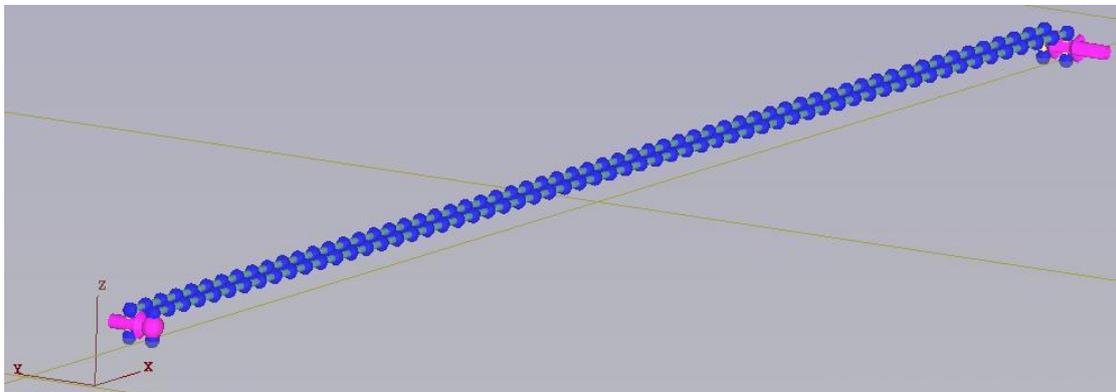


Figure 7.29: Full wave 3D simulation of transmission lines

The common mode and differential mode impedances of the transmission line configuration are extracted from the full wave model so that a similar setup can be implemented in VHDL-AMS concerning equal conductor lengths, transfer impedances and loads. Line parameters matrices are defined by the relation of the geometric configurations between transmission line 1, transmission line 2 and ground potential. The impedances can be calculated from L and C matrices. Detailed information can be found in [43].

$$L = \begin{bmatrix} 7.423e-07 & 2.819e-07 \\ 2.819e-07 & 7.422e-07 \end{bmatrix} \text{H}$$

$$C = \begin{bmatrix} 1.751e-11 & -6.653e-12 \\ -6.653e-12 & 1.752e-11 \end{bmatrix} \text{F}$$

The matrices are converted to modal parameters using transformation matrix T.

$$T = \frac{1}{\sqrt{2}} \cdot \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$L_{\text{modal}} = T^{-1} \times L \times T$$

$$C_{\text{modal}} = T^{-1} \times C \times T$$

The modal values are used to calculate the modal impedance matrix Z_{modal} .

$$Z_{\text{modal}} = \sqrt{\frac{L_{\text{modal}}}{C_{\text{modal}}}}$$

The first element on the main diagonal of Z_{modal} represents Z_{even} and the second element Z_{odd} . Common mode and differential mode impedances are calculated using the following relations.

$$Z_{\text{com}} = \frac{1}{2} \cdot Z_{\text{even}}$$

$$Z_{\text{diff}} = 2 \cdot Z_{\text{odd}}$$

The values for Z_{com} and Z_{diff} for the given configuration were found and can be used as parameters in the VHDL-AMS model.

$$Z_{\text{com}} = 153,5 \, \Omega$$

$$Z_{\text{diff}} = 276,0 \, \Omega$$

The results of both simulations are compared in Figure 7.30 and Figure 7.31 in frequency domain. Very small deviations of around 1 % between the curves of full-wave and VHDL-AMS simulation results can be seen only at resonance frequencies.

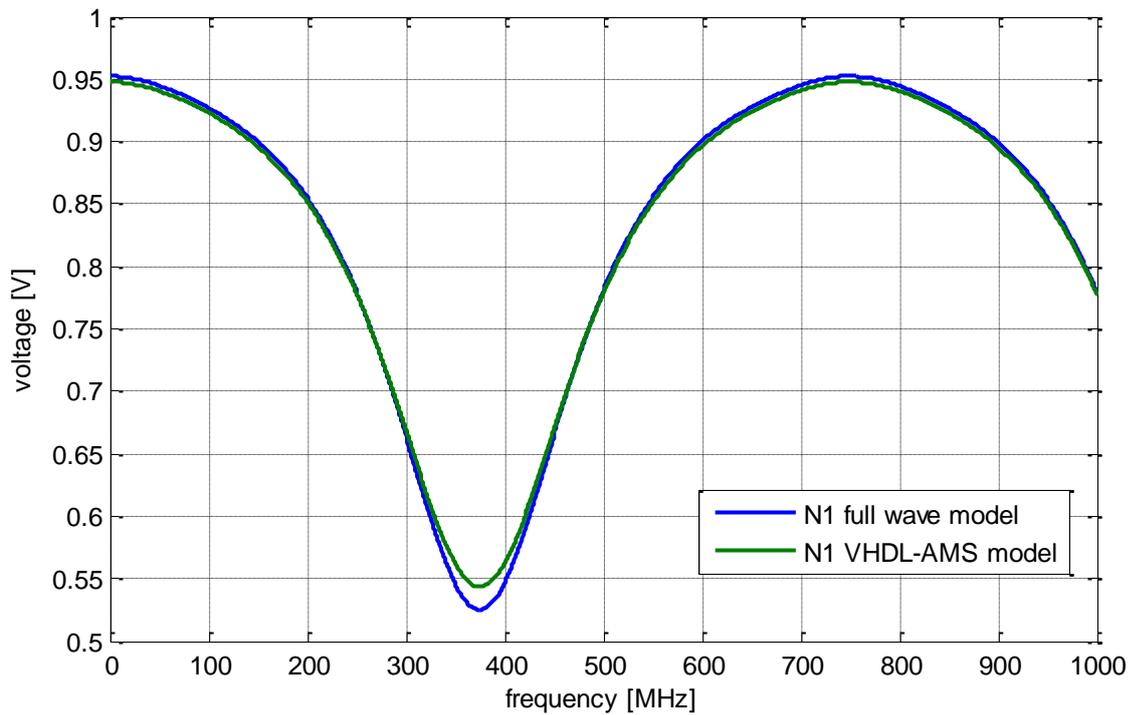


Figure 7.30: Comparison of VHDL-AMS and full wave simulation in frequency domain at node 1

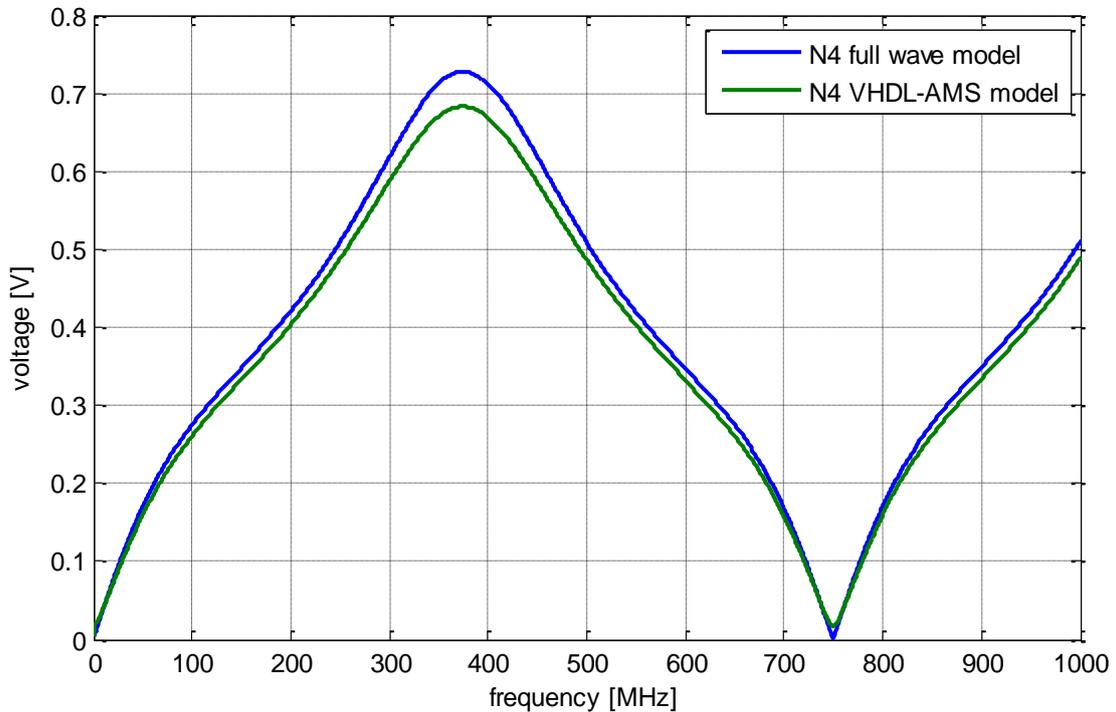


Figure 7.31: Comparison of VHDL-AMS and full wave simulation in frequency domain at node 4

In Figure 7.32 simulated waveforms are compared for a rectangular pulse with amplitude of 1000 V in time domain. Shown deviations are mainly caused by numerical problems of IFFT-algorithm of full wave solver.

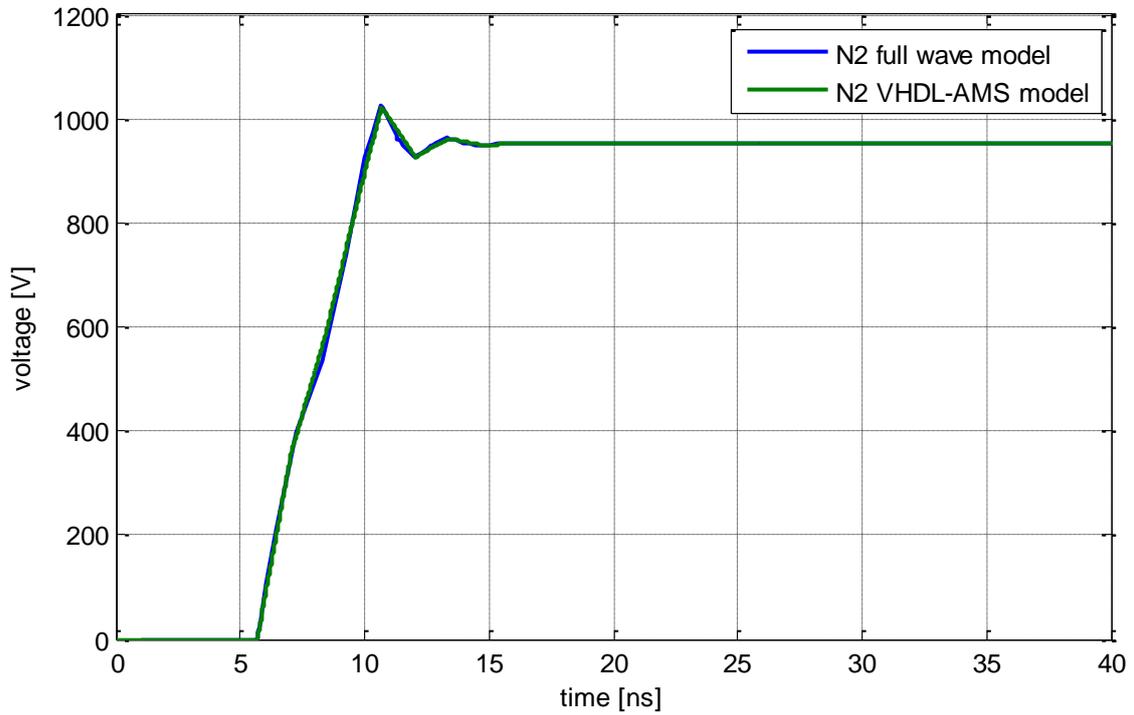


Figure 7.32: Comparison of full wave and VHDL-AMS model in time domain at node 2

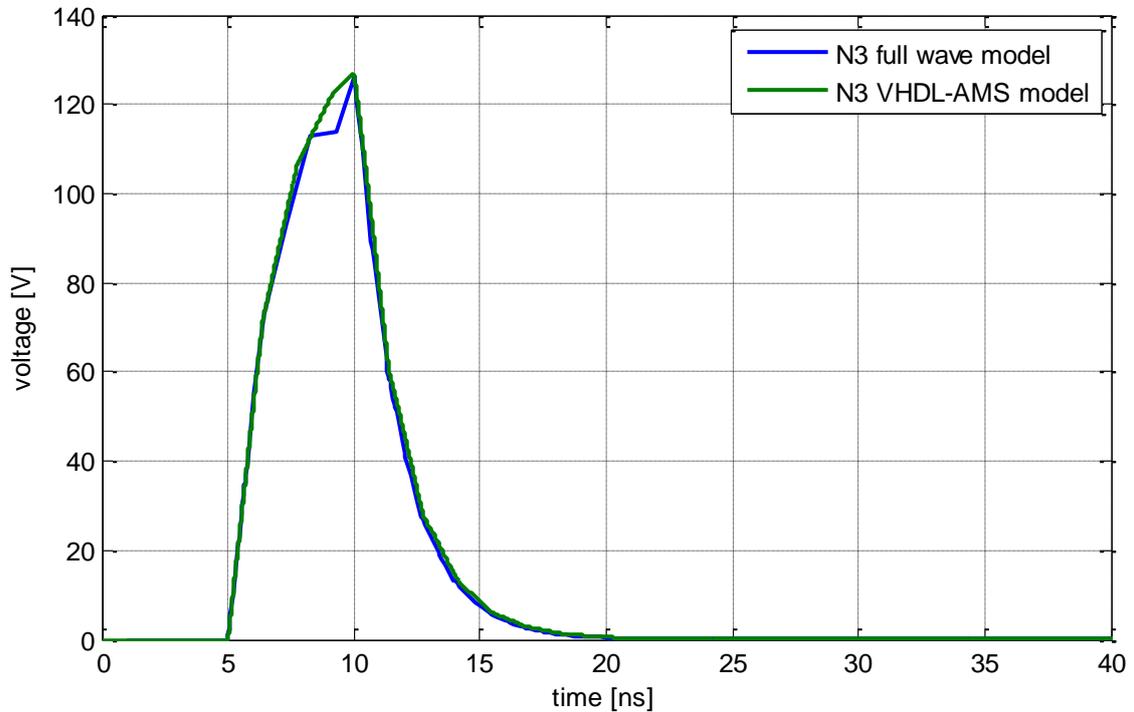


Figure 7.33: Comparison of full wave and VHDL-AMS model in time domain at node 3

7.5 Modeling of Field Coupling into a Transmission Line

The immunity of DUTs to ESD field coupling can be tested using an ESD generator which is discharged on a coupling plane. Similar to system level ESD tests, performed in direct contact discharge mode, indirect ESD immunity can be classified in terms of charging voltage and position of the ESD generator. Due to a long cable harness used in automotive ESD testing on system level and a short distance between the cable harness and the ESD event, strong coupling occurs, causing high voltage and current spikes which are conducted to the DUT. Calculation of coupling voltage and current of an indirect ESD event in cables mostly is required only at the end where the device is connected.

In [45] an impedance measurement method for ESD generator modeling was introduced. The current, flowing through the discharge tip, can be calculated if the transfer behavior between the points, where the voltage drop occurs, and the point of discharge is known. In [45] an ESD generator model is extended by a coupling structure represented by a single cable. This model can be used for discharge investigations into load models. The model represents the individual characteristics of the measured ESD generator without using complex 3D simulation and allows computation of field coupling by SPICE or VHDL-AMS circuit simulators.

For model generation measured n-port S-parameters are approximated to polynomials by using vector fitting algorithms [46]. The mathematical expressions can be transferred to state space representation and implemented for the use in circuit simulation tools like SPICE or VHDL-AMS. The model provides as many ports as measured with the Vector Network Analyzer (VNA).

For investigating possible disturbances of circuits by ESD coupling a 3-port ESD generator model for direct discharge and field coupling was created. In the setup shown in Figure 7.34 an ESD generator is discharged on a coupling plane. The current will be distributed from the excitation source represented by port 1. Port 2 is connected to the discharge tip and represents the direct contact discharge into the plane. The 3rd port allows simulation of an indirect ESD coupling into a transmission line of 1 m length which is located 3 cm above the ground plane. For measurement the cable is fixed between two metal angles with good connection to the ground plane. The ESD generator is discharged at distance of 3 cm from the cable and at half of the overall cable length so that there is 50 cm left to each end of the line.

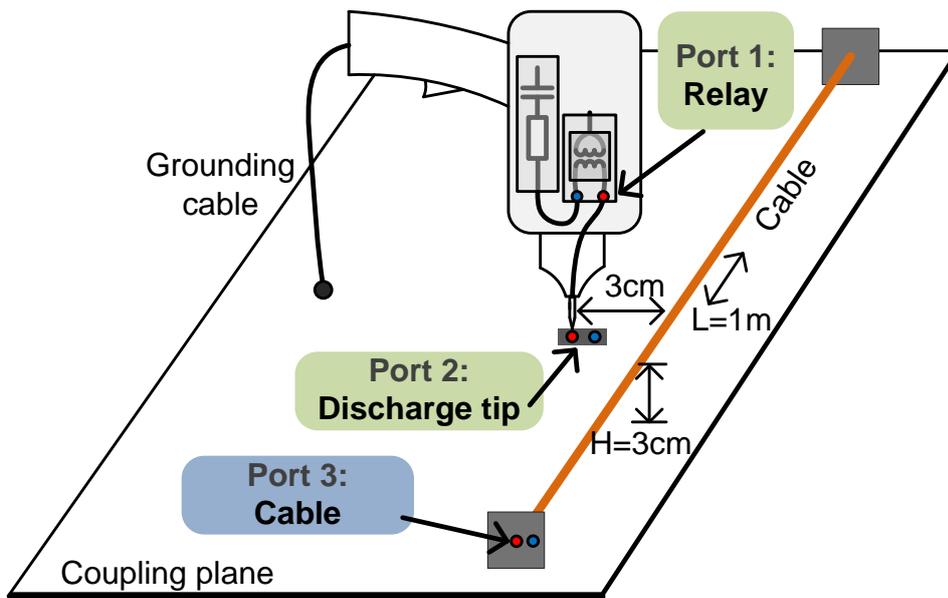


Figure 7.34: ESD generator model for direct discharge and coupling to cable

The model allows simulation of indirect ESD for arbitrary component models connected to the 3rd port if the other end of the transmission line is terminated by 50Ω . Method can be easily extended to non 50Ω terminations.

The accuracy of the model is verified by measurement in time domain. The ESD generator is discharged at the modeled position as shown in Figure 7.34. The discharge current and the coupling current were measured according to Figure 7.35.

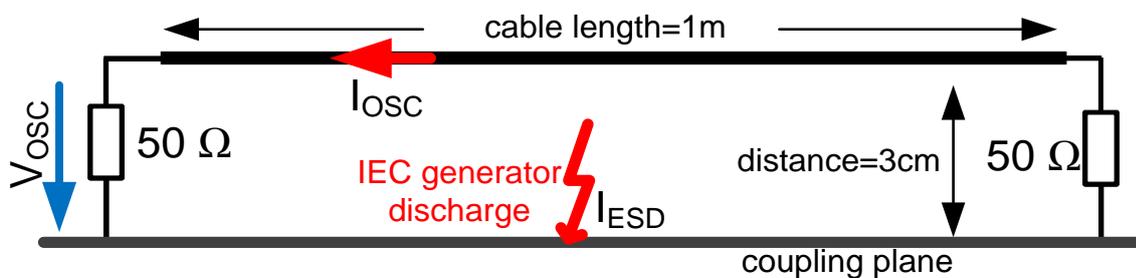


Figure 7.35: Measurement setup with 50Ω termination of the cable

The ESD generator model is excited at port 1 representing the relay blades. The simulated time domain response at port 2 is shown in Figure 7.36 for a discharge into 50Ω resistor and charging voltage 30 V and is compared to an oscilloscope (6 GHz bandwidth) measurement.

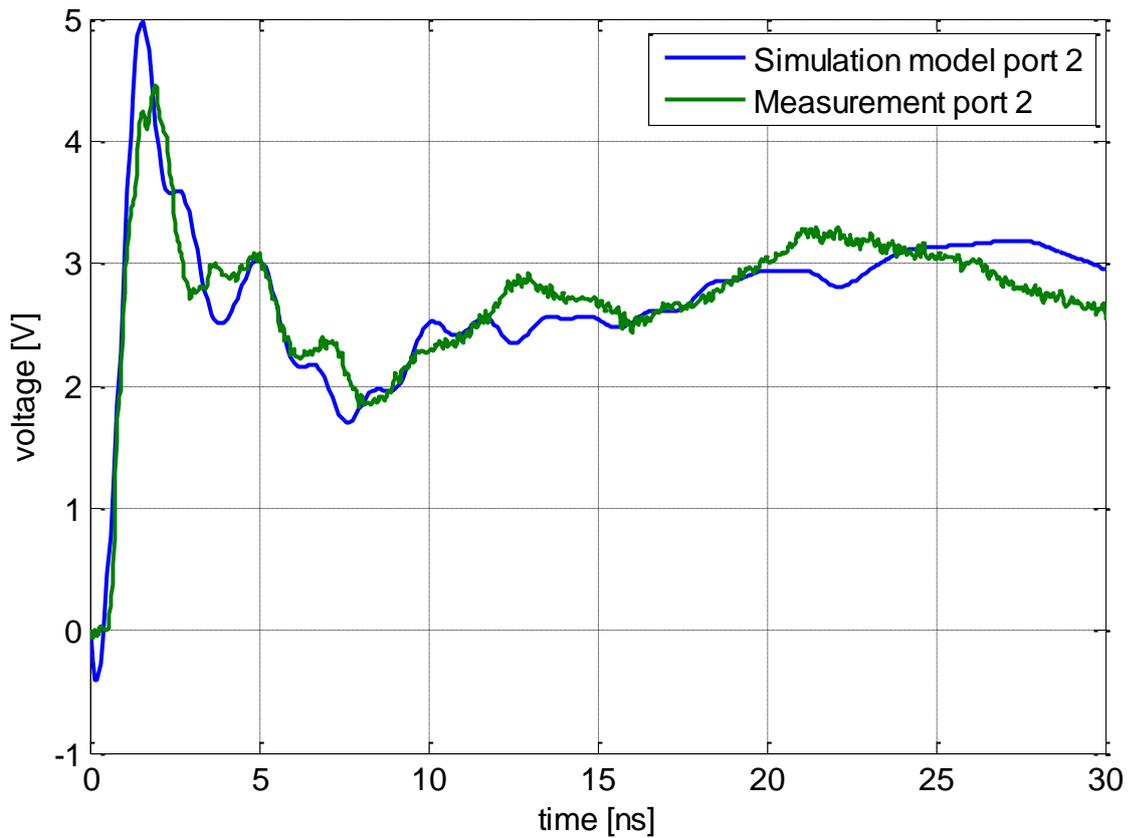


Figure 7.36: Measurement and simulation of ESD generator contact discharge current into 50 Ω

In Figure 7.37 the simulated voltage at port 3 is compared to an oscilloscope measurement (6 GHz bandwidth). In the setup the transmission line, which is situated at 3 cm from the discharge point, is terminated by a 50 Ω resistor at one end and by the 50 Ω internal impedance of the oscilloscope at the other end. The charging voltage of the ESD generator was set to 30 V.

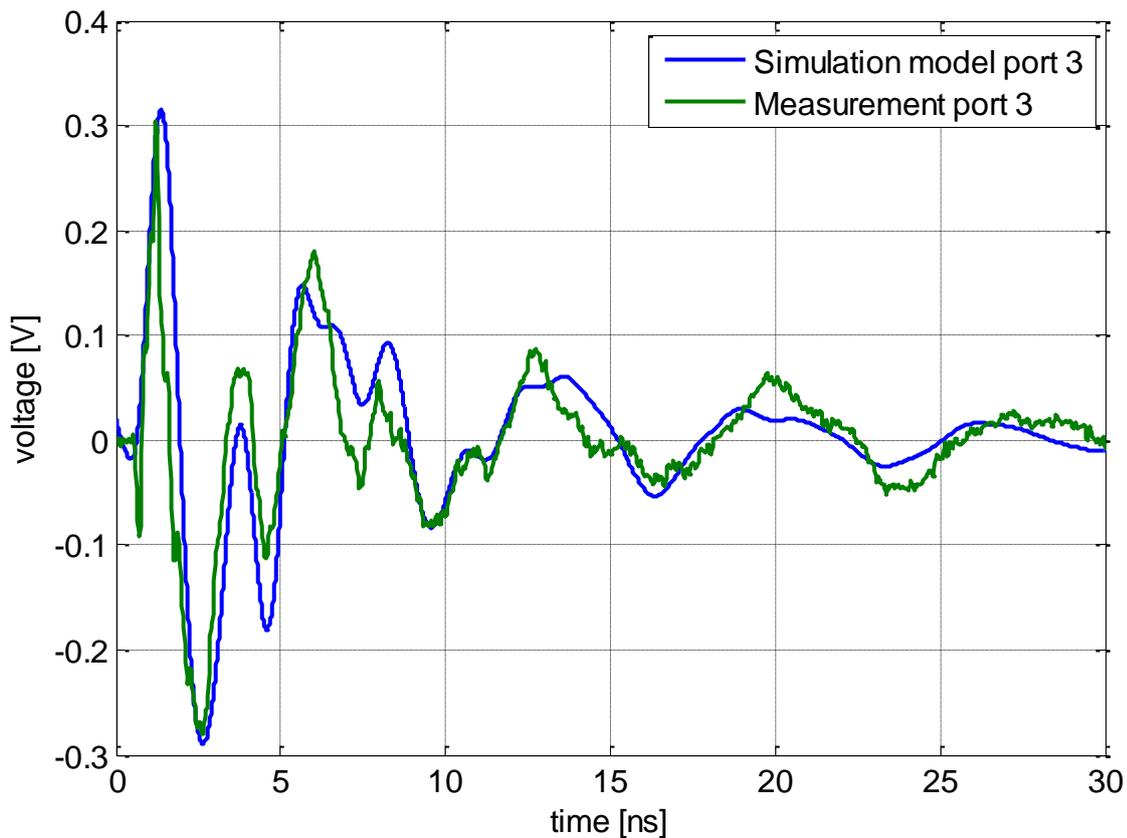


Figure 7.37: Measurement and simulation of ESD coupling current for cable with 50 Ω load

Results for other measured and simulated load configurations can be found in [45]. The model is linear and can be scaled for any charging voltage [44].

7.6 Destruction-IC-Model

A technique for ESD-failure modeling of IC structures is described in this section. More information can be found in [47]. In section 7.6.1 a general approach for modeling the static and dynamic electrical behavior of unpowered ICs-pins is explained. The general technique is limited to the electrical domain. A second approach focuses on the modeling of the thermal ESD robustness of ICs which is described in section 7.6.2.

The modeling approach is based on a pragmatic behavioral modeling technique without any information about IC internals such as geometry of package, physical characteristics, and so on.

7.6.1 General Modeling Approach for Electrical Domain

For model characterization data has to be measured. The IV-characteristic of a device is measured for low currents with an IV-source meter [48] and for high currents up to 60 A with a TLP [39]. In Figure 7.38 an equivalent circuit of the measurement setup is shown. Attenuation factors for voltage and current can be calibrated using the HPPI software [51]. The TLP current and voltage waveforms are

measured with an oscilloscope. A Tektronix CT1 current sensor is connected to measure I_{meas} . An additional resistor R_s is connected in the branch to the oscilloscope for attenuation. The voltage V_{meas} can be calculated with knowledge of all attenuation factors from V_{osc} .

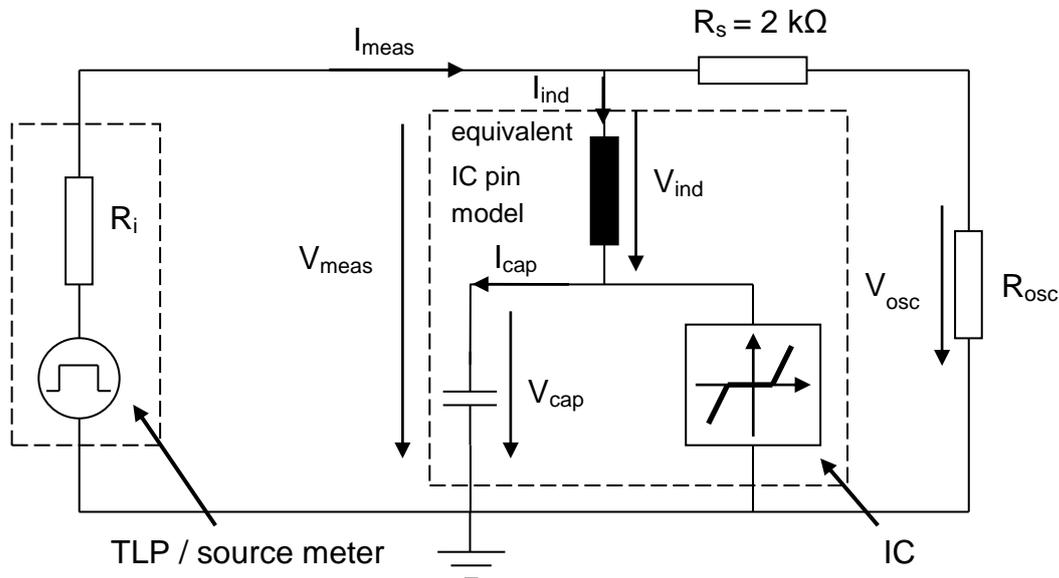


Figure 7.38: Measurement setup for characterization of ICs and behavioral model for an IC pin

The equivalent circuit of each IC pin is composed of elements which describe the static behavior and of those which describe the dynamic behavior.

The general equivalent circuit describing the electrical domain of the IC is shown in Figure 7.39. The frequency dependent parameters are measured with a network analyzer to define the size of the capacitance $C_{parallel}$ and inductance L_{serial} of an IC pin. The characteristic IV curve is composed from the source meter and TLP measurement data. The IV behavior is implemented in the model using a look-up table function. To generate reliable measurement data minimum two equal ICs have to be tested until destruction. Deviations between the failure levels must be low. Good results were obtained with a pulse width of 100 ns. The measurement data can be extrapolated if higher amplitudes should be simulated. Due to missing verification of this model region a warning will be returned by the model.

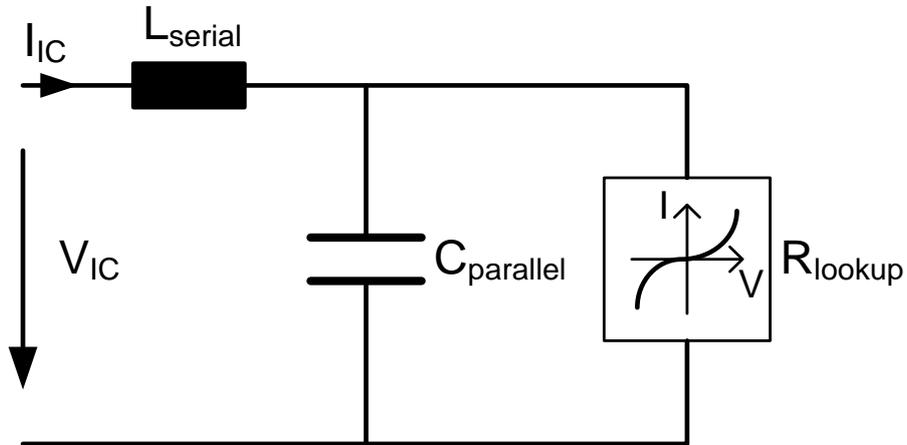


Figure 7.39: IC pin model für ESD failure analysis

The IC pin model can also be used for modeling of ESD-protection devices. Figure 7.40, Figure 7.41 and Figure 7.42 show an example of a composed IV-dataset of a varistor. Data in a dynamic range from nA up to 50 A are obtained by measurement.

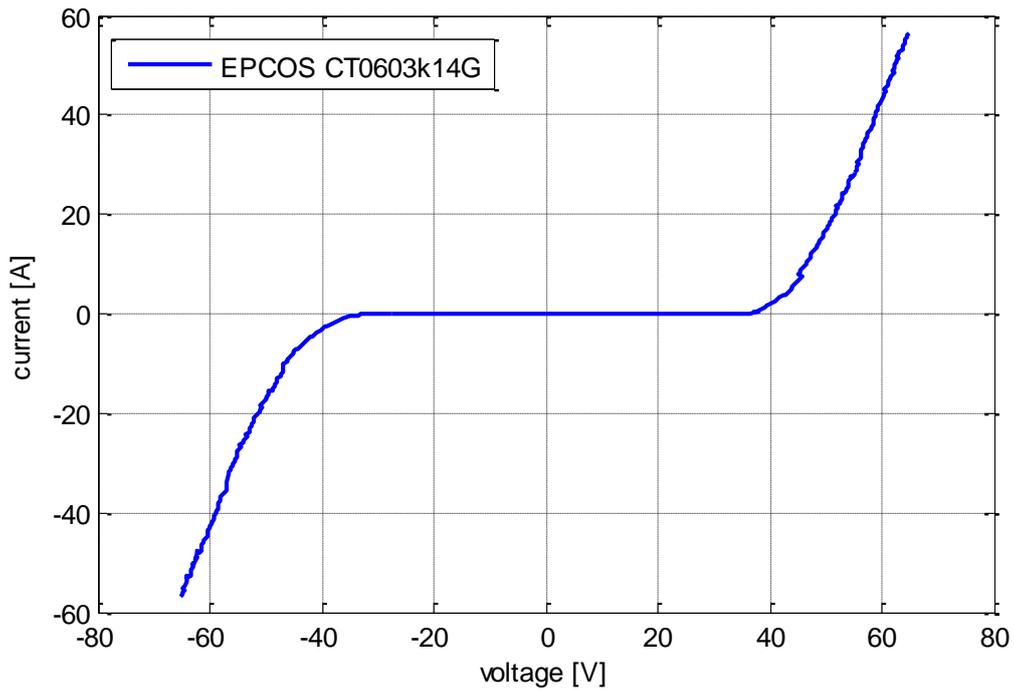


Figure 7.40: Composed varistor IV-curve

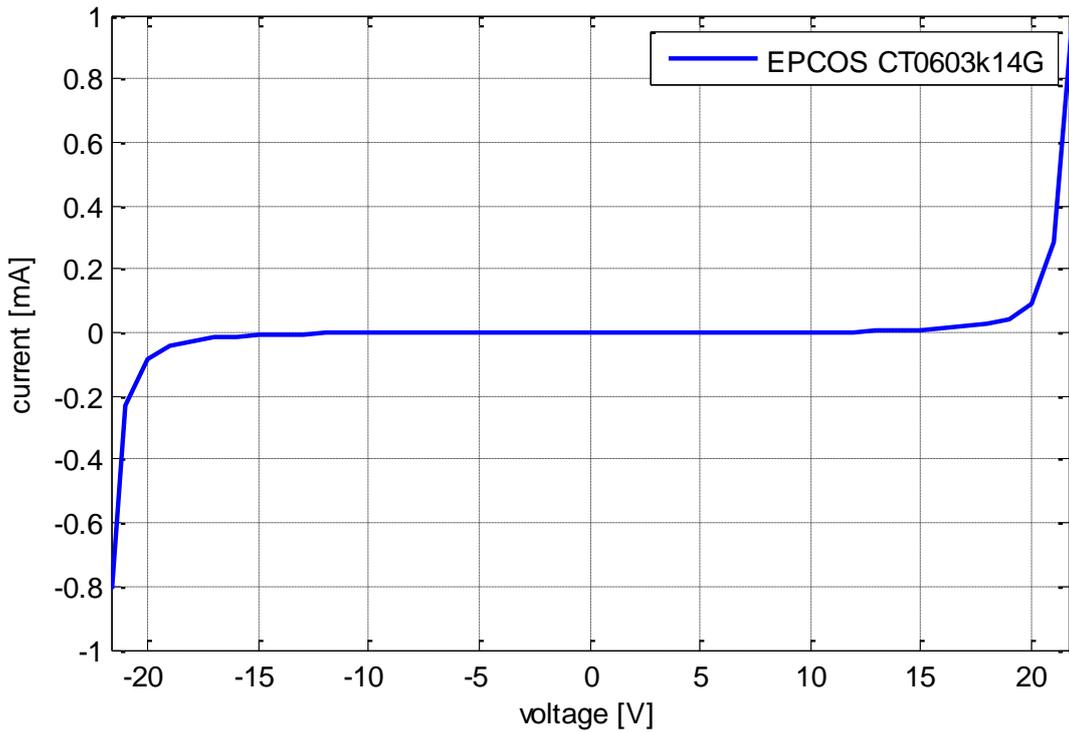


Figure 7.41: Composed varistor IV-curve in detail

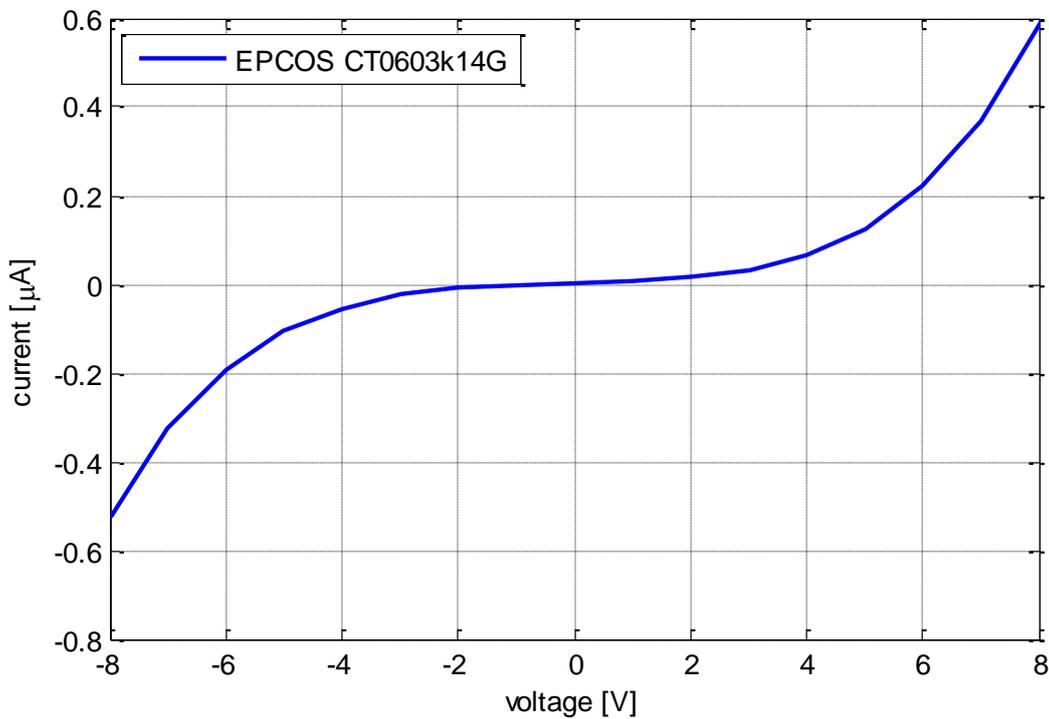


Figure 7.42: Exact modeling of varistor for low voltage behavior

Some protection circuits show a snap-back effect. ICs can be protected using snap-back of the IV curve. If a voltage level is exceeded a breakdown of the voltage occurs.

Current amplitudes are rising. The IV curve in Figure 7.43 shows a snap-back around 250 V for positive and negative amplitudes.

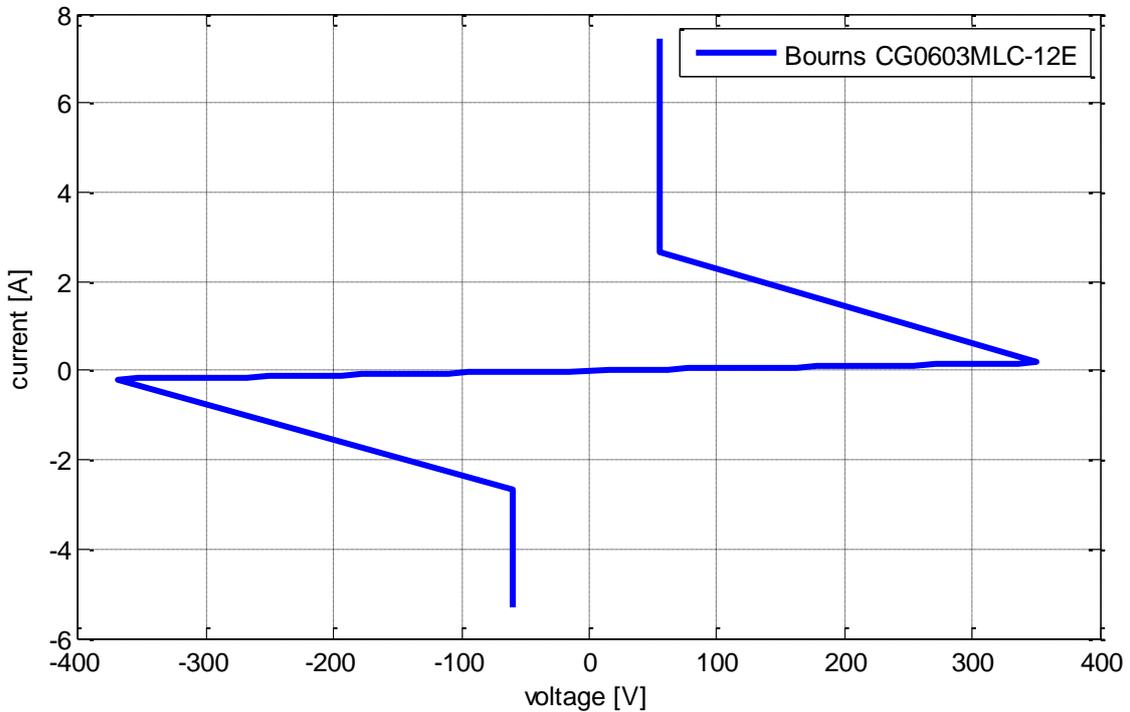


Figure 7.43: Measured IV characteristic of a polymer protection device

Snap-back effects cannot be implemented with a single lookup-table because of continuity problems. For modeling a second dataset has to be composed containing measurement data after the breakdown. In Figure 7.44 the switch S_1 is closed if the defined value of breakdown voltage is exceeded. A more complex implementation is possible if hysteresis functions are considered.

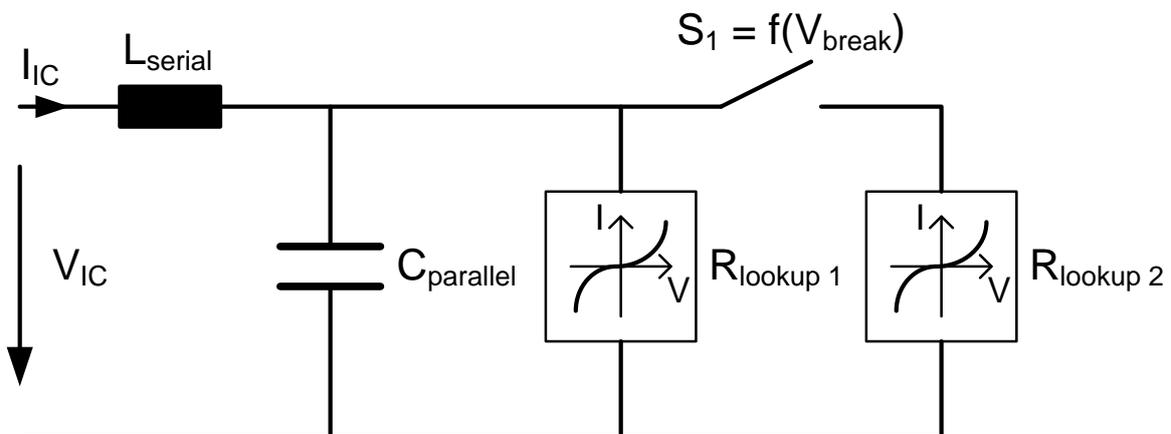


Figure 7.44: ESD protection element model with snap-back

7.6.2 Thermal Failure Model

IC failures can often be referred either to a critical voltage or a critical temperature. In case of critical voltage a dielectric breakdown due to high local field strength inside the semiconductor might have been the reason. Failure voltage is the critical parameter and should be independent from pulse width, when TLP testing is applied. Thermal failures are energy dependent. Energy level should be constant, independent from voltage level, when TLP pulse width is adapted.

Thermal behavior of semiconductors can be represented by thermal capacitor C_{Th} and thermal resistor R_{Th} [58]. An approximately adiabatic change in the silicon temperature is assumed for short time transient pulse stress of ICs in conventional silicon technology. In this case only the thermal capacitor has to be taken into account. For long term or periodic pulses, the heat dissipation to the environment is considered by the thermal resistor R_{Th} [59]. A simplified model for thermal behavior is shown in Figure 7.45.

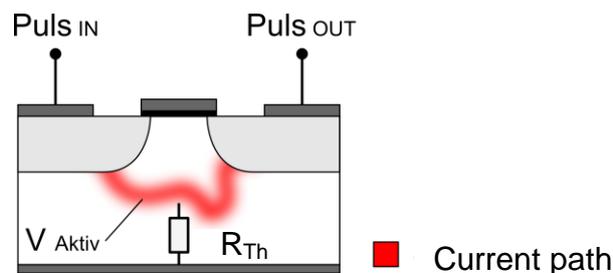


Figure 7.45: Simplified thermal model for an IC pin

For a known geometry of the structure affected by a pulse, the equivalent thermal capacity may be calculated with analytical formulas. The affected silicon volume V_{Active} is determined by several factors, therefore an exact localization is not possible in practice.

TLP based testing of the IC to determine the destruction limit may be used to calculate C_{Th} independent from V_{Active} . Preconditions for the calculation are the known critical semiconductor temperature $T_{structure\ max}$ and the thermal resistance R_{Th} of the IC package. The critical energy is determined by the TLP discharge parameters on the destruction limit of the IC [60]. Based on those three parameters C_{Th} can be calculated. The temperature rise $T_{\Delta} = T_{structure\ max} - T_0$ is obtained as a function of all thermal parameters in the circuit and from environment temperature T_0 .

$$P_{Th} = C_{Th} \cdot \frac{dT_{\Delta}(t)}{dt} + \frac{T_{\Delta}(t)}{R_{Th}} \quad 3$$

The solution of the equation for C_{Th} is:

$$C_{Th} = - \frac{t_{TLP}}{R_{Th} \cdot \ln \left(1 - \frac{T_C - T_0}{P_{TLP} \cdot R_{Th}} \right)} \quad 4$$

A defined critical temperature rise ΔT is reached for a certain failure power P_{TLP} obtained from TLP measurement with the pulse width t_{TLP} . All models are based on TLP data with a selected pulse width of 100 ns. Power P_{TLP} can be calculated from the measured energy E_{TLP} and pulse width t_{TLP} if power output of a TLP discharge is assumed to be constant.

$$P_{TLP} = \frac{E_{TLP}}{t_{TLP}} \quad 5$$

Power dissipation is controlled by the thermal resistance R_{th} which is difficult to estimate because failed chips could not be analyzed and the active area after Wunsch-Bell may change due to local hot spots inside the semiconductor. The active area may decrease to 1/10. This means that the thermal resistance also is affected. For modeling R_{th} should be chosen in accordance with the type of the IC. Dimensions of silicon structures inside ICs with higher ESD robustness are supposed to be larger than inside ESD-sensitive ICs. Thermal resistance R_{Th} therefore should be lower for extended structures and higher for smaller active areas.

IC failure models are implemented in VHDL-AMS in thermal domain. The power at the IC pin is transformed into a heat source in thermal domain. In Figure 7.46 the source indicated with P_{Th} is connected to a thermal capacitor C_{Th} and resistor R_{Th} .

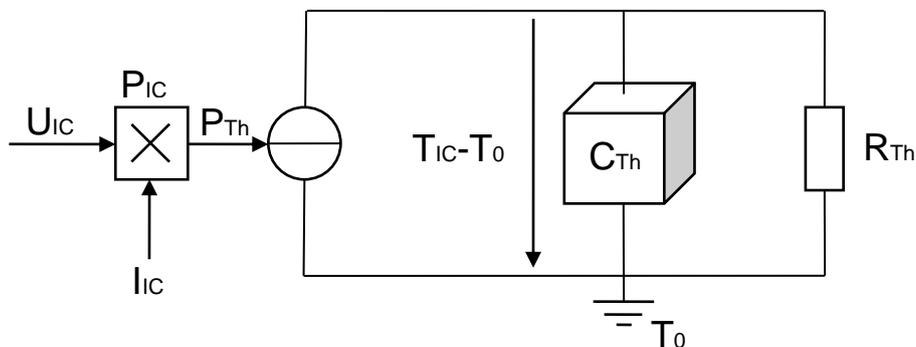


Figure 7.46: Thermal domain of IC model

7.6.3 Scaling of the IC ESD Robustness

Once the model parameters of the test chips are known and the models are verified, the thermal behavior of the models can be modified and the failure levels can be changed in order to simulate different robustness levels.

For simplification the structures in semiconductors are supposed to be in general very simple and identical like shown in Figure 7.47

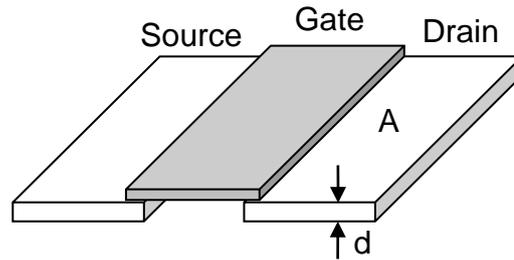


Figure 7.47: Planar structures in semiconductors

The thermal capacitance C_{Th} and resistance R_{Th} then are both dominated by the surface A . This gives another possibility to compute the thermal capacitance from material constants:

$$C_{Th} = \rho \cdot c_p \cdot A \cdot d \quad 6$$

Also thermal resistance can be calculated by:

$$R_{Th} = \frac{d}{k \cdot A} \quad 7$$

κ	Thermal conductivity:	30,6 W/mK (for Si)
c_p	Specific heat capacitance:	756,6 J/kgK (for Si)
ρ	Specific density:	2330 kg/m ³ (for Si)

When scaling down the current-carrying capacity of semiconductor models the thermal capacity decreases. This is equivalent to a downscaling of the dimensions of the IC's ESD protection circuit which also has impact on the thermal resistance R_{th} .

To avoid unbalanced heat dissipation of failure models with scaled thermal domain, the time constant τ of R_{th} and C_{th} is assumed to be constant:

$$\tau = R_{th} C_{th} = const \quad 8$$

This means that the scaling factors are calculated related to a certain pulse energy where the scaled model is supposed to show a given failure behavior. Scaling for a new testing device or a new failure level is performed according to the following steps:

- Simulate the absorbed energy at the IC pin for a new testing device or charging voltage level
- Calculate the factor between the energy obtained for the new testing level and the original IC model
- Divide the original thermal capacitance and resistance by the factor from (2)

7.6.4 TLP-Test-PCB for IC Model Parameterization for μ C, LIN- and CAN-Transceivers

A detailed TLP (transmission line pulser) characterization of all selected IC pins is required for modeling. For measurement with the TLP the ICs are fixed on special test-boards. The layout is optimized for short lengths of PCB traces. To prevent reflections due to mismatch, traces are designed to have a line impedance of $50\ \Omega$ in order to match to the $50\ \Omega$ source impedance of the TLP. The PCBs with dimensions $60\ \text{mm} \times 80\ \text{mm}$ are shown in Figure 7.48 and Figure 7.49.

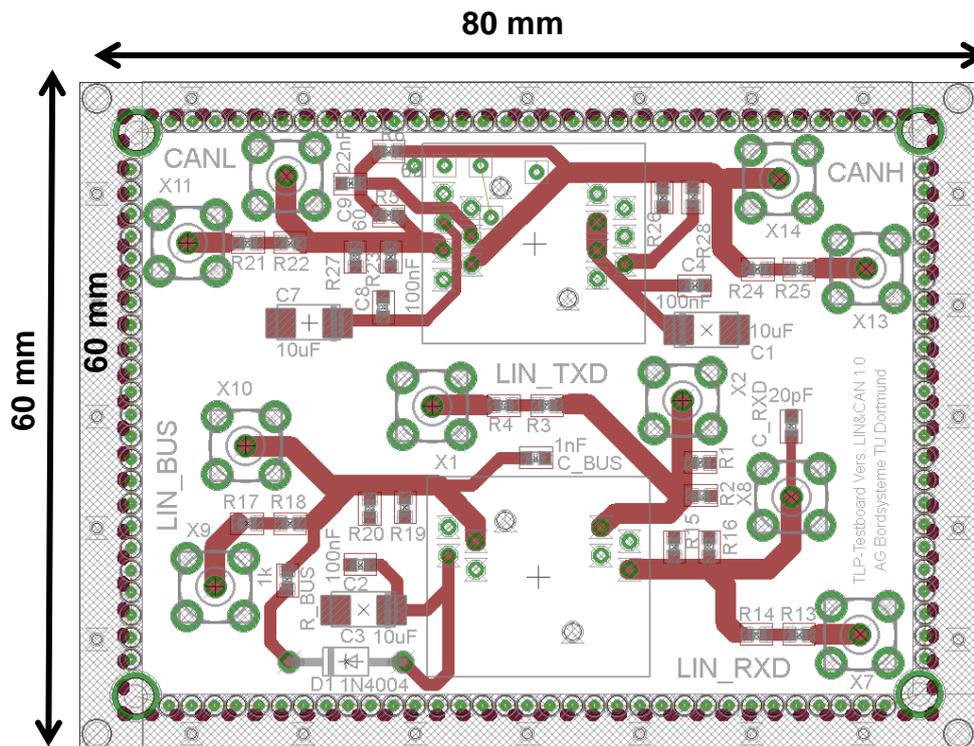


Figure 7.48: TLP testboard with sockets for LIN and CAN transceivers

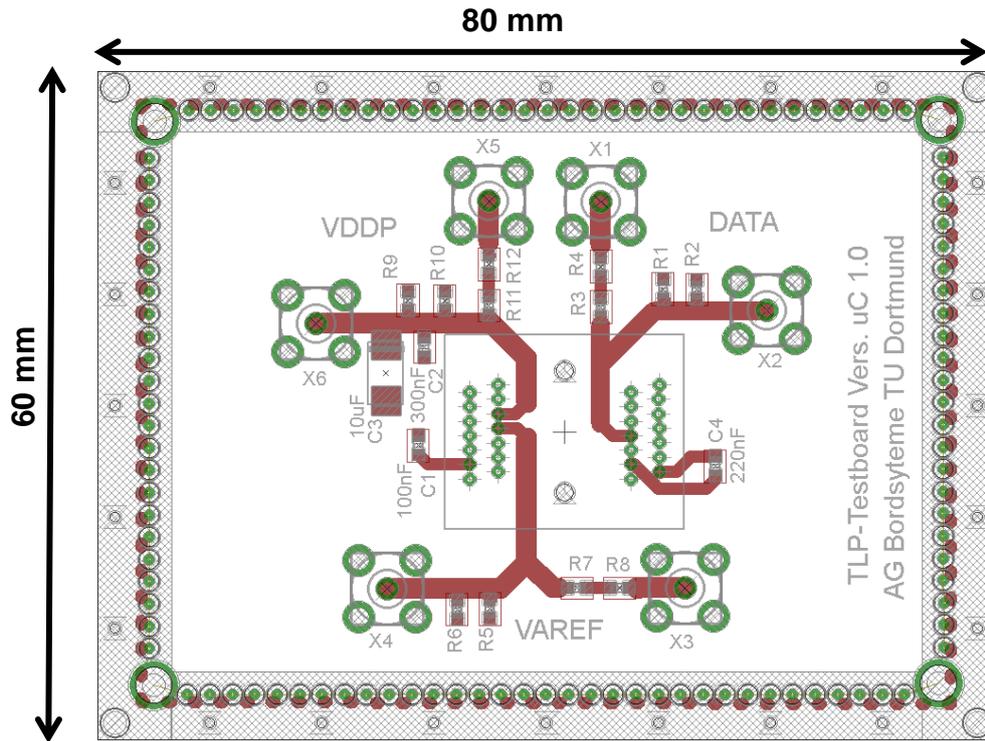


Figure 7.49: TLP testboard with μC socket

Capacitors of $10\ \mu\text{F}$ can be soldered parallel to the voltage supply pins of all ICs for characterization. Similar wiring and circuits as described for the demonstrator PCB are considered in the TLP PCB layout to make sure that testing conditions are comparable in each setup. As a second testing option the ESD robustness of single IC pins protected by parallel devices can be measured with the TLP setup.

7.6.5 Measurement Results

7.6.5.1 Selected ICs

The ESD robustness according to the datasheet is specified up to a testing level of 2 kV HBM for all pins. Although the ESD specification is similar for all pins, a different behavior is expected during characterization and testing.

IC	Pins	ESD protection level	
Infineon XC864 8-bit μC TSSOP-20	All pins	HBM -2 kV..2 kV	C=100 pF R=1,5 k Ω
		CDM -500 V..500 V	C=330 pF R=150 Ω

Table 7.4: ESD protection levels of μC pins as specified in datasheet

The selected ICs are designed to withstand minimum 6 kV IEC discharge for global pins. According to Table 7.5 local pins are specified with 2 kV HBM except the SPLIT-pin of the TLE 6251 G transceiver.

IC	Pins	ESD protection level	
Infineon TLE 6251 G HS-CAN Transceiver P-DSO-14-13	CANH, CANL	IEC -6 kV ..6 kV IEC61000-4-2	C=150 pF R=330 Ω
	CANH, CANL, WK	HBM -6 kV..6 kV	C=100 pF R=1,5 kΩ
	SPLIT	HBM -1 kV..1 kV	C=100 pF R=1,5 kΩ
	All other pins	HBM -2 kV..2 kV	C=100 pF R=1,5 kΩ
NXP TJA1041T SO14	CANH, CANL, SPLIT	HBM -6 kV ..6 kV	C=100 pF R=1,5 kΩ
	TXD, RXD, VI/O, STB	HBM -3 kV..3 kV	C=100 pF R=1,5 kΩ
	All other pins	HBM -4 kV..4 kV	C=100 pF R=1,5 kΩ
	All pins	MM -200 V..200 V	C=200 pF R=10 Ω

Table 7.5: ESD specifications of selected CAN transceivers

In comparison to microcontrollers a higher level of ESD protection is specified for most LIN pins. Available parameters from Datasheet are listed in Table 7.6.

IC	Pins	ESD protection level	
Infineon TLE7259-2GE LIN Transceiver PG-DSO-8	Bus Pins	IEC -11 kV ..11 kV IEC61000-4-2	C=150 pF R=330 Ω
	Vs, Bus, WK vs. GND	HBM -6 kV..6 kV	C=100 pF R=1,5 kΩ
	All pins	HBM -2 kV..2 kV	C=100 pF R=1,5 kΩ
Atmel ATA6662C LIN Transceiver SO8	Vs, LIN vs. GND	IEC -6 kV ..6 kV IEC61000-4-2	C=150 pF R=330 Ω
	WK	IEC -5 kV ..5 kV IEC61000-4-2	C=150 pF R=330 Ω
	Vs, LIN, WK, INH Pins vs. GND	HBM -6kV..6kV	C=100 pF R=1,5 kΩ

	All Pins	other	HBM -3 kV ..3 kV MM -100 V..100 V CDM -750 V..750 V	C=100 pF R=1,5 kΩ C=500 pF R=10 Ω L=0.75 μH C=330 pF R=150 Ω
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Table 7.6: ESD specifications of selected LIN transceivers

For selected diodes no information about ESD robustness is provided by datasheet.

IC	Pins	ESD protection level
NXP BAW156	All pins	Not available
Not available Rearlight LED	All pins	Not available

Table 7.7: ESD specifications of selected diodes

7.6.5.2 Characterization of Selected IC Pins with TLP

The characterization data for the selected IC pins is measured with two measurement setups. The TLP measurement setup shown in section 7.6.5.2.1 was used in time domain. A frequency domain setup with a network analyzer is described in section 7.6.5.2.2. In the following sections 7.6.5.4.1, 7.6.5.3.1 and 7.6.5.5.1 waveforms and IV curves are presented for a LIN ATA6662C transceiver, CAN TJA1041T transceiver and a XC864 microcontroller. For verification of the measurement data and the created model simulated and measured waveforms are compared.

7.6.5.2.1 Time Domain Measurement Setup

The time domain characterization setup shown in Figure 7.50 is controlled via a PC which is connected to the TLP unit, a fast 6 GHz 20 GS/s oscilloscope, and a source meter with minimal current resolution of 10 pA. All instruments are connected to the test board by a switch.

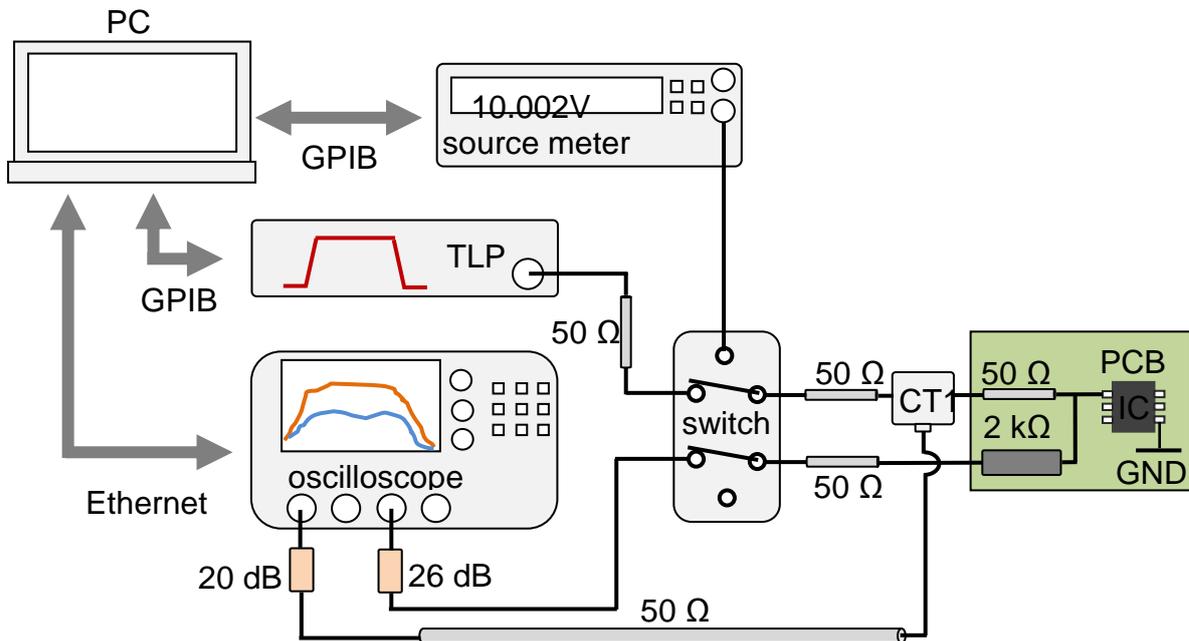


Figure 7.50: Measurement setup for IC characterization

For the investigations two test boards were developed. On the board shown in Figure 7.51 selected socket pins for CAN and LIN transceivers are connected via short traces to SMA connectors for measurement. Each selected pin for characterization is independent so that all SMA connectors are left open on the board except two used for measurement. Current is measured with a CT1 current sensor. Voltage and current amplitudes are attenuated by minimum 20 dB in order to protect measurement devices.

Figure 7.52 shows the equivalent test board with a socket for the μC . During measurement the PCBs were screwed on a metal plane to ensure adequate grounding conditions.

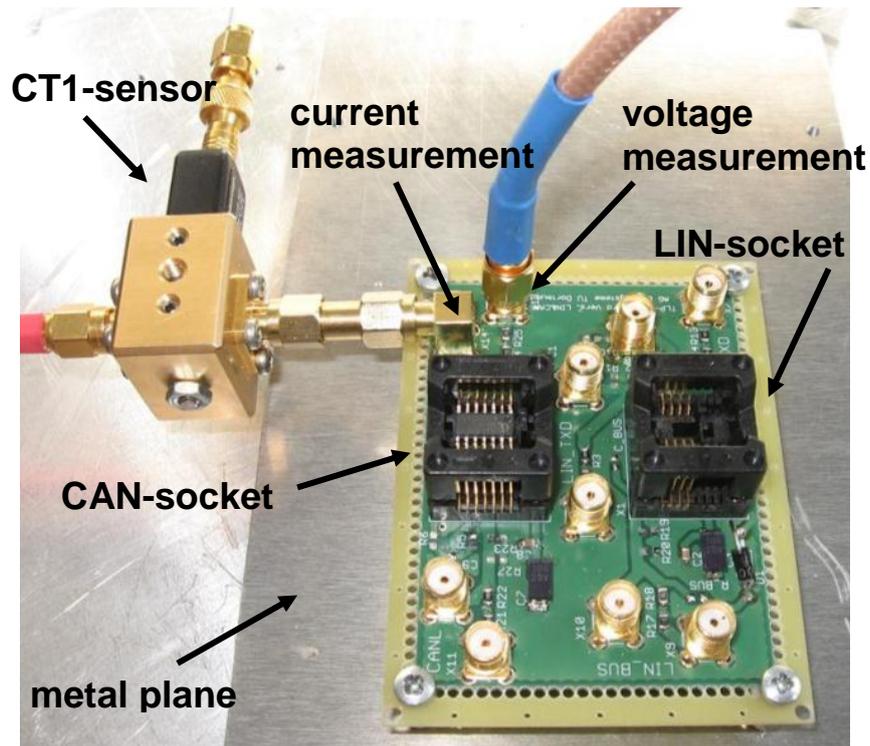


Figure 7.51: TLP measurement setup with PCB for LIN and CAN transceivers

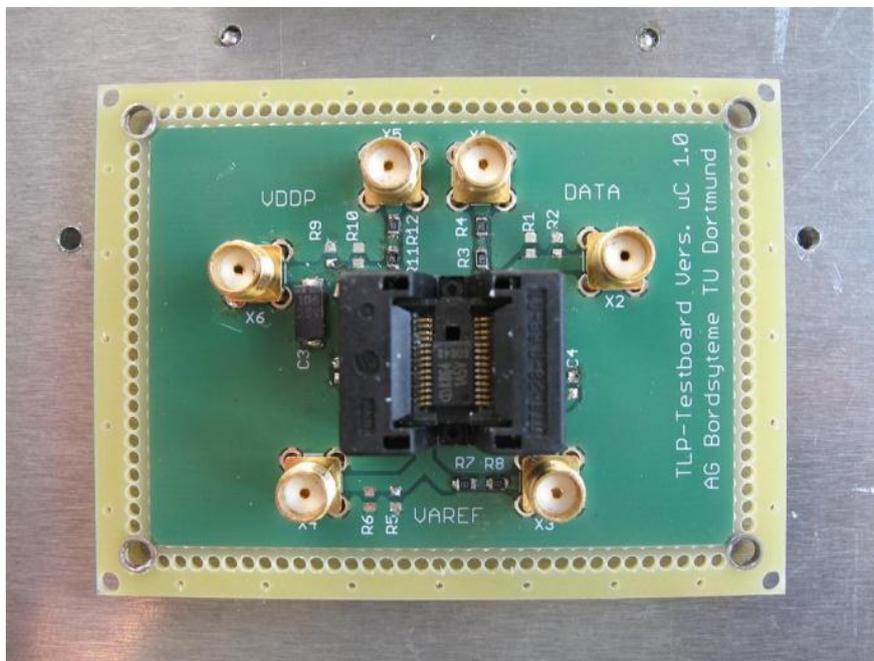


Figure 7.52: TLP board with μ C socket

The settings of the TLP measurement setup are calibrated using a resistor. In Figure 7.53 the IV curves measured with TLP and source meter for a 47Ω resistor are compared. The curve consists of 2 TLP datasets and 1 dataset from source meter. For low charging voltages of the TLP some deviations may occur because of high attenuation factors. Precise results are obtained for high charging voltages.

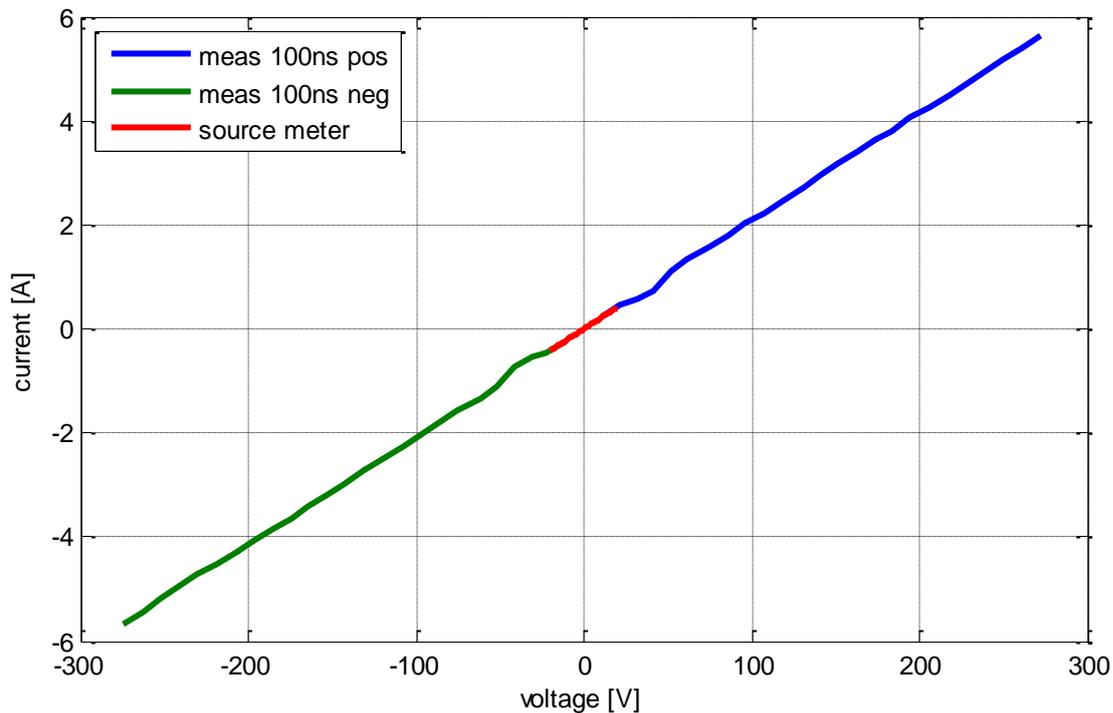


Figure 7.53: Measured IV curve of a 47 Ω resistor

As a first step for IC testing a TLP sweep with negative and positive charging voltages is done to estimate the negative and positive breakdown voltages of the ESD structures. Then the static behavior is measured with the source meter till 95 % of the estimated breakdown voltage is reached. Breakdown voltage of an IV curve is defined where the current increases more than 10 % compared to the preceding voltage step. From the measured curve a characteristic point is also selected at about 90 % of the defined breakdown voltage. This current at the characteristic point will be monitored after each TLP discharge which is major criteria for destruction of an IC. Permanent IC damage generally is assumed if a DC current measurement at a voltage level before the characteristic point exceeds the initially measured values by a factor of ten.

The failure energies are determined with changing voltage amplitude until destruction of the IC is detected with IV curve measurements. The increment of the charging voltage should be selected dynamically to minimize pre-damaging. Smaller voltage steps are applied close to the level of breakdown voltage which is an first estimation for the failure level.

7.6.5.2.2 Frequency Domain Measurement Setup

S-parameters are measured with a network analyzer (NWA) according to Figure 7.54. For more accuracy TLP testboards were used without sockets. The NWA was calibrated by soldering open short and load SMD devices on the PCB close to the IC

soldering pads. Values for the pin capacitance C are calculated from S11 parameters at 10 MHz and for pin inductance L at about 1GHz.

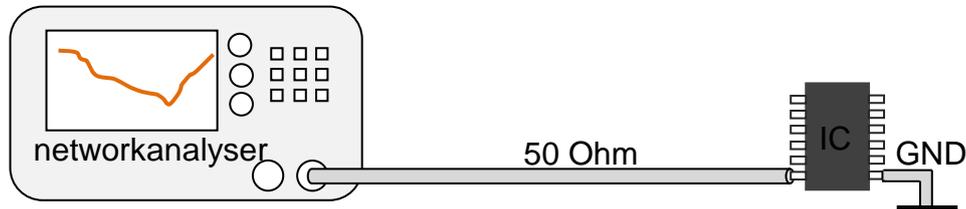


Figure 7.54: Setup for IC characterization in frequency domain

7.6.5.3 CAN Transceivers

7.6.5.3.1 Characterization of CAN Transceiver TJA1041T CANH

In Figure 7.55 a circuit diagram is given. 10 μF and 100 nF capacitors are connected to V_S and V_{CC} pins in order to obtain realistic conditions for failure model parameter measurements with TLP.

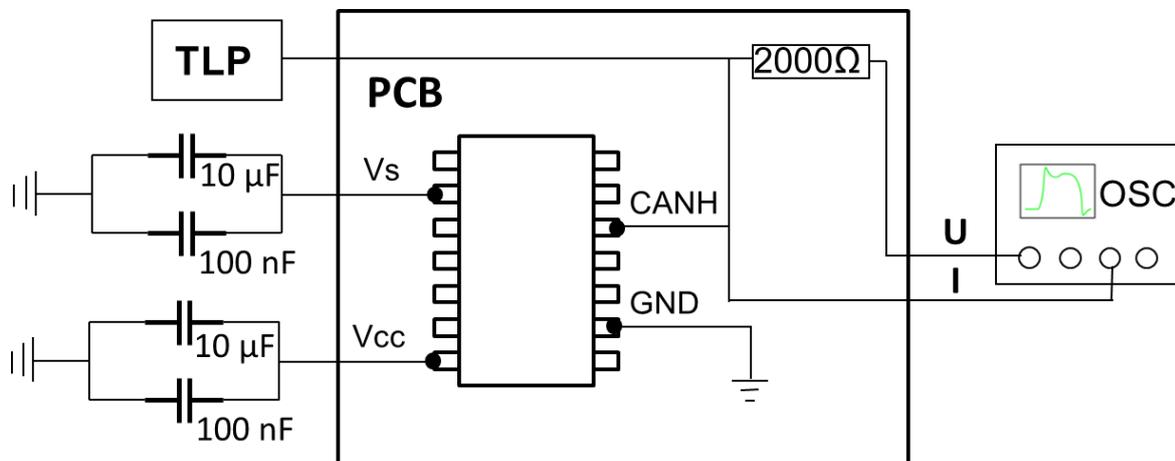


Figure 7.55: Circuit diagram of TLP measurement setup for CAN TJA1041T CANH pin

The overlaying IV curves of the selected CANH pin are shown in Figure 7.56 for positive charging voltages. Destruction was detected for all pulse widths.

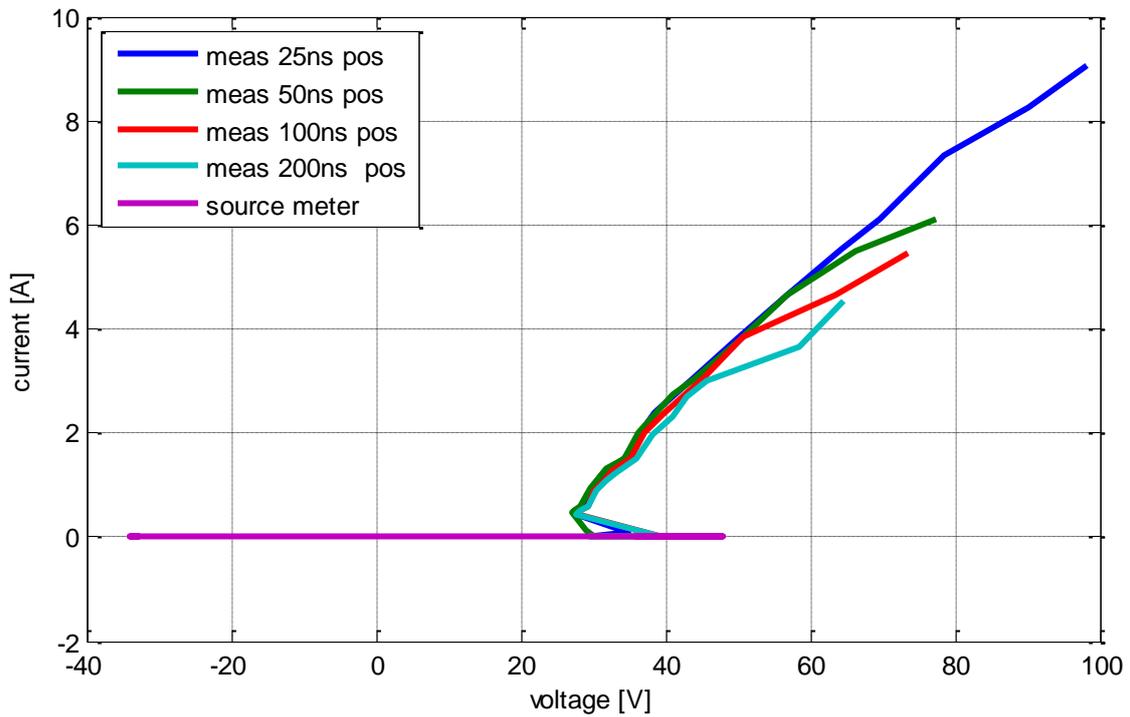


Figure 7.56: Comparison of measured IV-characteristics for CANH pin

The positive critical curve shapes of TLP pulses for the CANH pin are shown in Figure 7.57 and in Figure 7.58. Table 7.8 includes all measured amplitudes and energies for the selected pulse widths. The highest amplitudes before destruction is detected about 126 V and 7.3 A. Similar to LIN TxD the calculated energies differ by a factor of 2 for 25 ns and 200 ns pulses.

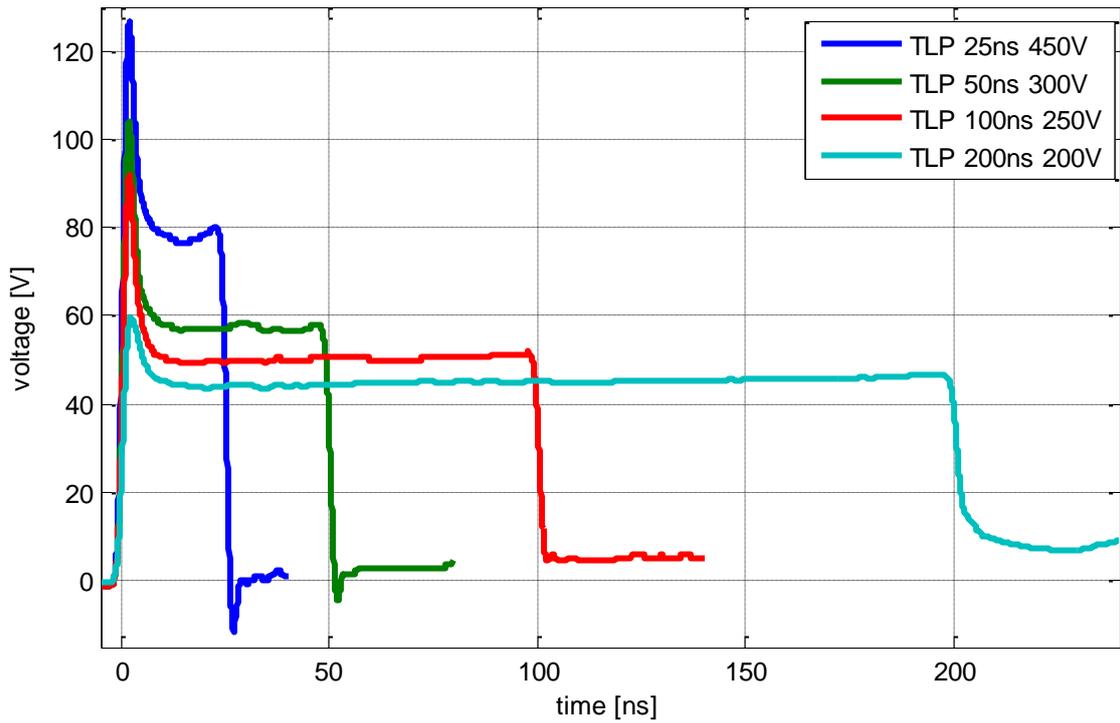


Figure 7.57: Critical positive voltage waveforms for different pulse widths at CANH pin

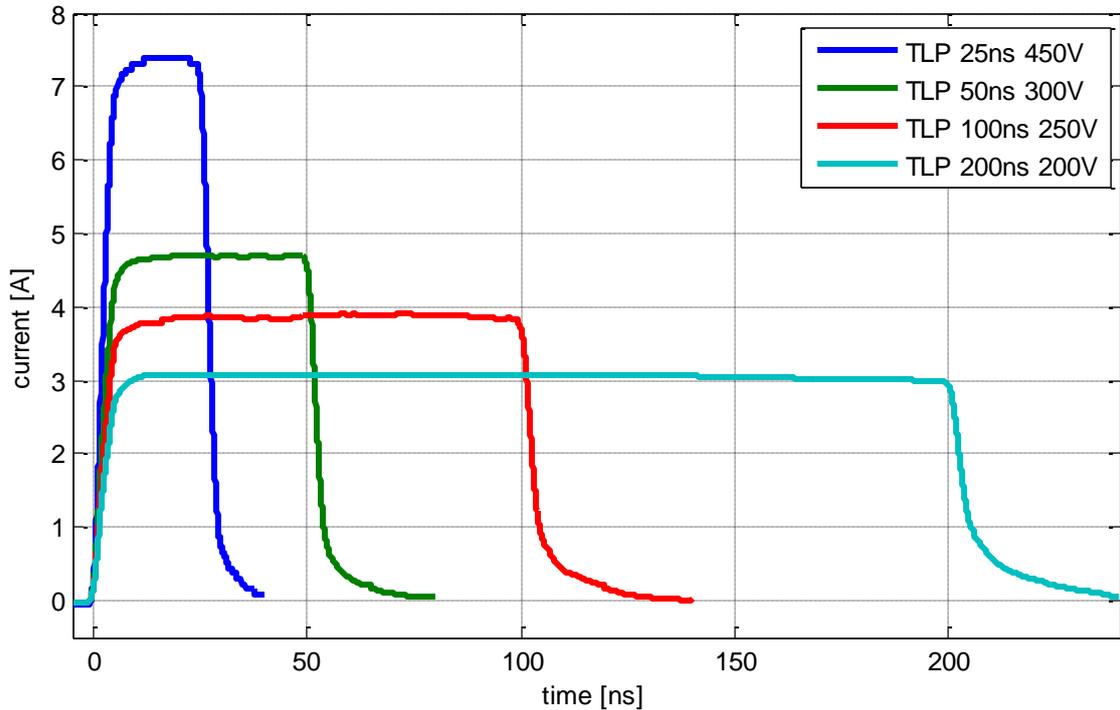


Figure 7.58: Critical positive current waveforms for different pulse widths at CANH pin

IC (PIN)	t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [μ J]
CAN-	25	450	126.5	7.3	78.5	7.3	13.6

TJA1041T (CANH)	50	300	104.1	4.7	56.7	4.6	13.1
	100	250	91.8	3.9	50.6	3.9	19.2
	200	200	59.5	3.0	45.7	3	27.5

Table 7.8: Measured parameters with variation of TLP pulse width for CANH pin

In frequency domain a capacitance of 10.5 pF and inductance of 4.5 nH was measured for the CANH pin.

IC (PIN)	C _{parallel}	L _{serial}
TJA1041T (CANH)	10.5 pF @ 10 MHz	4.5 nH @ 1 GHz

Table 7.9: Measured values for L_{serial} and C_{parallel} for CANH pin

7.6.5.3.2 Characterization of CAN Transceiver TLE6251G CANH

Test setup is equal to TJA1041T transceiver (see Figure 7.55). 10 µF and 100 nF capacitors are connected to V_S and V_{CC} pins in order to obtain realistic conditions for failure model parameter measurements with TLP.

The overlaying IV curves of the selected CANH pin are shown in Figure 7.59. For 25 ns pulse width no destruction was detected.

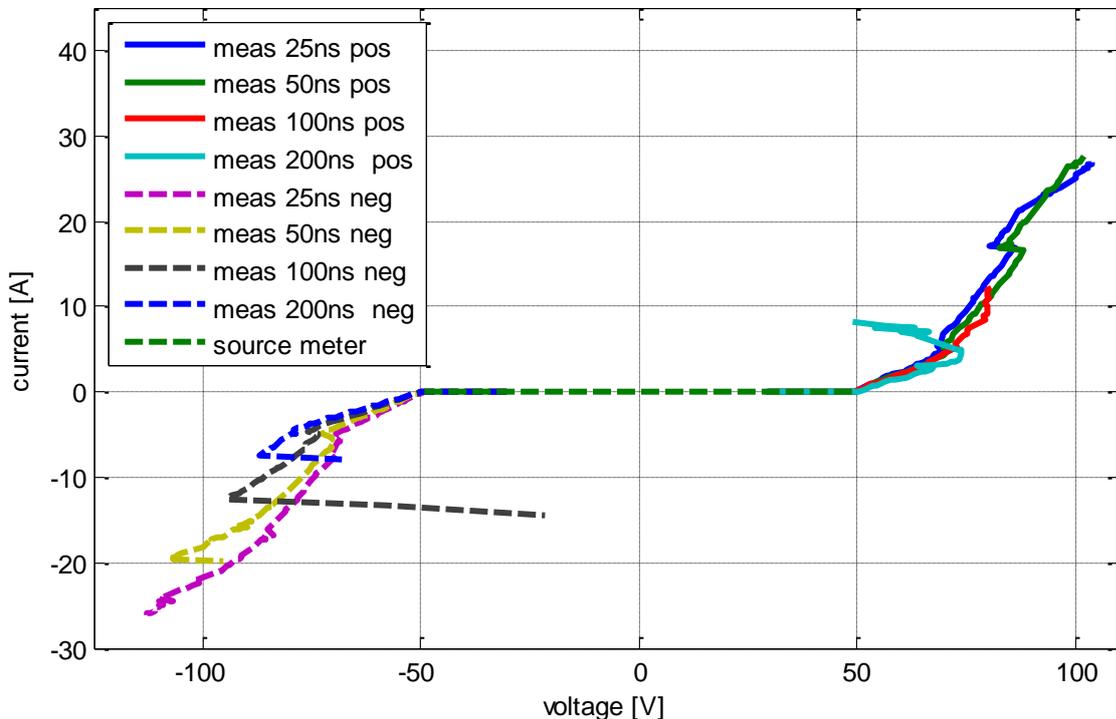


Figure 7.59: Comparison of measured IV-characteristics for CANH pin

In Figure 7.60 and Figure 7.61 the critical waveforms are compared for different pulse widths for positive TLP charging voltages before destruction. TLP charging voltage and pulse width behave inversely proportional. Due to similar charging voltage for

25 ns and 50 ns pulses, amplitudes of the similar range are observed. A high serial inductivity of the pin leads to high initial voltage peaks. Increasing TLP pulse length require less charging voltage for a damage of the IC pin.

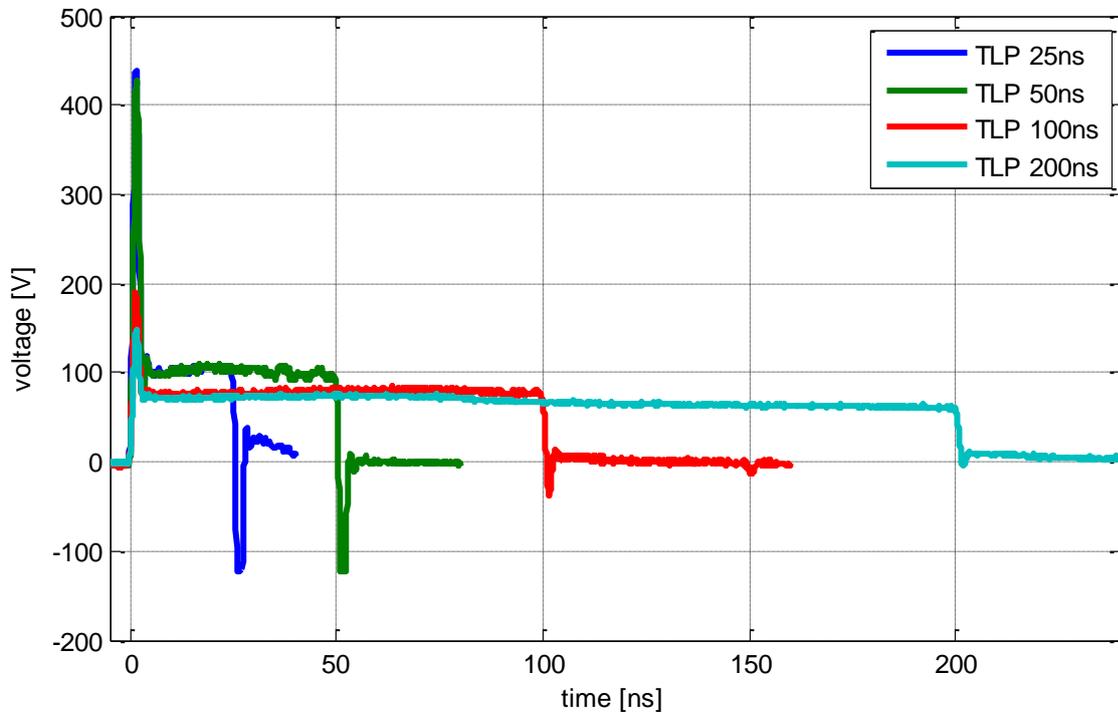


Figure 7.60: Critical positive voltage waveforms for different pulse widths at CANH pin

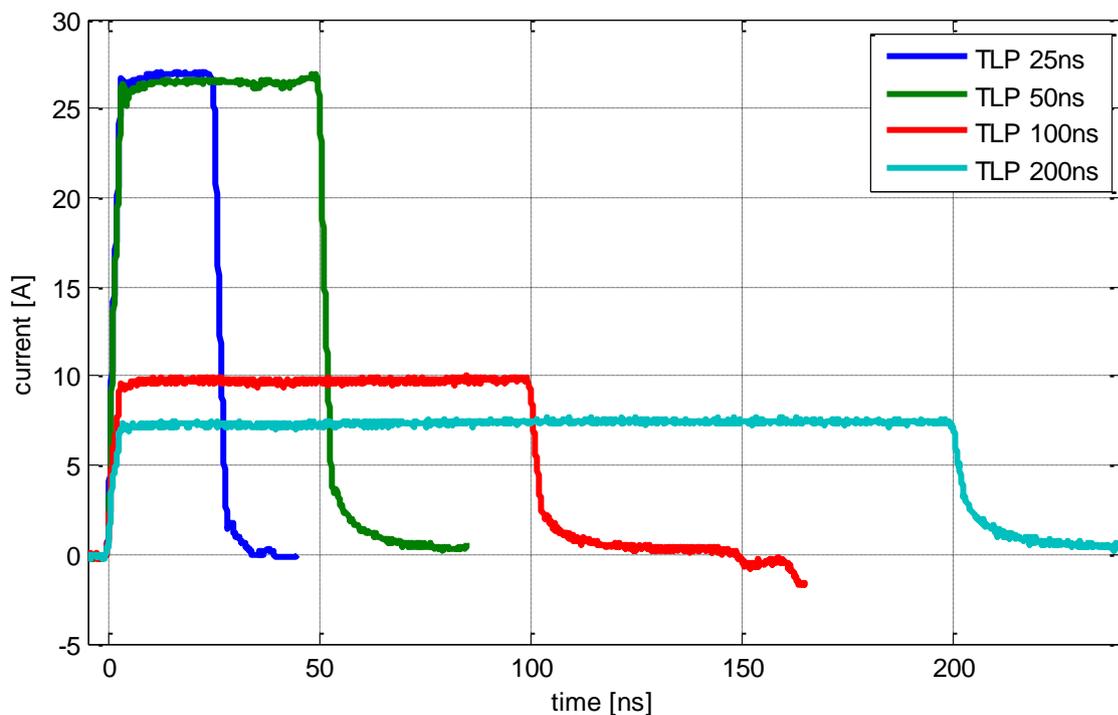


Figure 7.61: Critical positive current waveforms for different pulse widths at CANH pin

Table 7.10 summarizes the parameters from the curves. For 25 ns measurement no IC damage could be detected. Maximum charging voltage was 1480 V where a peak voltage of 439 V and a peak current of 27 A were measured. The energy can be calculated from current and voltage waveforms. The critical energy by a 50 ns TLP pulse is much higher compared to others. This is considered as an outlier.

t_{TLP} [ns]	+/-	U_{TLP} [V]	U_{max} [V]	I_{max} [A]	E_{aus} [μ J]
25	+	1480	439	27	69.94
50	+	1430	428	26	130.78
100	+	565	191	10	77.31
200	+	440	147	8	93.79

Table 7.10: Measured parameters with variation of TLP pulse width for CANH pin

Table 7.11 shows the results of measurement in frequency domain. Relatively high serial inductance of 21.7 nH can be noticed.

IC (PIN)	$C_{parallel}$	L_{serial}
TJA6251G (CANH)	25 pF @ 10 MHz	21.7 nH @ 1 GHz

Table 7.11: Measured values for L_{serial} and $C_{parallel}$ for CANH pin

7.6.5.3.3 Characterization of CAN Transceiver TLE6251G Split

TLP test setup is similar to TJA1041T transceiver, instead of CANH the Split pin is processed (see Figure 7.55).

All measured IV curves are shown in Figure 7.62. Because of a limited number of testing transceivers a 200 ns measurement was not performed. For positive charge voltage a good match of the curves may be registered. For negative charge voltage the slope reduces with higher pulse width. For 25 ns pulse width no destruction was detected for both polarities.

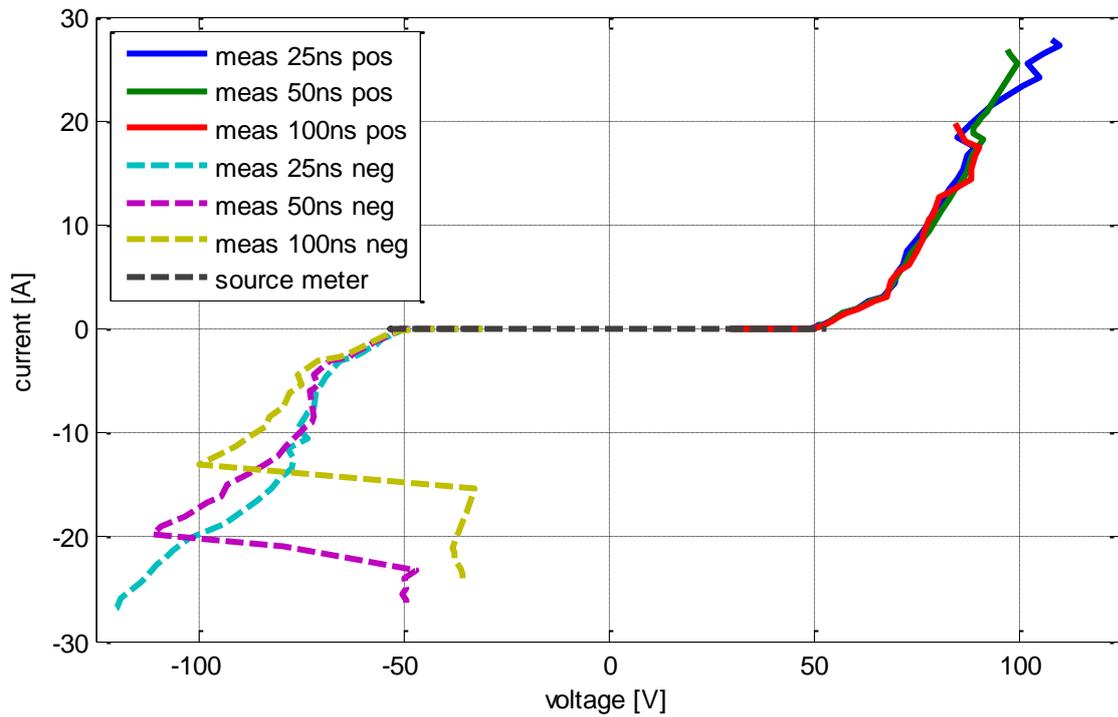


Figure 7.62: Comparison of measured IV-characteristics for Split pin

Figure 7.63 and Figure 7.64 shows the critical waveforms for positive TLP charging voltages. According to the calculated energy for 25 ns TLP pulse, an insignificant larger voltage as 1480 V would lead to an IC damage. The voltage and current level are nearly constant over the pulse length. The initial voltage peaks are up to about four times higher than the clamping voltages. All measured amplitudes are listed in Table 7.12.

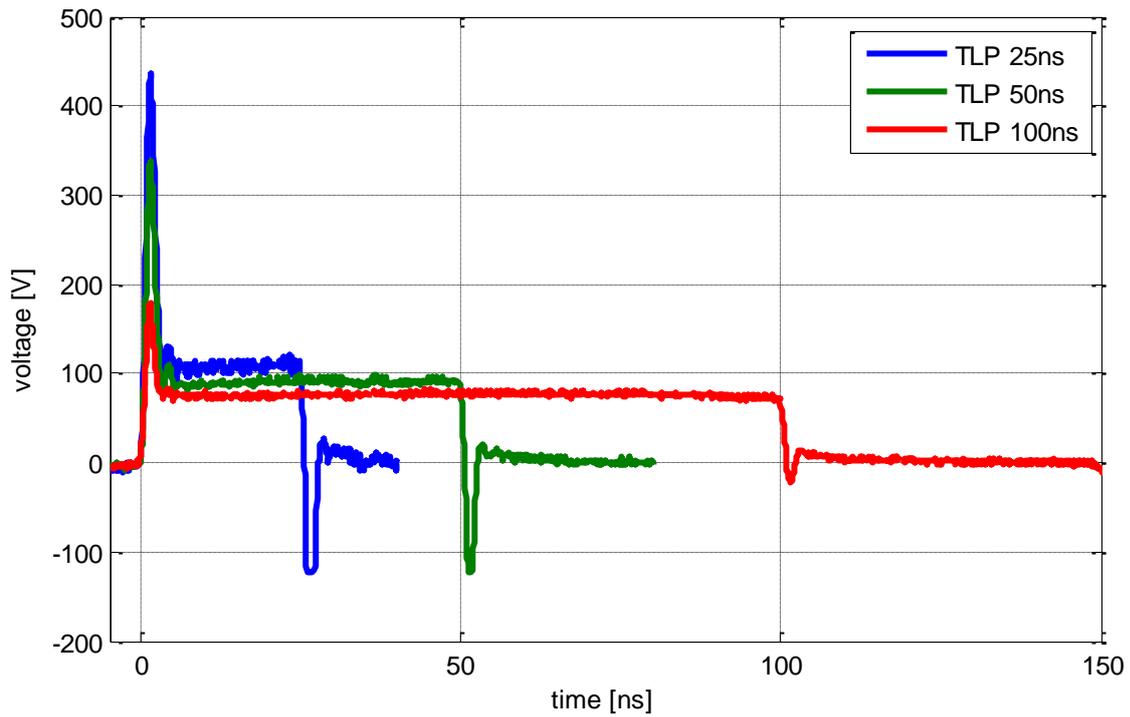


Figure 7.63: Critical positive voltage waveforms for different pulse widths at Split pin

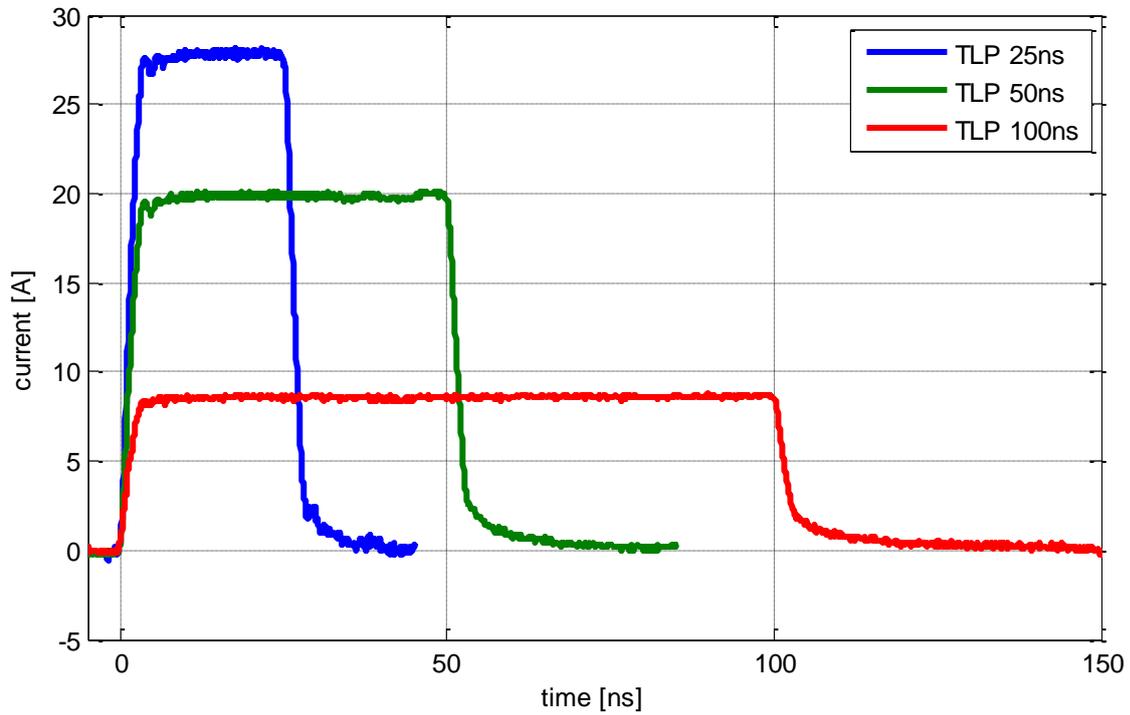


Figure 7.64: Critical positive current waveforms for different pulse widths at Split pin

IC (PIN)	t_{TLP} [ns]	+/-	U_{TLP} [V]	U_{max} [V]	I_{max} [A]	E_{aus} [μ J]
CAN-TLE6251G (SPLIT)	25	+	1480	436	27.8	75.06
	50	+	1150	338	20.8	89.20
	100	+	500	179	8.6	65.79

Table 7.12: Measured parameters with variation of TLP pulse width for Split pin

Table 7.13 shows the results of measurement in frequency domain. Relatively high serial inductance of 17.8 nH can be noticed.

IC (PIN)	$C_{parallel}$	L_{serial}
TLE6251G (Split)	13.8 pF @ 10 MHz	17.8 nH @ 1 GHz

Table 7.13: Measured values for L_{serial} and $C_{parallel}$ for Split pin

7.6.5.4 LIN Transceivers

7.6.5.4.1 Characterization of LIN Transceiver ATA6662C TxD

In Figure 7.65 the schematic of the measurement setup is shown. 10 μ F and 100 nF capacitors are connected to V_s pin in order to obtain realistic conditions for failure model parameter measurements.

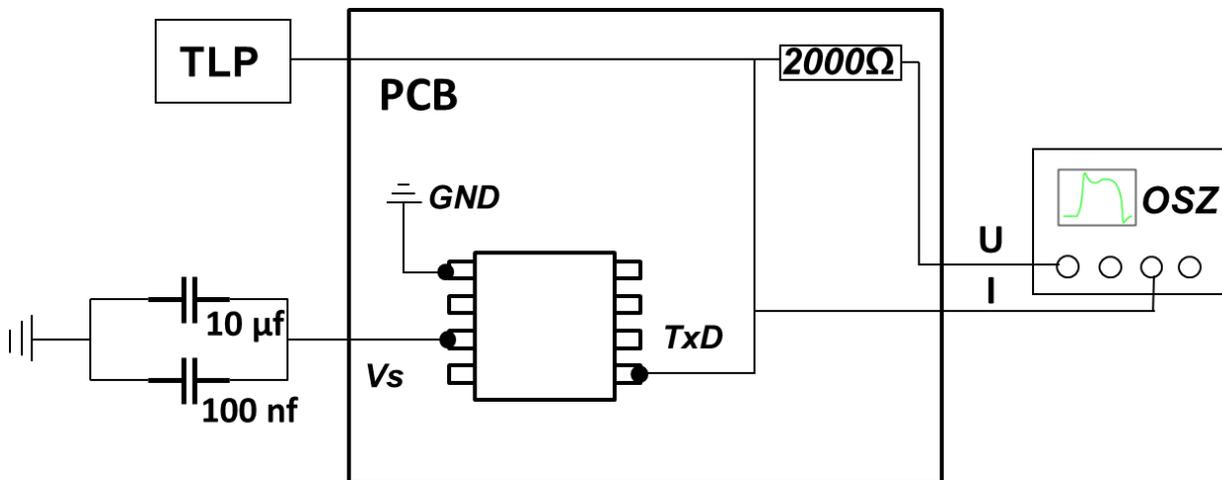


Figure 7.65: Schematic of TLP measurement setup for LIN ATA6662C TxD pin

The IV curves for the LIN TxD pin are shown in Figure 7.66. Measurement data up to about 13 A were measured for 25 ns pulse width. Beside from the measured DC spot current yet the last points of each IV curve indicate destruction of the IC because of a significant voltage drop.

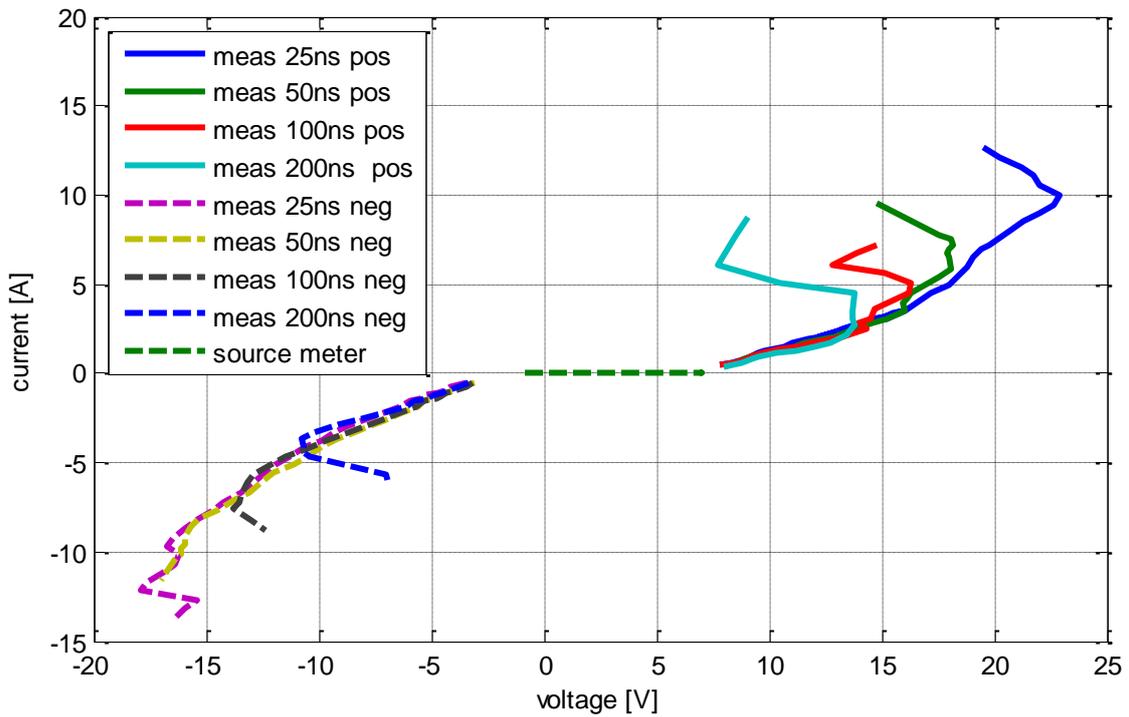


Figure 7.66: Comparison of measured IV characteristics for LIN TxD pin

In Figure 7.67 and Figure 7.68 the critical waveforms are compared for different pulse widths for positive TLP charging voltages before destruction. TLP charging voltage and pulse width behave inversely proportional.

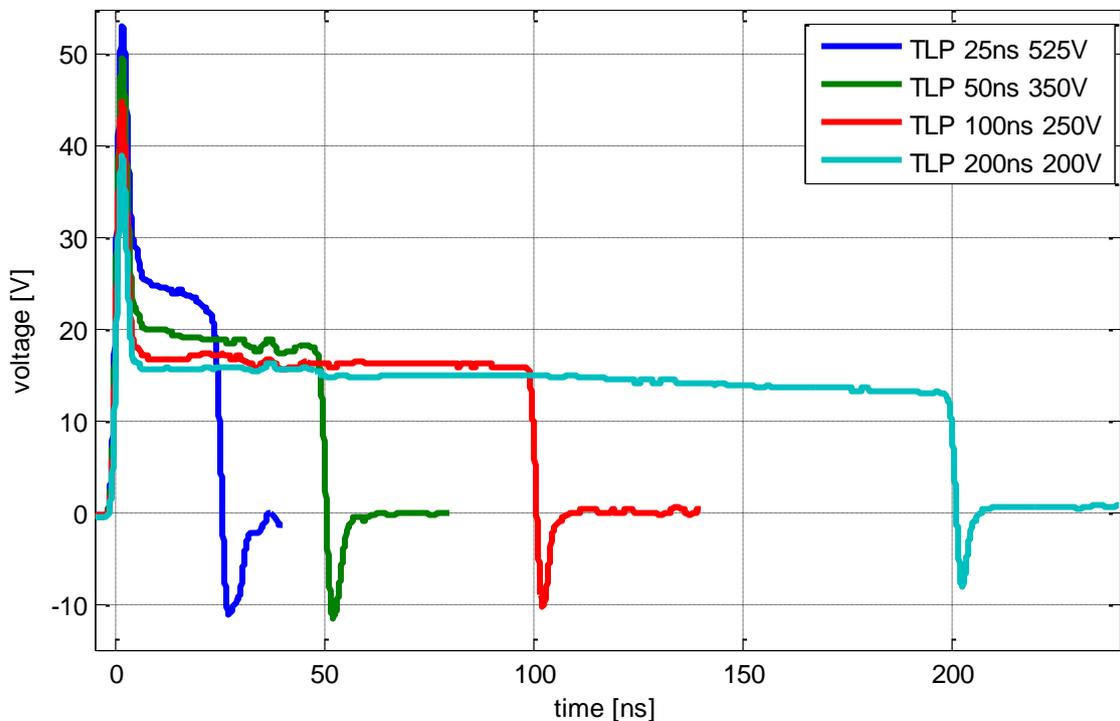


Figure 7.67: Critical positive voltage waveforms for different pulse widths at LIN TxD pin

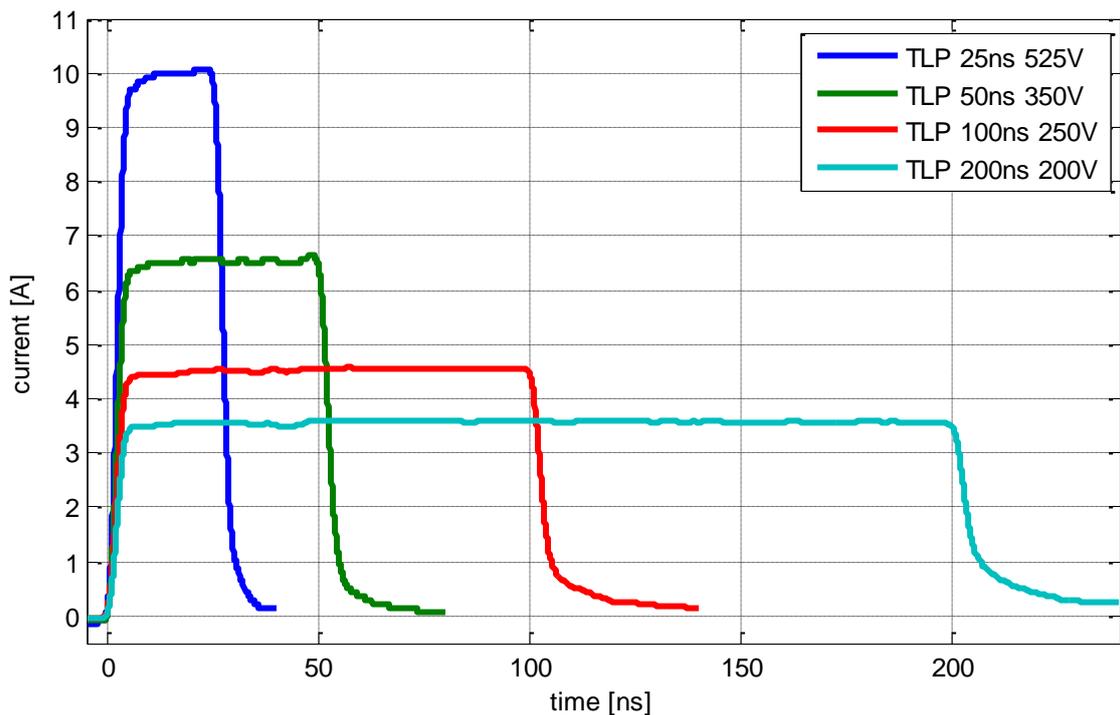


Figure 7.68: Critical positive current waveforms for different pulse widths at LIN TxD pin

Table 7.14 summarizes the parameters from the curves. Maximum charging voltage was 525 V where a peak voltage of 53 V and a peak current of 10 A were measured. The energy can be calculated from current and voltage waveforms. For many IC-pins an increasing critical energy can be found with increasing pulse width. This fact can be explained by heat dissipation before the pulse has decayed which is especially true for 200 ns pulses.

IC (PIN)	t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [μ J]
LIN-ATA6662C (TXD)	25	525	53.2	10.0	22.9	10	5.8
	50	350	49.7	6.6	18	6.5	6.1
	100	250	44.8	4.6	16.2	4.6	7.4
	200	200	39.0	3.6	13.7	3.6	10.4

Table 7.14: Measured parameters with variation of TLP pulse width for LIN TxD pin

All parallel IC-capacitances C and serial IC-package-inductances L for modeling were measured with a network analyzer without a bias voltage. Table 7.15 contains the results for LIN TxD pin. Measurement data in frequency domain was measured without additional capacitors connected to the IC pins.

IC (PIN)	C _{parallel}	L _{serial}
ATA6662C (TxD)	8.5 pF @ 10 MHz	2.5 nH @ 1 GHz

Table 7.15: Measured values for L_{serial} and C_{parallel} for TxD pin

7.6.5.4.2 Characterization of LIN Transceiver ATA6662C BUS

The measurement setup is identical to the one shown in Figure 7.65, except the processed BUS pin.

All measured IV curves are shown in Figure 7.62. Because of a limited number of testing transceivers only the 100 ns measurement was performed for negative charging voltages. For positive charge voltages the slope reduces with higher pulse width. For 25 ns pulse width no IC damage could be detected. Apart to an increased leakage current a significant voltage drop can be detected after IC damage for both polarities.

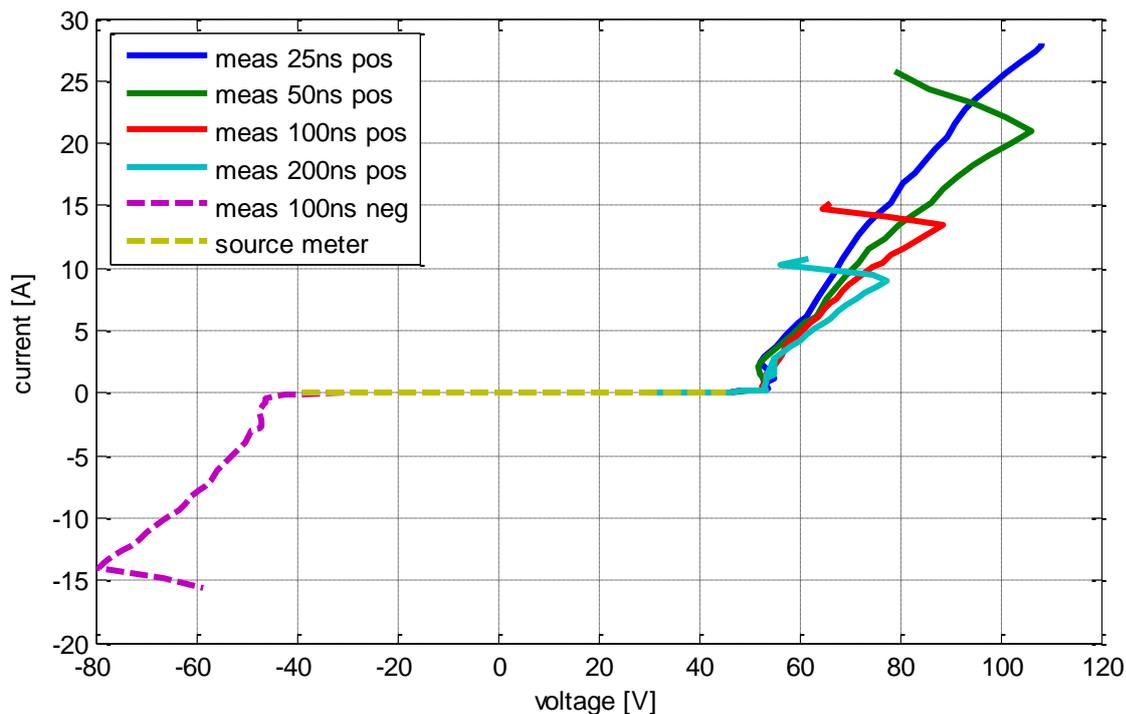


Figure 7.69: Comparison of measured IV-characteristics for BUS pin

Figure 7.70 and Figure 7.71 show the critical waveforms for positive TLP charging voltages. The initial voltage peak is followed by rise of the voltage with progress of the TLP pulse. This could be caused by heating effects in the IC's current path. The rise accounts about 10 % for the 25 ns measurement, however no damage was detected. The current remains at the same level over the pulse width.

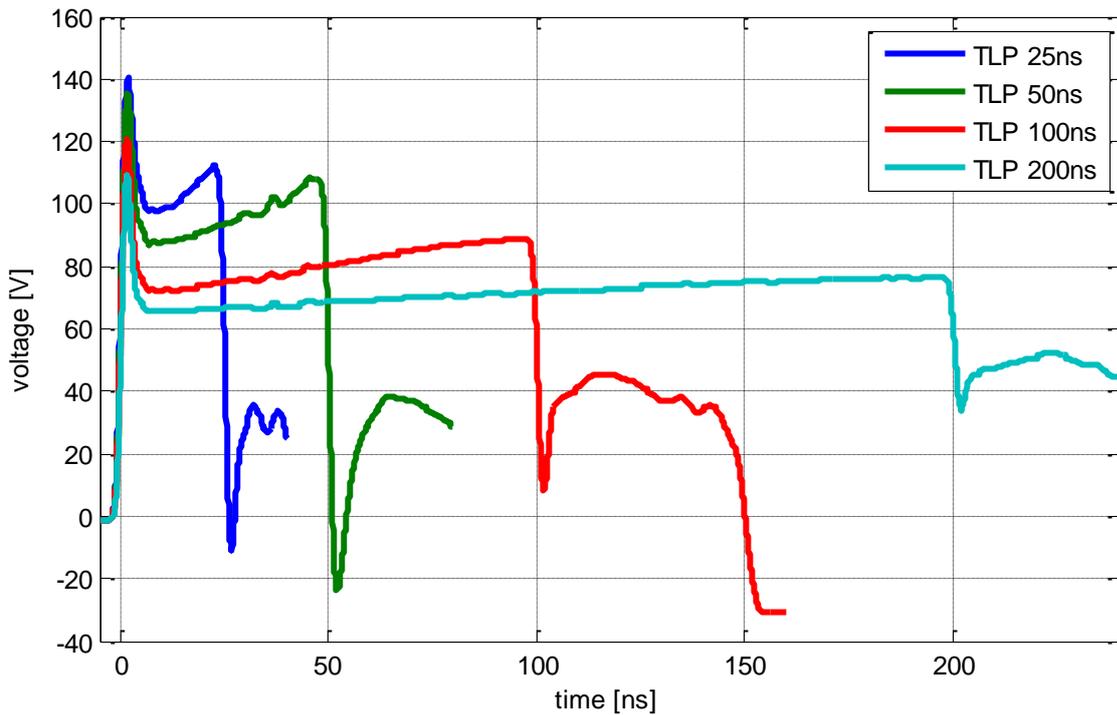


Figure 7.70: Critical positive voltage waveforms for different pulse widths at BUS pin

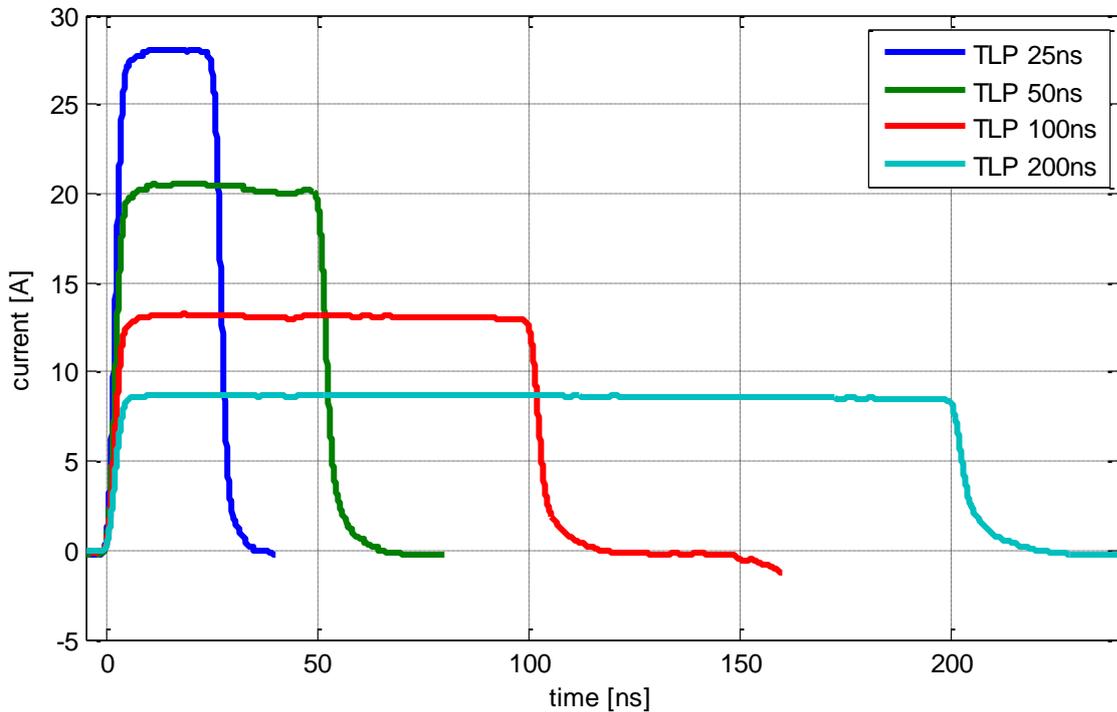


Figure 7.71: Critical positive current waveforms for different pulse widths at BUS pin

All measured amplitudes for critical positive TLP voltages are listed in Table 7.12. Maximum charging voltage was 1480 V where a peak voltage of 140 V and a peak current of 28 A were measured. Only a slight rise in critical energy may be noticed

with increasing pulse width. This fact can be explained by heat dissipation before the pulse has decayed. The rise between 50 ns und 200 ns pulses amounts about 25 %.

IC (PIN)	t_{TLP} [ns]	+/-	U_{TLP} [V]	U_{max} [V]	I_{max} [A]	E_{aus} [μ J]
LIN-ATA6662C (BUS)	25	+	1480	140	28	75.60
	50	+	1100	135	20	102.00
	100	+	725	120	13	112.71
	200	+	500	110	8.7	127.84

Table 7.16: Measured parameters with variation of TLP pulse width for BUS pin

Model parameters in frequency domain were measured without additional capacitors connected to the IC pins.

IC (PIN)	$C_{parallel}$	L_{serial}
ATA6662C (BUS)	9.5 pF @ 10 MHz	4.0 nH @ 1 GHz

Table 7.17: Measured values for L_{serial} and $C_{parallel}$ for BUS pin

7.6.5.5 μ C Pins

7.6.5.5.1 Characterization of μ C XC864 DATA

Characterization and modeling results are described for the DATA pin of the XC864 microcontroller in this section. 10 μ F and 100 nF capacitors were soldered in parallel to the VDDP pin during the TLP test as shown in Figure 7.72.

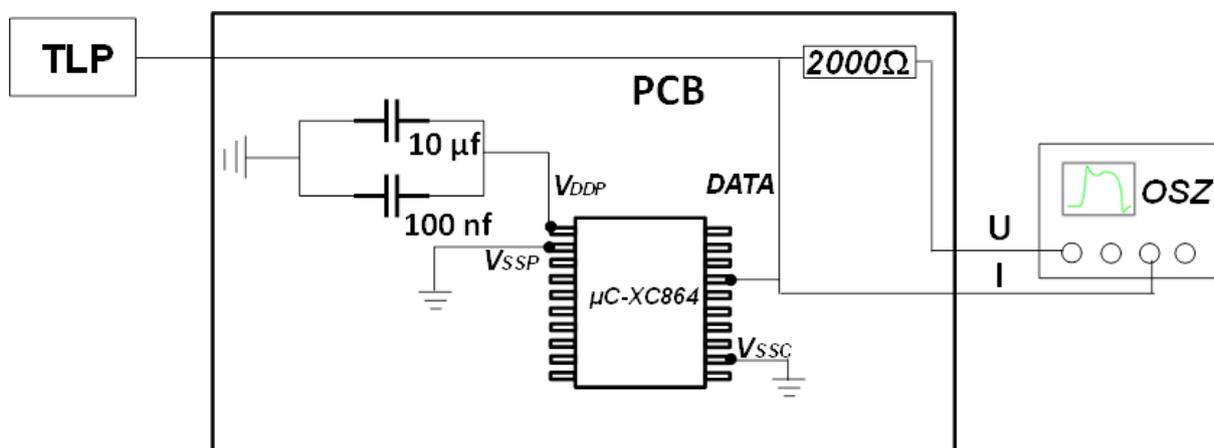


Figure 7.72: Circuit diagram of TLP measurement setup for XC864 DATA pin

Measured IV curves of the DATA pin are compared in Figure 7.73. The pin turns out to be fail at current amplitudes of less than minus 20 A. In comparison to the characteristic of CAN and LIN transceiver pins the failure voltage of the DATA pin is quite low.

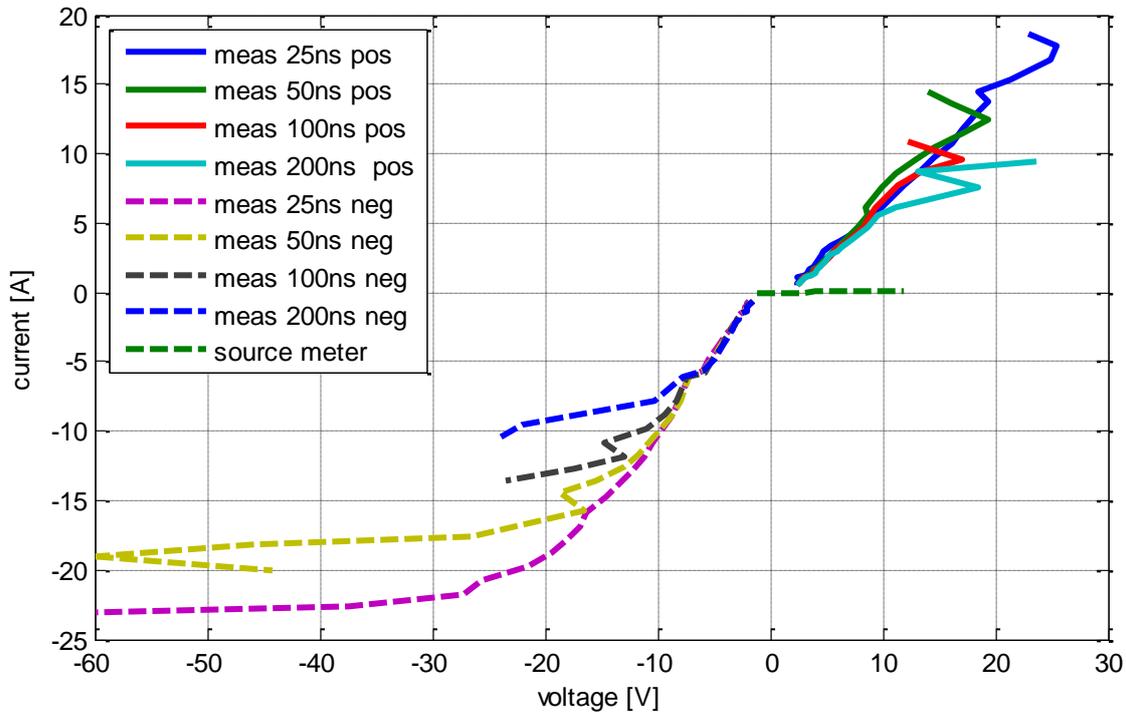


Figure 7.73: Comparison of measured IV-characteristics for DATA pin of μC

In the plots comparing critical voltage over pulse width for positive TLP charging voltages the clamping voltage of all curves is about 20 V. In Figure 7.74 a slight rise of the voltage can be observed with progress of the TLP pulse. This could be caused by heating effects in the current path of the IC.

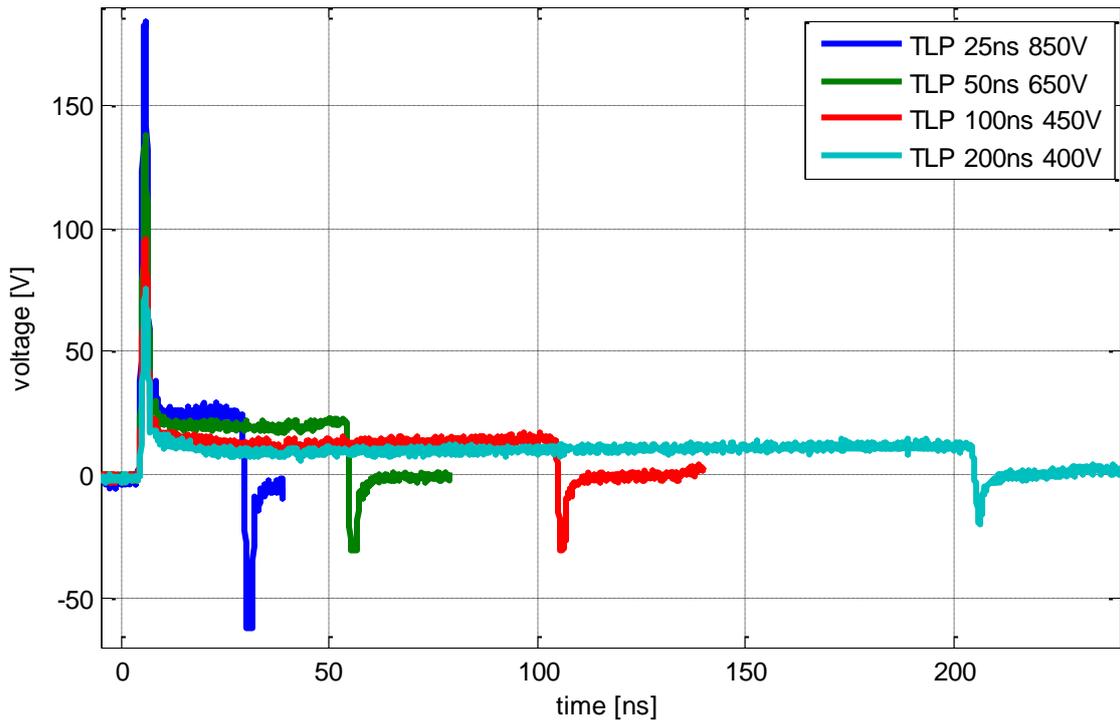


Figure 7.74: Critical positive voltage waveforms for different pulse widths at DATA pin of XC864

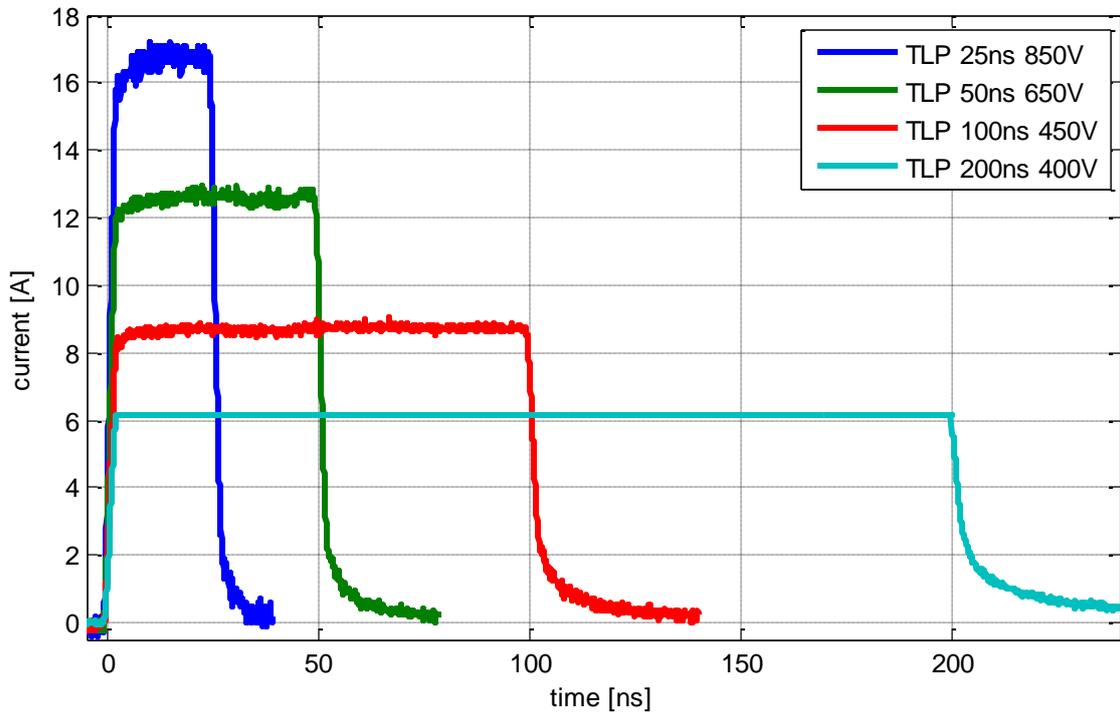


Figure 7.75: Critical positive current waveforms for different pulse widths at DATA pin of XC864

The maximum TLP charging voltage before destruction was 850 V. The highest voltage and current amplitudes of all tested ICs are reached at about 183 V and 17 A. The calculated critical energy from the pulses was found to be very stable.

IC (PIN)	t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [μ J]
μ C-XC864 (DATA)	25	850	183.7	17.2	24.9	16.7	12.7
	50	650	138.1	12.9	19.3	12.5	13.9
	100	450	95.4	9.0	13.5	8.7	12.3
	200	400	75.2	6.1	11.1	6.1	13.3

Table 7.18: Measured parameters with variation of TLP pulse width for μ C DATA pin

$C_{parallel}$ and $L_{parallel}$ are set to 7,6 pF and 9,2 nH in the model.

IC (PIN)	$C_{parallel}$	L_{serial}
XC864 (DATA)	7,6 pF @ 10 MHz	9,2 nH @ 1,2 GHz

Table 7.19: Measured values L_{serial} and $C_{parallel}$ for XC864 μ C

7.6.5.5.2 Characterization of μ C XC864 VAREF

TLP test setup is identical to Figure 7.72, instead of DATA the VAREF pin is processed.

All measured IV curves are shown in Figure 7.62. For currents below 5 A and positive TLP voltage the curves overlay. The same may be observed for negative polarity. Similar to the characteristic of DATA pin the failure voltage of the VAREF pin is quite low compared to the characteristic of CAN and LIN transceiver pins.

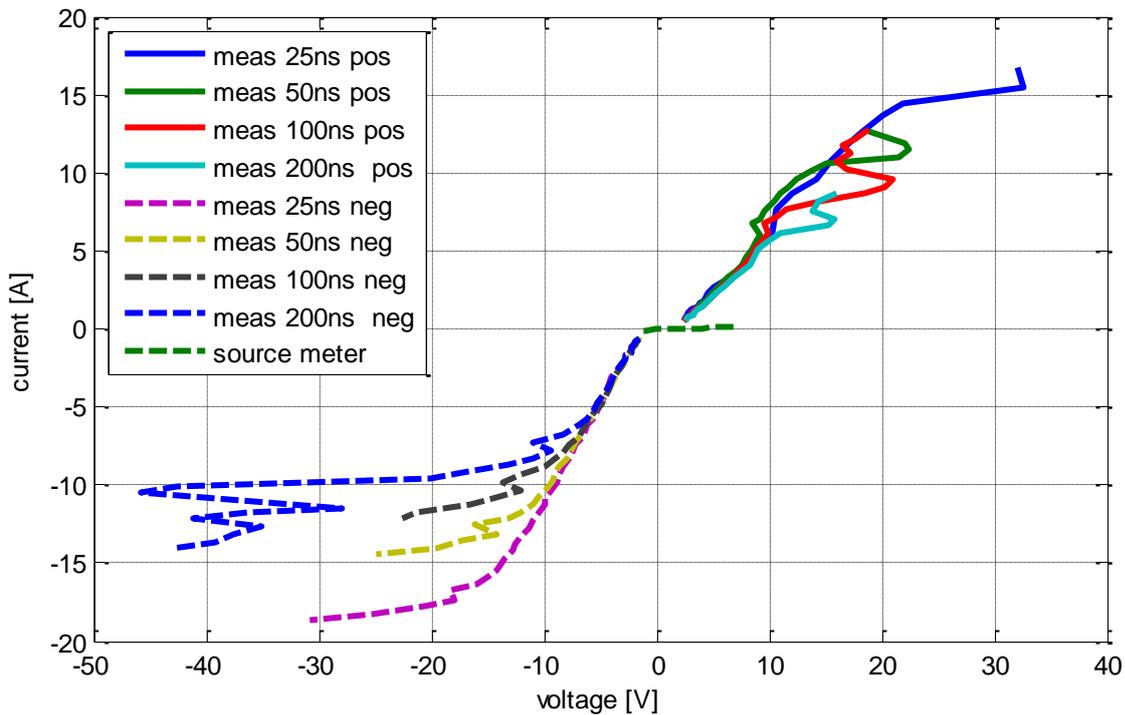


Figure 7.76: Comparison of measured IV-characteristics for VAREF pin

A positive clamping voltage of about 20 V may be noticed in Figure 7.77 for all pulse widths. For 25 ns and 50 ns TLP pulses the initial voltage peak is followed by rise of the voltage with progress of the TLP pulse. The rise of the 25 ns pulse is from 22 A to 28 A. This could be caused by heating effects in the IC's current path. High initial voltage peaks are measured. 200 ns pulse has the least charge TLP voltage; however the initial peak is about four times higher than clamping voltage. All amplitude details are listed in Table 7.20. Current remain at the same level over the respective pulse width (see Figure 7.78).

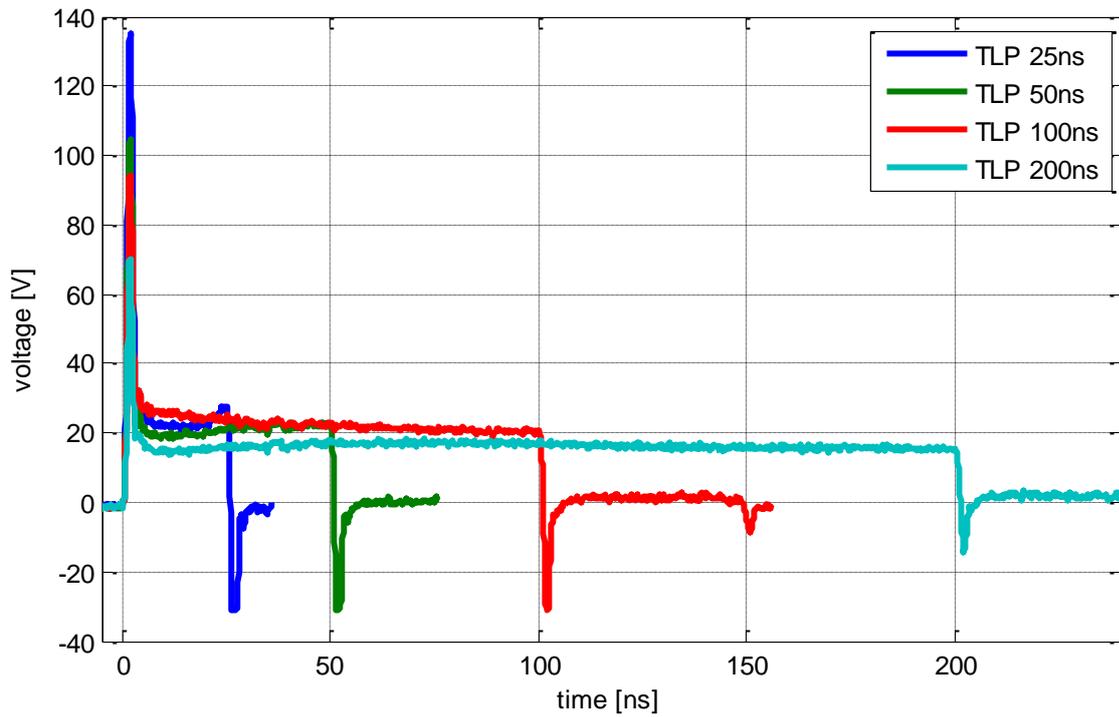


Figure 7.77: Critical positive voltage waveforms for different pulse widths at VAREF pin

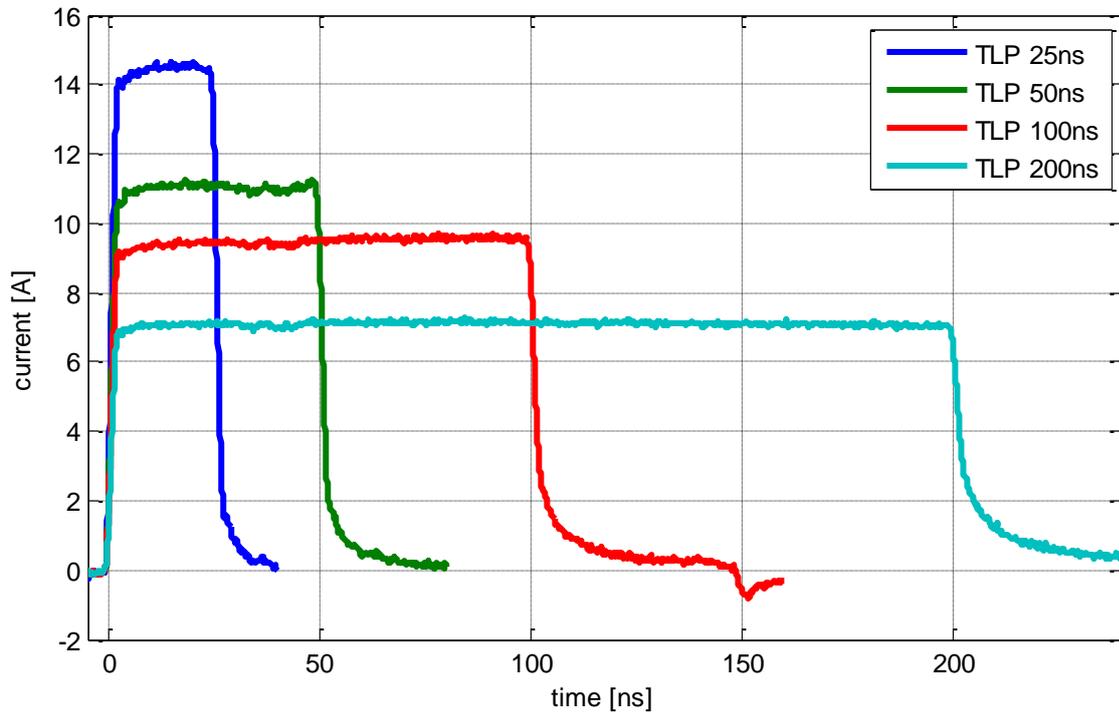


Figure 7.78: Critical positive current waveforms for different pulse widths at VAREF pin

The deviation in critical energy for 100 ns and 200 ns pulses is only about 10 %. The failure mechanism is supposed to be energy-based.

IC (PIN)	t_{TLP} [ns]	+/-	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	E_{crit} [μ J]
μ C-XC864 (VAREF)	25	+	750	136	14.8	7.90
	50	+	575	106	11	11.88
	100	+	500	95	9.8	20.16
	200	+	375	71	7.4	22.44

Table 7.20: Measured parameters with variation of TLP pulse width for VAREF pin

All parallel IC-capacitances C and serial IC-package-inductances L for modeling were measured with a network analyzer without a bias voltage. Table 7.15 contains the results for μ C XC864 VAREF pin. Measurement data in frequency domain was measured without additional capacitors connected to the IC pins.

IC (PIN)	$C_{parallel}$	L_{serial}
XC864 (VAREF)	7.6 pF @ 10 MHz	9.4 nH @ 1 GHz

Table 7.21: Measured values for L_{serial} and $C_{parallel}$ for VAREF

7.6.5.6 Diodes

7.6.5.6.1 Diode BAW156

BAW156 is a low-leakage double diode. A symmetrical construction of the double diode is assumed, thus only one side was characterized. TLP-test-PCB for LIN and CAN transceivers (Figure 7.48) is used for characterization of the diode.

The overlaying TLP IV curves of the diode in reverse direction and the source meter IV curve are shown in Figure 7.79. Leakage current was measured for positive and negative voltage. Breakdown voltage can be specified at 120 V. The device can be destroyed using 25 ns, 50 ns, 100 ns and 200 ns pulse width. Apart from the leakage current measurement, destruction is indicated by a significant voltage drop.

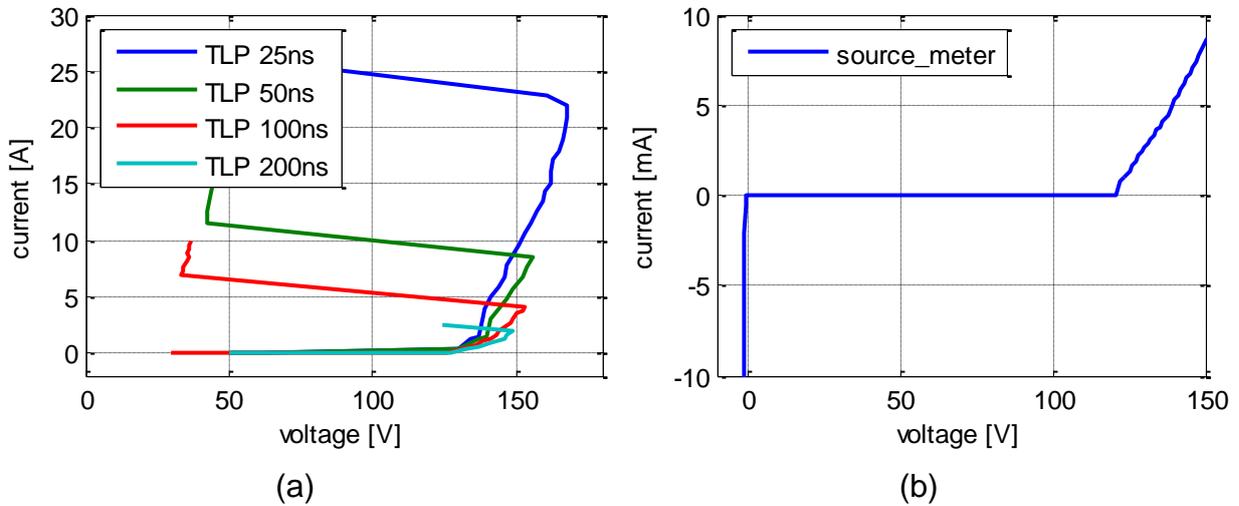


Figure 7.79: Comparison of measured IV-characteristics for BAW 157 diode with TLP (a) and source meter (b)

Figure 7.80 show the critical waveforms for positive TLP charging voltages. The initial voltage peak is followed by rise of the voltage with progress of the TLP pulse. This could be caused by heating effects in the IC's current path. The current remains at the same level over the pulse width.

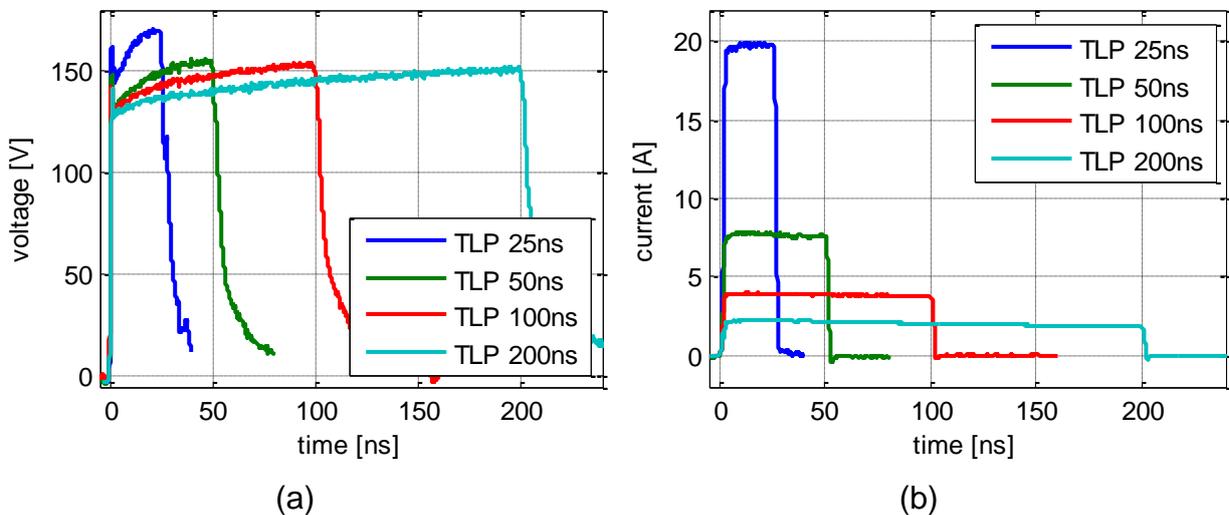


Figure 7.80: Critical positive voltage (a) and current (b) waveforms for different pulse widths at BAW 156 diode

Table 7.22 summarizes all measured amplitudes for the critical TLP charging voltage considering the last measured waveform before destruction. Critical energy is calculated from voltage and current curves for the selected pulse widths. The maximum TLP charging voltage before destruction is 1200 V.

The highest clamping voltage and current amplitudes of all tested devices are 172 V and 22 A. The calculated critical energy from the pulses was found to be stable for all

pulse width settings except the 25 ns pulse. Thus the failure mechanism is supposed to be energy based.

t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [μ J]
25	1200	172	20.2	168	21.9	78.7
50	550	160	8.1	154	7.6	56.4
100	350	157	4.05	152	3.8	56.6
200	250	155	2.3	149	1.9	58.7

Table 7.22: Measured parameters with variation of TLP pulse width for BAW 157 diode

7.6.5.6.2 Rear light LED

Rear light LED in SMD package is characterized. TLP-test-PCB for LIN and CAN transceivers (Figure 7.48) is used for characterization of the diode. The overlaying TLP IV curves of the diode in forward and reverse direction and the source meter IV curve are shown in Figure 7.81. Leakage current was measured for positive and negative voltage. Breakdown voltage can be specified at 55 V. The device can be destroyed using 25 ns, 50 ns, 100 ns and 200 ns pulse width. Apart from the leakage current measurement, destruction is indicated by a significant voltage drop for characterization in reverse direction.

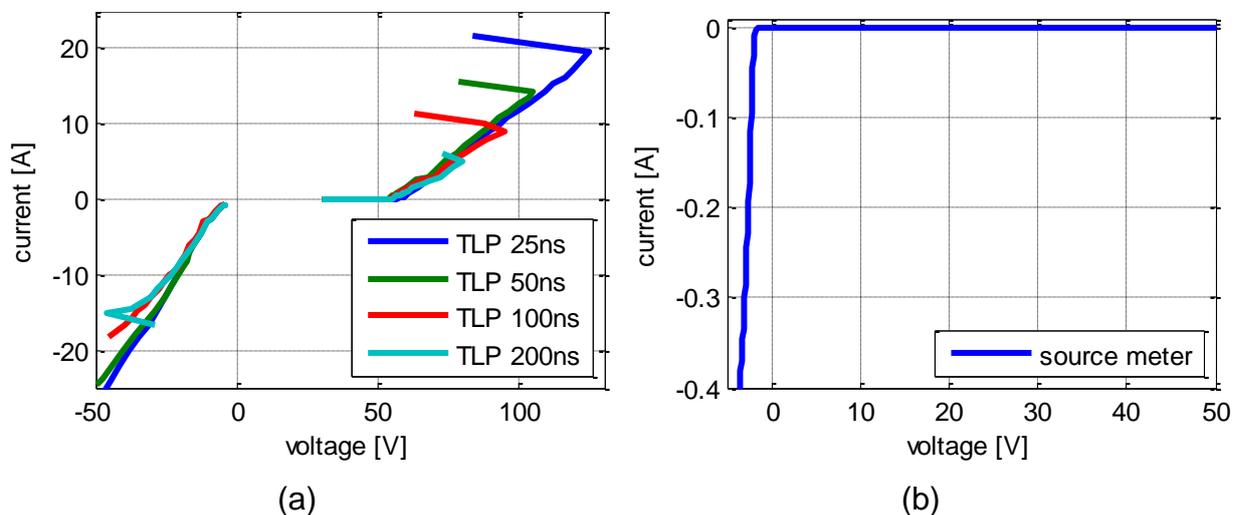


Figure 7.81: Comparison of measured IV-characteristics for BAW 157 diode with TLP (a) and source meter (b)

Figure 7.82 show the critical waveforms for positive TLP charging voltages. The initial voltage peak is followed by rise of the voltage with progress of the TLP pulse. This could be caused by heating effects in the IC's current path. The current remains at the same level over the pulse width. The highest clamping voltage and current amplitudes of all tested devices are 119 V and 17 A. The calculated critical energy

from the pulses was found to be stable for 100 ns and 200 ns pulses. Thus the failure mechanism is supposed to be energy based.

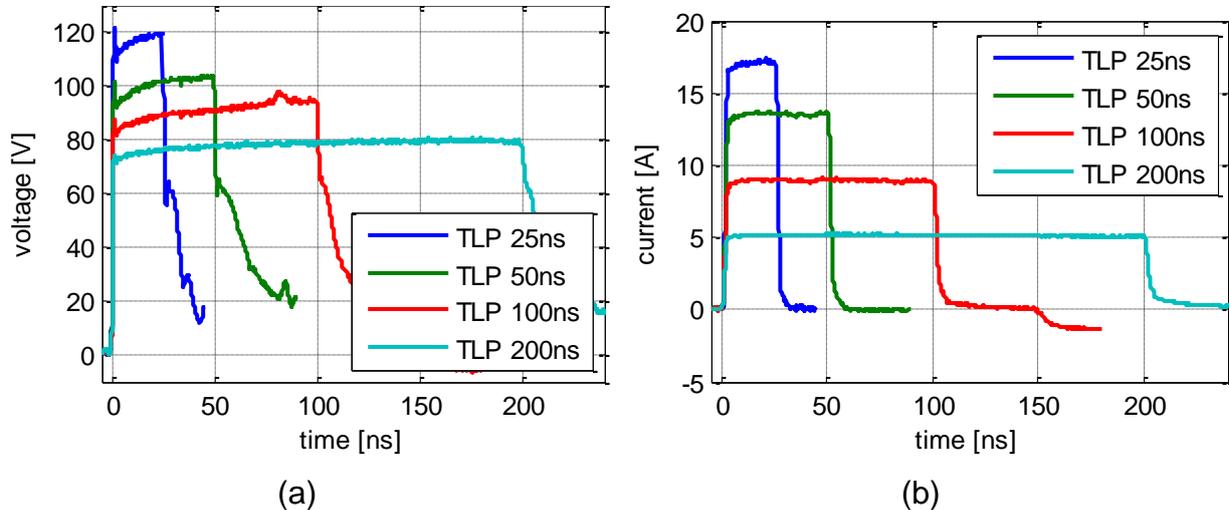


Figure 7.82: Critical positive voltage (a) and current (b) waveforms for different pulse widths at BAW156 diode

Table 7.23 summarizes all measured amplitudes for the critical TLP charging voltage considering the last measured waveform before destruction. Critical energy is calculated from voltage and current curves for the selected pulse widths. The maximum TLP charging voltage before destruction is 1000 V.

t_{TLP} [ns]	V_{TLP} [V]	V_{max} [V]	I_{max} [A]	V_{mean} [V]	I_{mean} [A]	E_{crit} [μ J]
25	1000	123	17	119	17	48
50	800	105	14	103	13	67
100	550	99	9	94	9	81
200	350	83	5	79	5	81

Table 7.23: Measured parameters with variation of TLP pulse width for rearlight LED

7.6.6 Model Verification

7.6.6.1 Measurement and Simulation Setup for Verification of IC Models

7.6.6.1.1 Setup TLP board

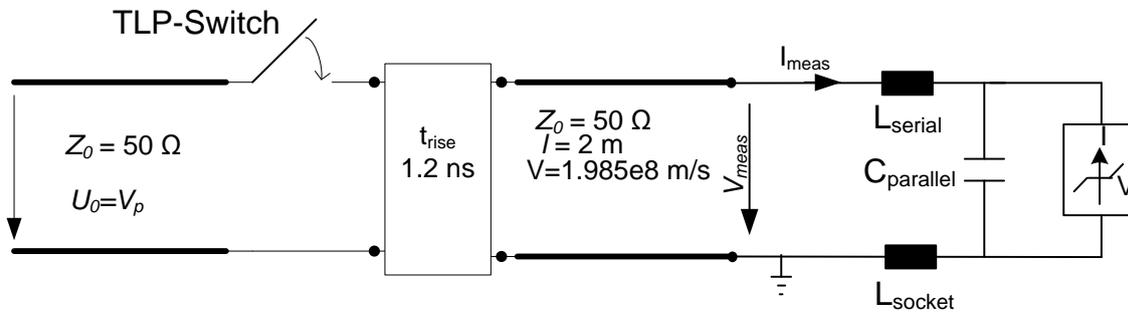


Figure 7.83: Setup for verification of measured data by simulation

7.6.6.1.2 Measurement of IEC Robustness on Demonstrator PCB

Different IC pins were characterized using the TLP setup. IC models were implemented in the electrical and thermal domain from the characterization data. In this section the simulated failure behavior is compared to measurement using the IEC ESD generator and the demonstrator PCB. Three discharges within 3 s were performed per voltage level. To avoid pre-damaging effects a new IC was used for each voltage level. Three ICs were tested with increasing voltages until a significant rise in the current consumption could be measured. The minimum step of charging voltage was 0,5 kV.

For testing the ESD robustness of IC pins on system level the ESD generator is discharged via the connector pin of the demonstrator PCB. Figure 7.84 gives an overview of the setup. The discharge current through a short additional wire soldered in the PCB current path was measured with a CT1 or CT6 current sensor and an oscilloscope. The setup is shown in Figure 7.85. During discharge the IV source meter was not connected. For additional investigations ESD protection elements were connected parallel to PCB pads close to the connector pin. The ESD pulse propagates through a 10 cm transmission line to the IC pin. In this case the conductor was modeled as a single transmission line. The impedance can be calculated using a microstrip configuration e.g. in the program TXLINE. For the adjusted parameters shown in Figure 7.86 the line impedance in the simulation model was set to 83 Ω .

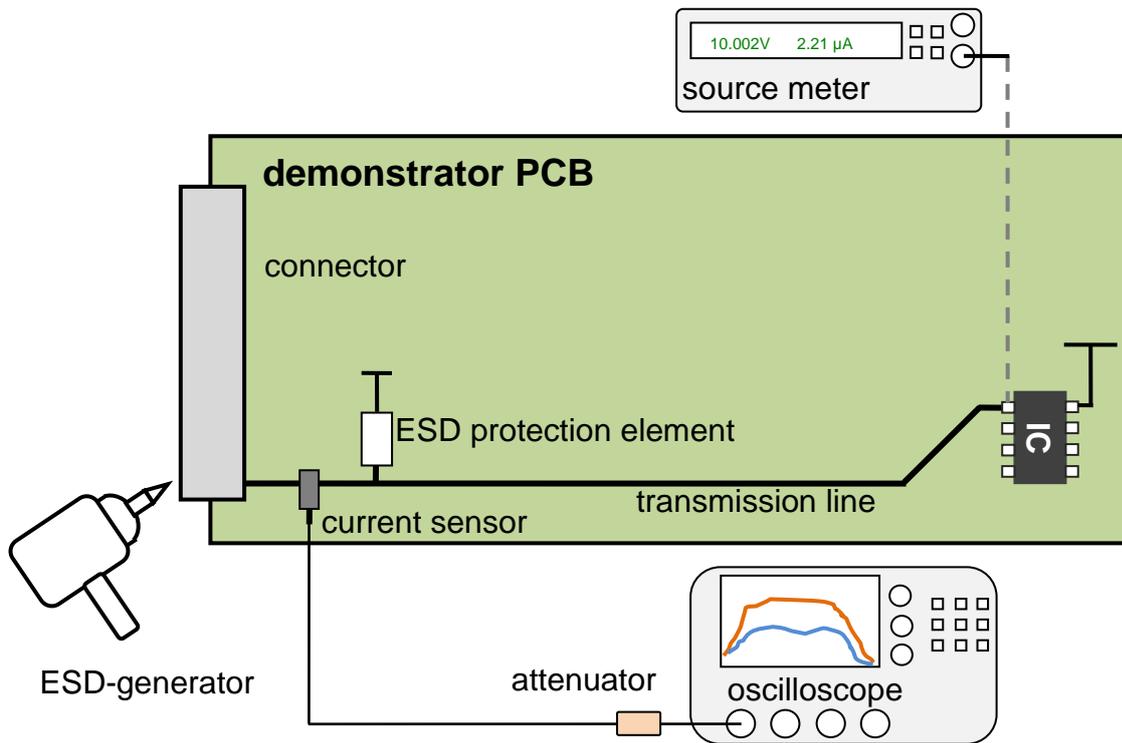


Figure 7.84: Measurement setup with IC

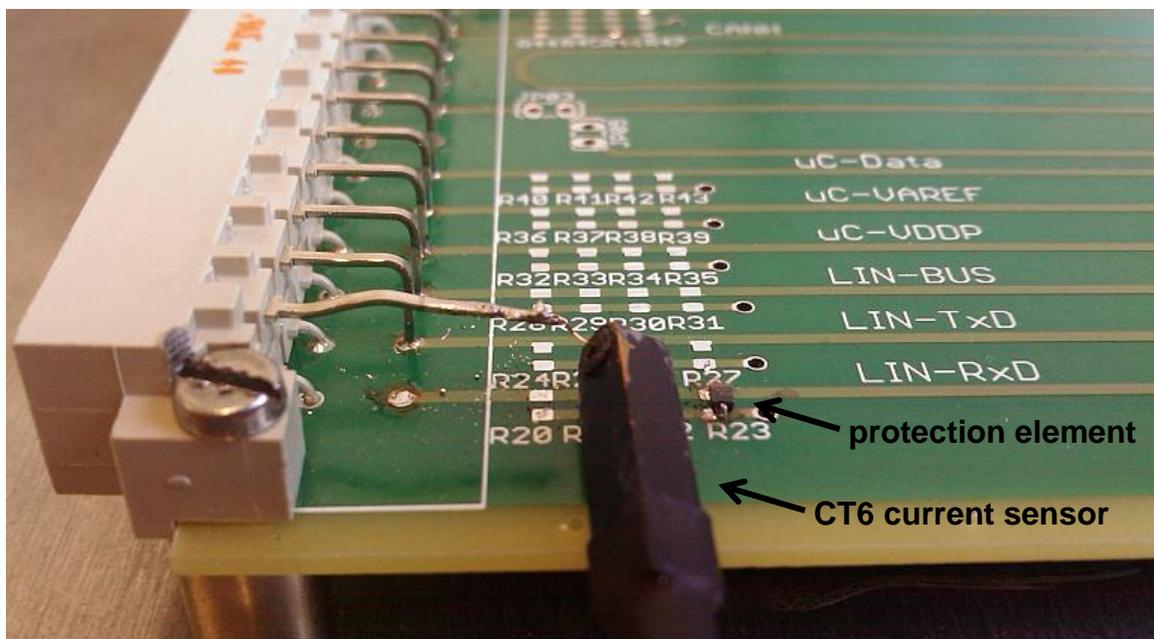


Figure 7.85: Demonstrator PCB with CT6 current sensor

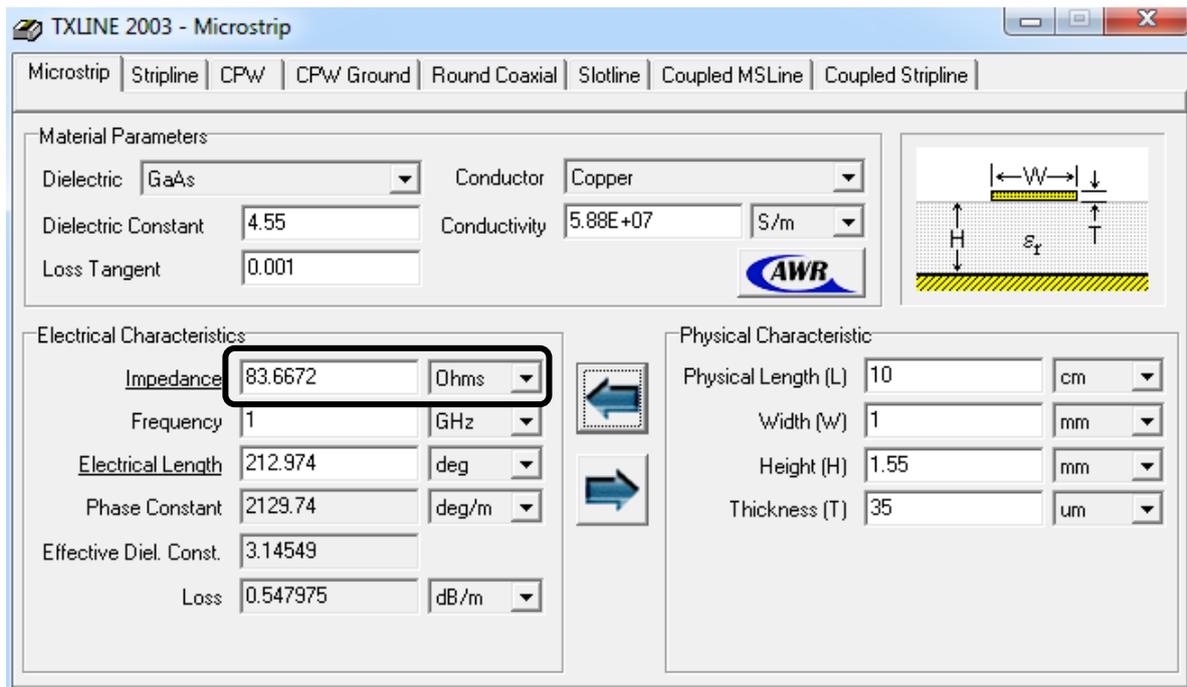


Figure 7.86: Calculation of stripline impedance with TXLINE

The equivalent simulated circuit is shown in Figure 7.87. The effect of the connector on the current shape was modeled by a 2 nH inductor and a parallel 1 pF capacitor. Similar to the TLP setup the IC socket inductance was included in the ground path of the IC. I_{sim} is the simulated discharge current through the connector. I_{IC} and V_{IC} are simulated current and voltage shapes at the IC pin which will be compared to measured amplitudes obtained with the TLP setup.

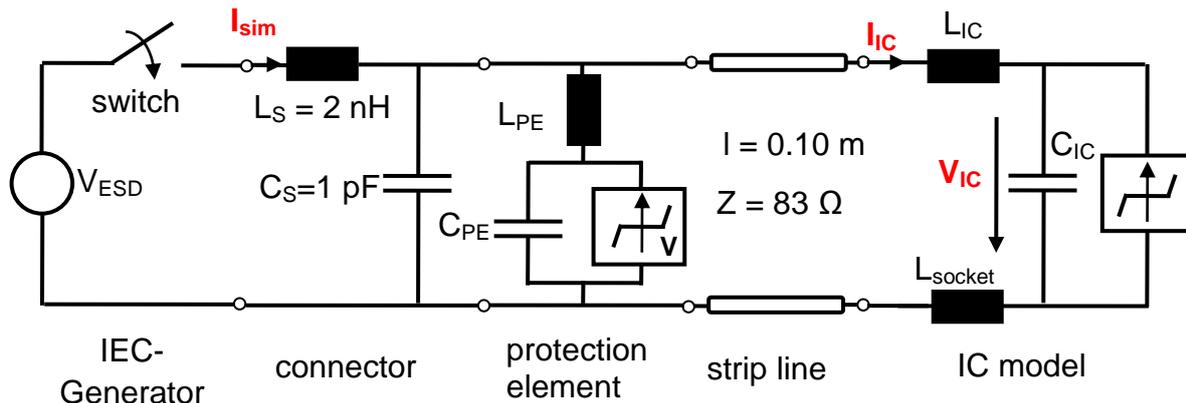


Figure 7.87: Equivalent simulation setup

7.6.6.2 Verification of CAN Transceiver Models

7.6.6.2.1 Verification of CAN Transceiver TJA1041T CANH Model

In Figure 7.88 measurement results and a simulated IV curve of the CANH pin are compared. Good matching can be obtained for positive and negative TLP charging voltages. The corresponding TLP simulation for 100 ns pulse width can be found in Figure 7.89 and Figure 7.90. L_{socket} was set to 18 nH.

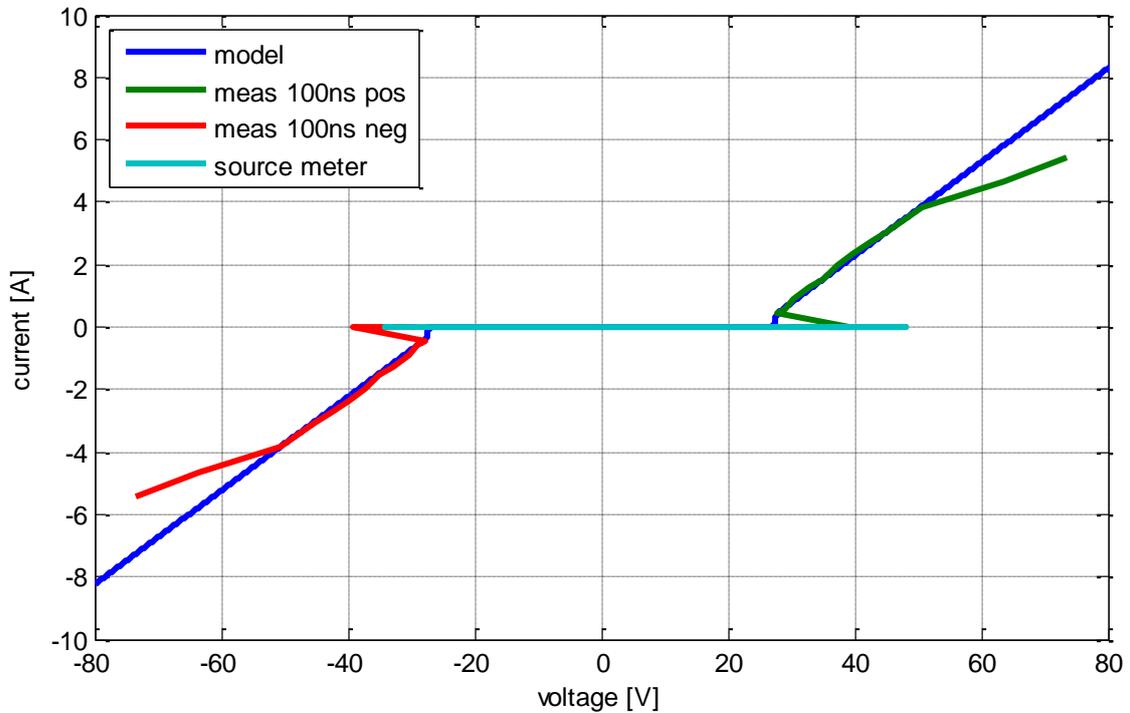


Figure 7.88: Comparison of measured and implemented IV-curves of TJA1041T CANH pin

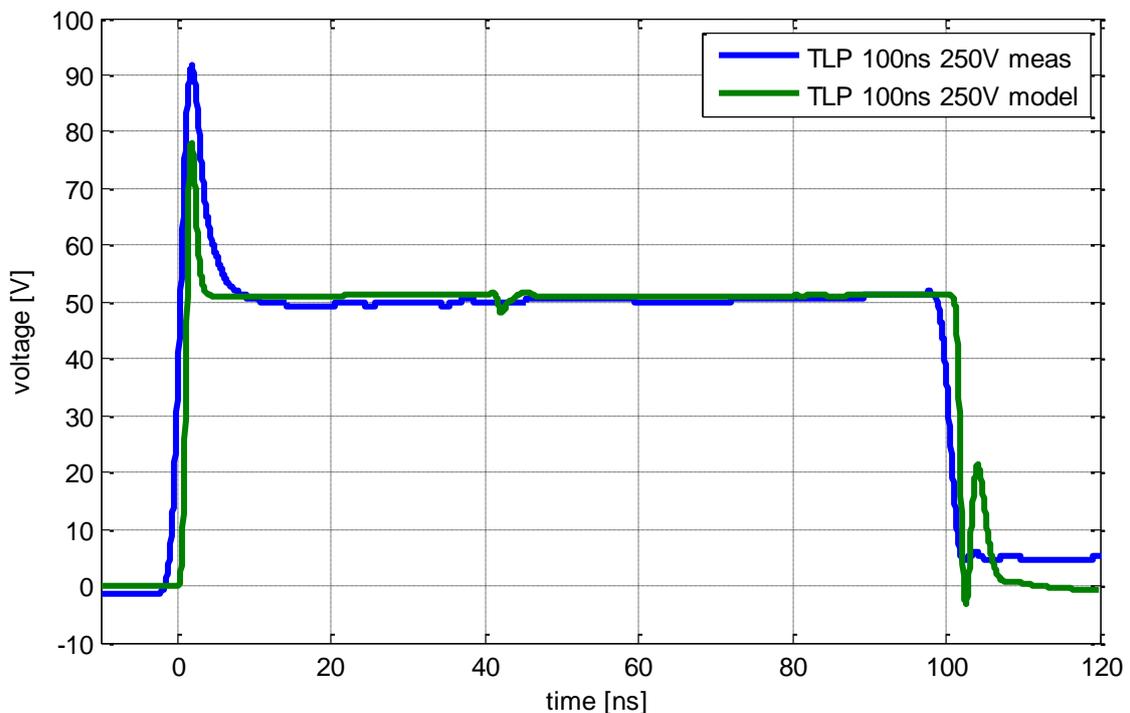


Figure 7.89: Comparison of measured and simulated critical voltage at TJA1041T CANH pin

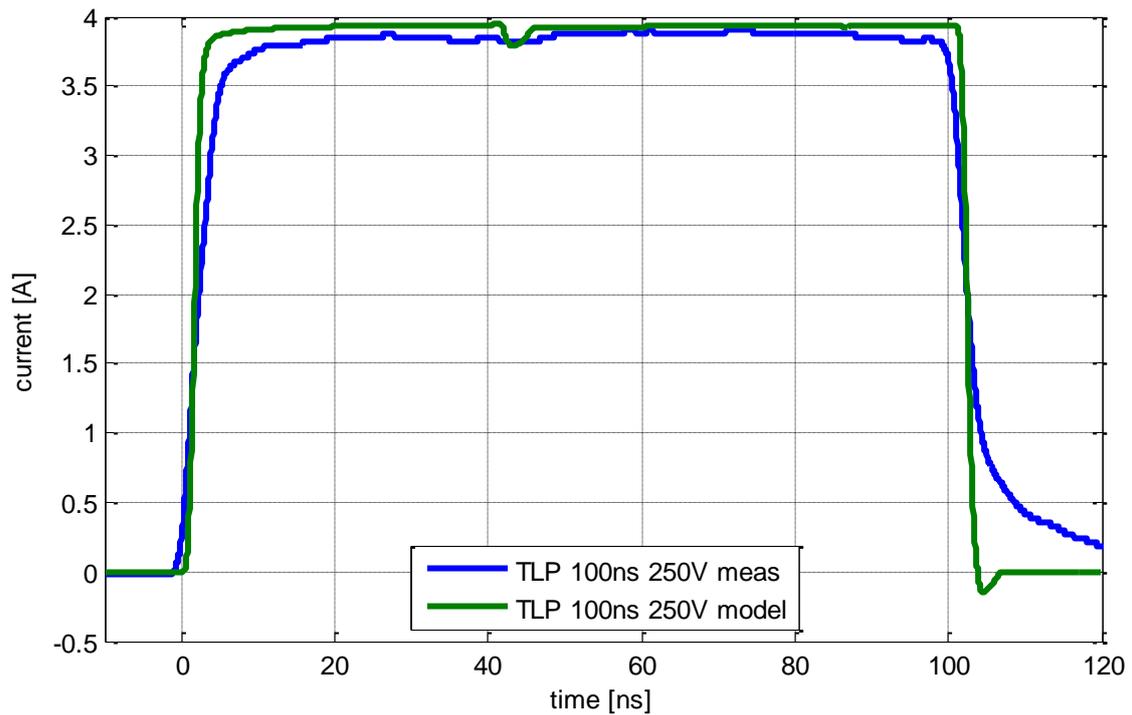


Figure 7.90: Comparison of measured and simulated critical current at TJA1041T CANH pin

The simulated and measured current waveforms for IEC discharges via the CANH pin on the demonstrator PCB are shown in Figure 7.91. The charging voltage causing IC destruction was 2,5 kV. In the measurement data the high pass characteristics and saturation effects of the CT6 current sensor can be observed after 50 ns.

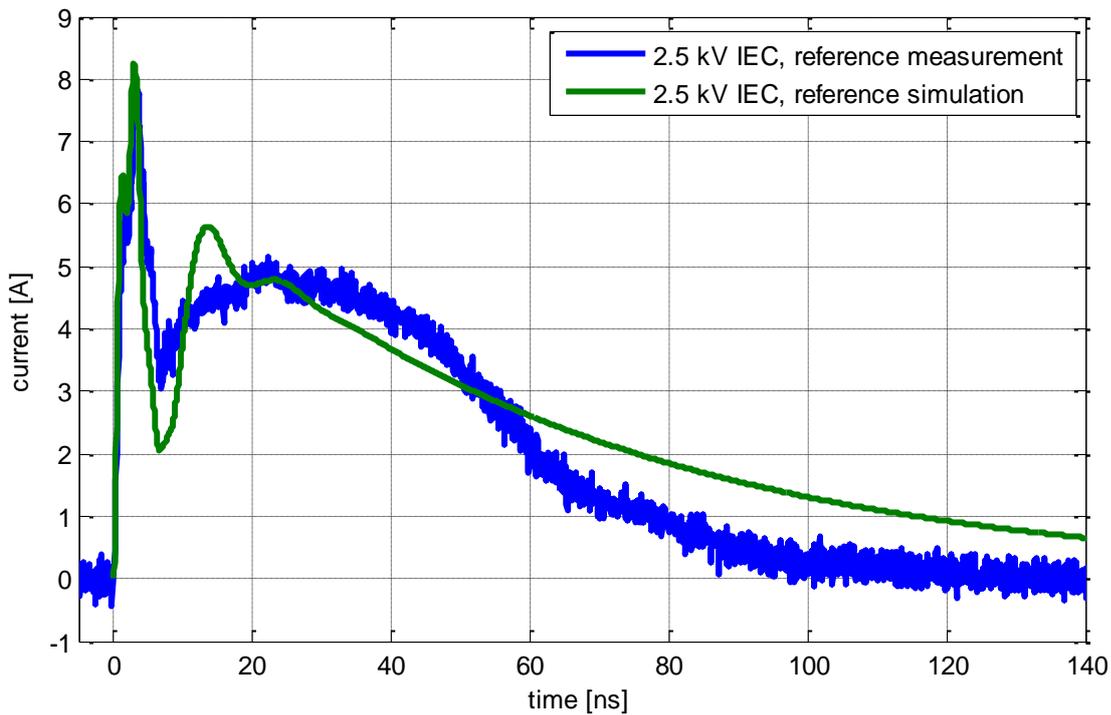


Figure 7.91: Simulated and measured current for TJA1041T CANH pin at connector of demonstrator PCB

The simulated voltage and current for the IEC discharge are compared to TLP measurement data in Figure 7.92 and Figure 7.93. Peak amplitudes of over 120 V and about 7,5 A were measured for 450 V charging voltage and 25 ns pulse width. The voltage peak at the IC pin is about 100 V in case of IEC discharges.

The comparison of the calculated failure energies underlines the assumption that the IC failure due to TLP and IEC discharges is energy-based. The deviation is about 10 %.

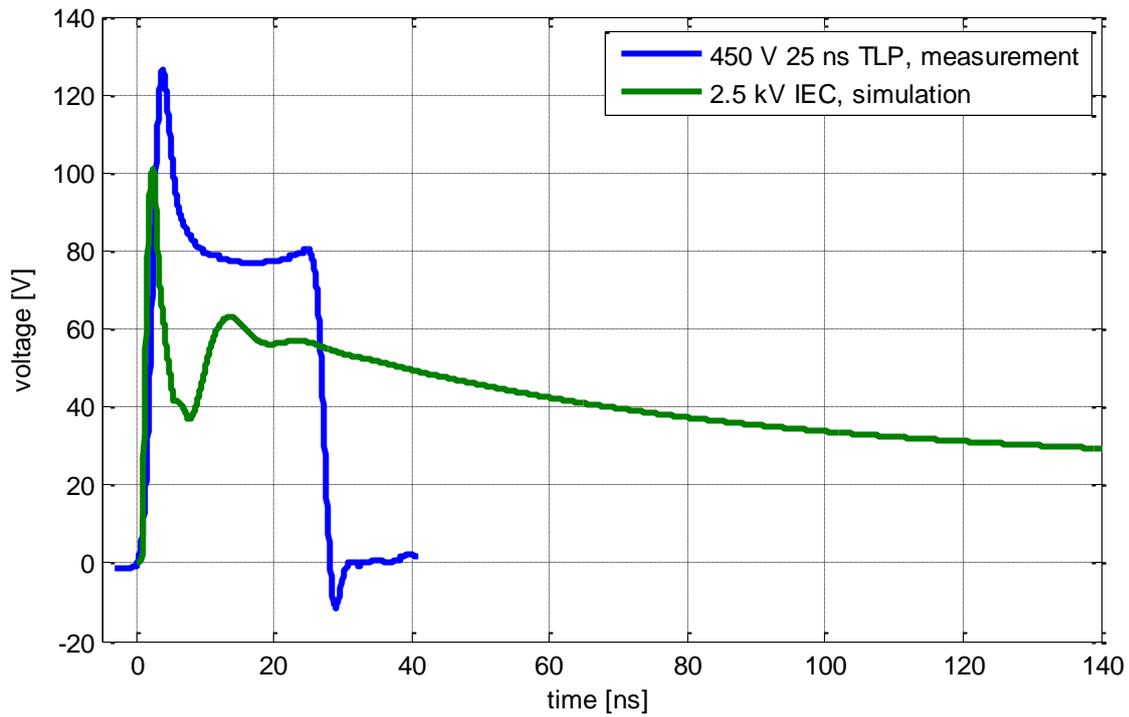


Figure 7.92: Maximum TLP voltage and IEC generator voltage at TJA1041T CANH pin

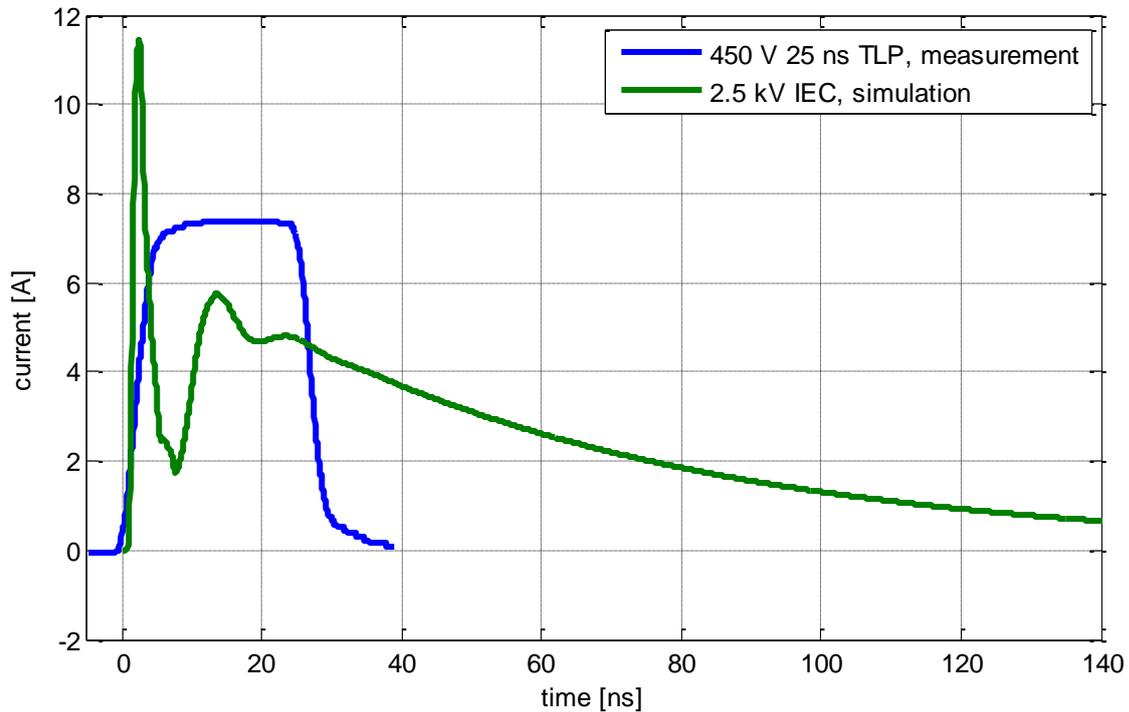


Figure 7.93: Maximum TLP current and IEC generator current at TJA1041T CANH pin

ESD pulse	V_{ESD} [V]	$V_{IC,max}$ [V]	$I_{IC,max}$ [A]	E_{fail} [μ J]	Deviation [%]
IEC NoiseKen	2500	100.86	11.44	17.5	9
TLP 100 ns	250	91.8	3.9	19.2	0

Table 7.24: Comparison of IEC and TLP failure energies for TJA1041T CANH pin

7.6.6.2.2 Verification of CAN Transceiver TLE6251G CANH Model

In Figure 7.94 measurement results and a simulated IV curve of the TLE6251G CANH pin are compared. Good matching can be obtained for positive and negative TLP charging voltages. The corresponding TLP simulation for 100 ns pulse width can be found in Figure 7.95 and Figure 7.96. L_{socket} was set to 18 nH.

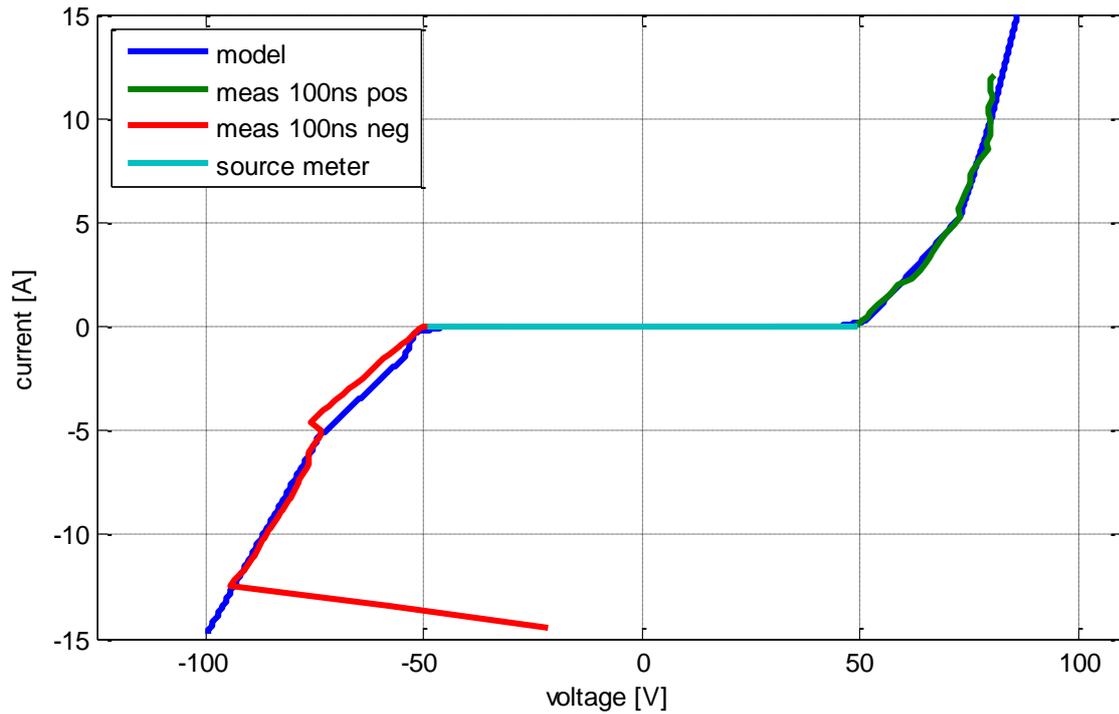


Figure 7.94: Comparison measured and simulated IV curve (TLP 100 ns)

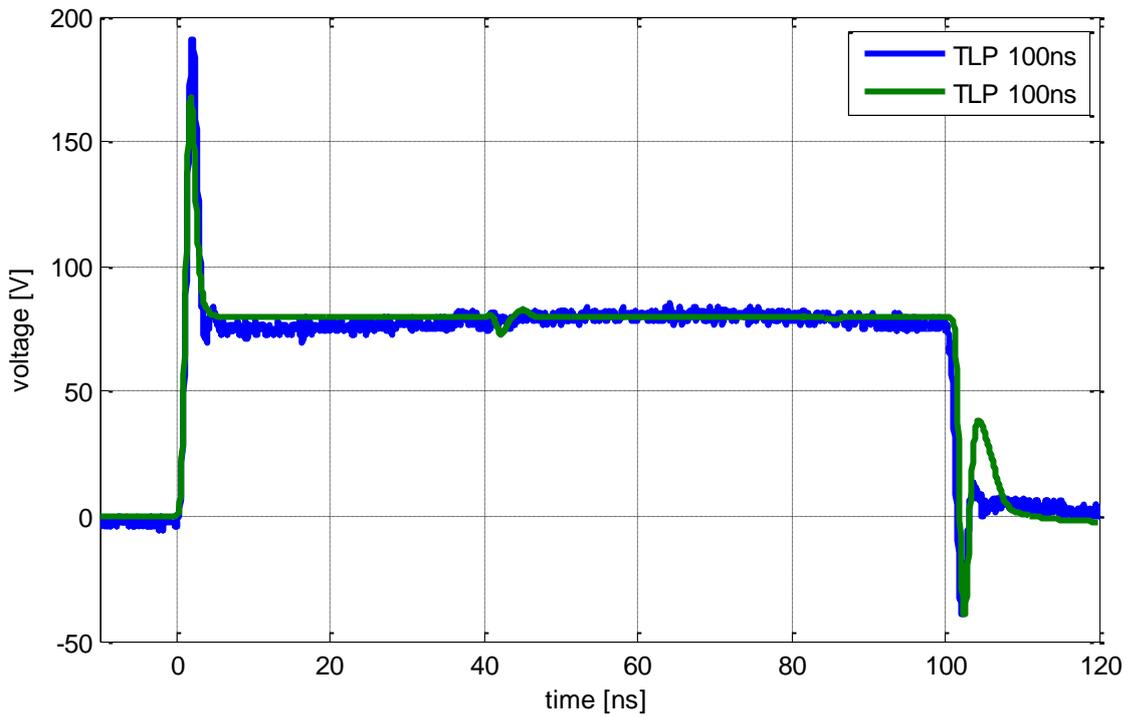


Figure 7.95: Comparison of measured and simulated critical voltage at TLE6251G CANH pin

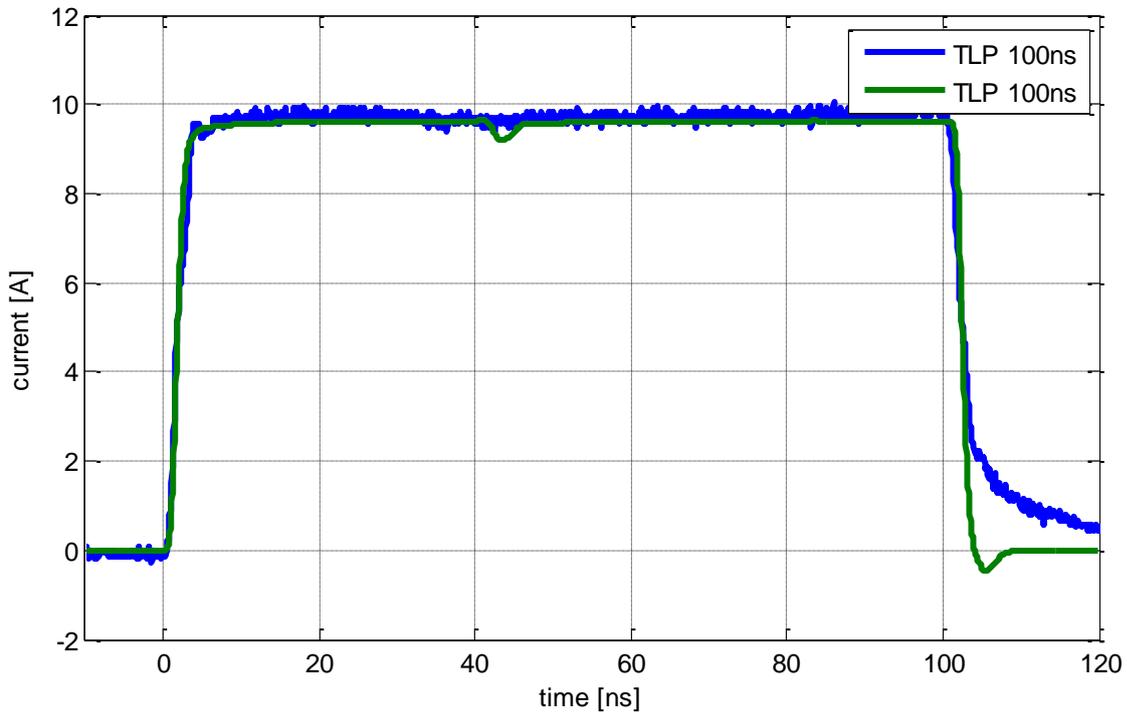


Figure 7.96: Comparison of measured and simulated critical voltage at TLE6251G CANH pin

The current waveform for IEC discharges via the CANH pin on the demonstrator PCB is not measured. The critical IEC voltage was 12 kV and a damage of the CT6 current sensor is very likely. Figure 7.97 and Figure 7.98 compare the simulated waveforms

of a 12 kV IEC discharge to the 1480 V, 25 ns TLP measurement. No IC failure could be detected for a 25 ns discharge.

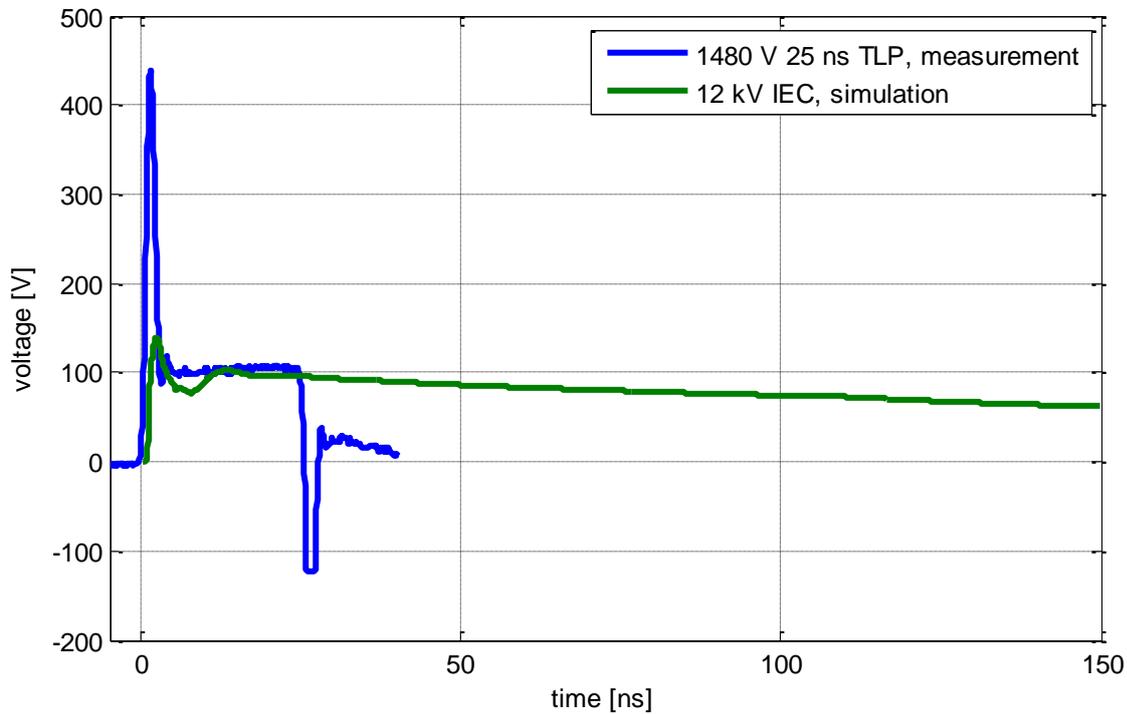


Figure 7.97: Maximum TLP voltage and IEC generator voltage at TJA1041T CANH pin

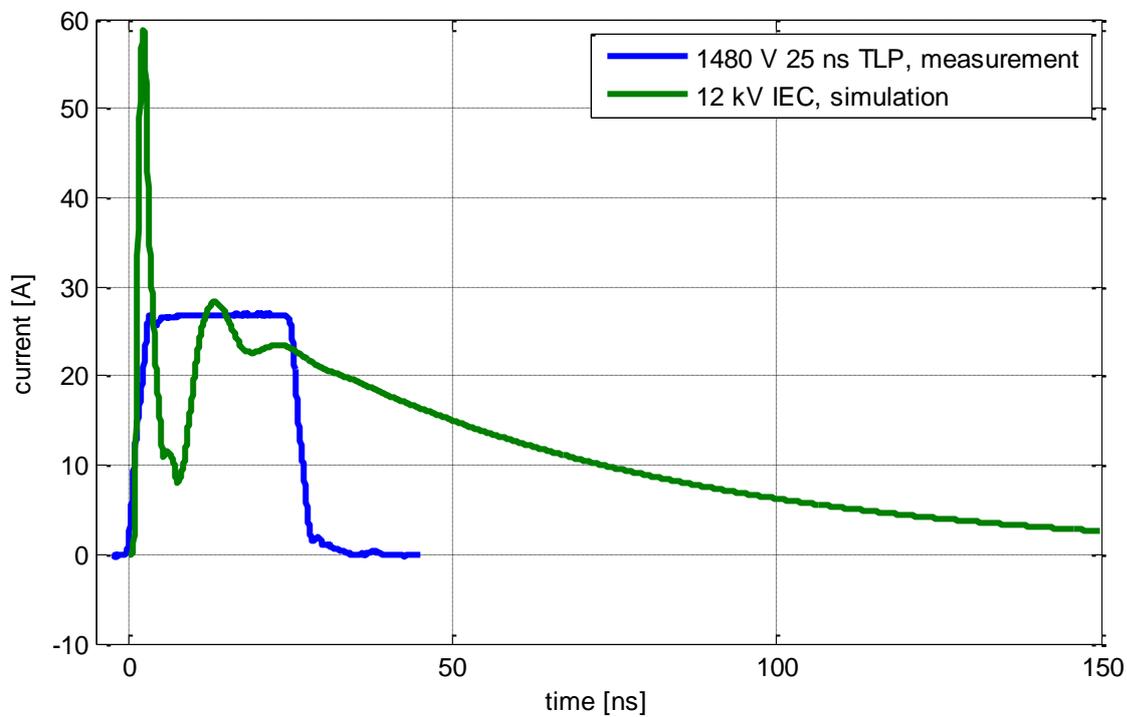


Figure 7.98: Maximum TLP current and IEC generator current at TLE6251 CANH pin

All measured amplitudes are compared in Table 7.25. The energy based failure mechanism could not be stated, because of the differences between failure energies

of about 50 %. The on-chip protection structure seems to be more advanced. Further investigations on failure mechanism are required.

ESD pulse	V _{ESD} [V]	V _{IC,max} [V]	I _{IC,max} [A]	E _{fail} [μJ]
IEC NoiseKen	12000	140	59	154
TLP 100 ns	565	190.9	10	77.31
TLP 25 ns*	1480*	439.6*	27.6*	69.94*

Table 7.25: Comparison of IEC and TLP failure energies for TLE6251G CANH pin (* = no IC failure could be detected)

7.6.6.2.3 Verification of CAN Transceiver TLE6251G Split Model

Measurement results and a simulated IV curve of the SPLIT pin are compared in Figure 7.99. Good matching can be obtained for positive and negative TLP charging voltages. The corresponding critical TLP simulation for 100 ns pulse width can be found in Figure 7.100 and Figure 7.101. IC socket inductance L_{socket} is set to 18 nH.

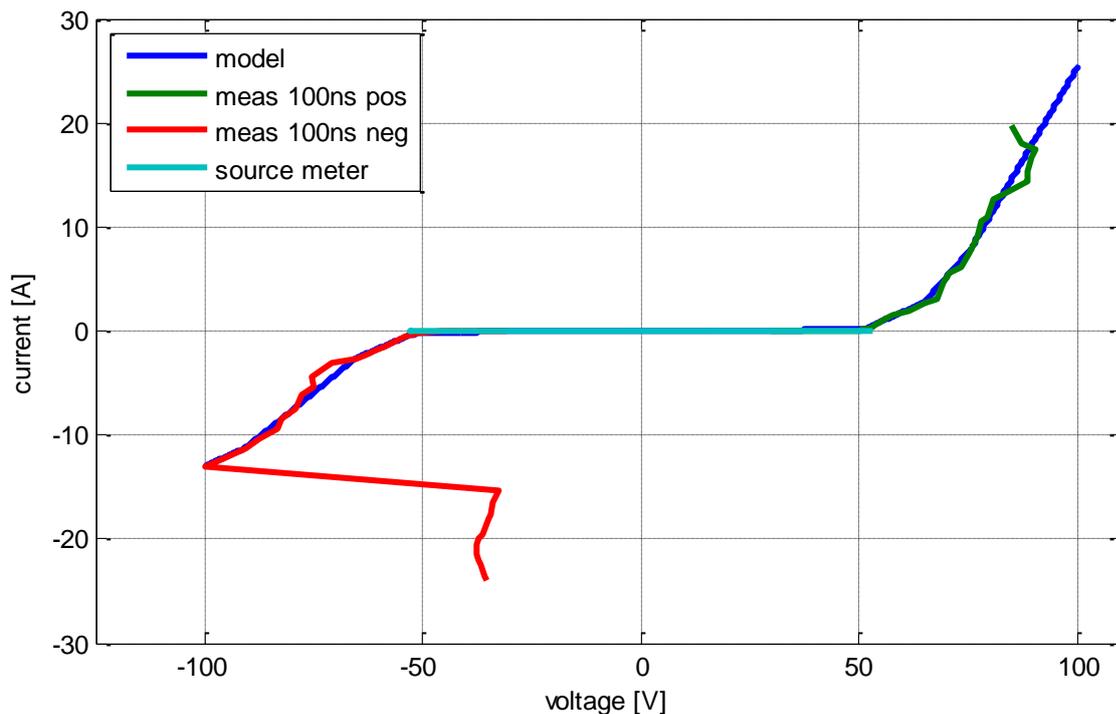


Figure 7.99: Comparison of measured and implemented IV-curves of TLE6251G Split pin

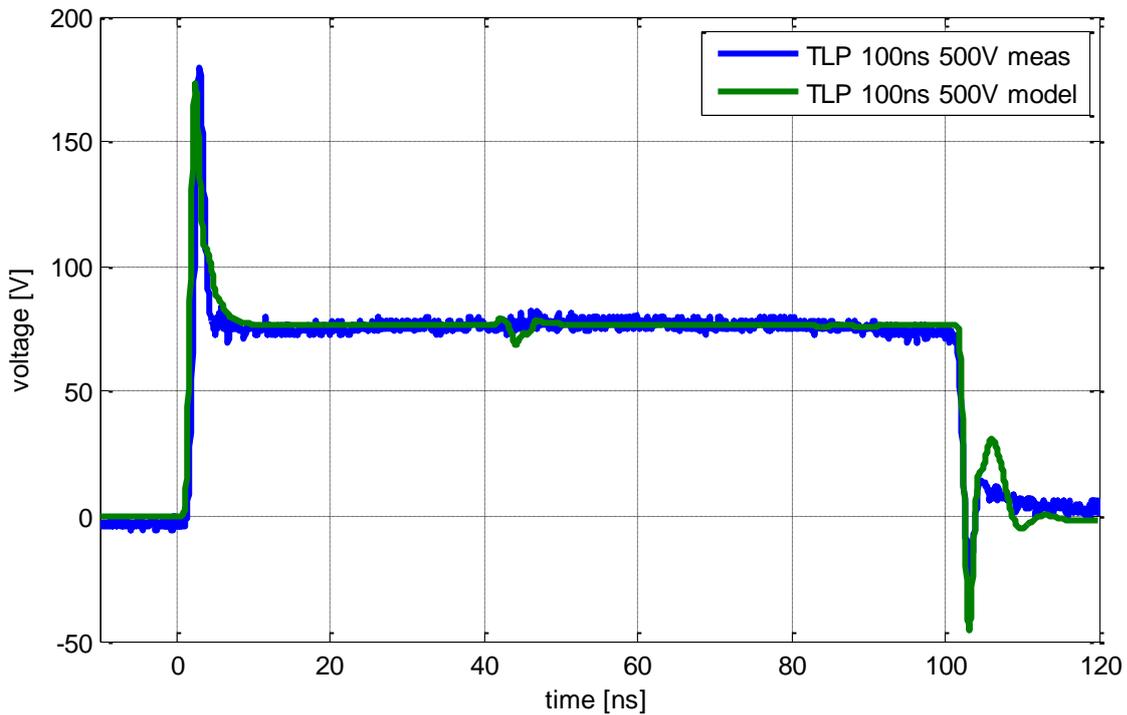


Figure 7.100: Comparison of measured and simulated critical voltage at TLE6251G Split pin

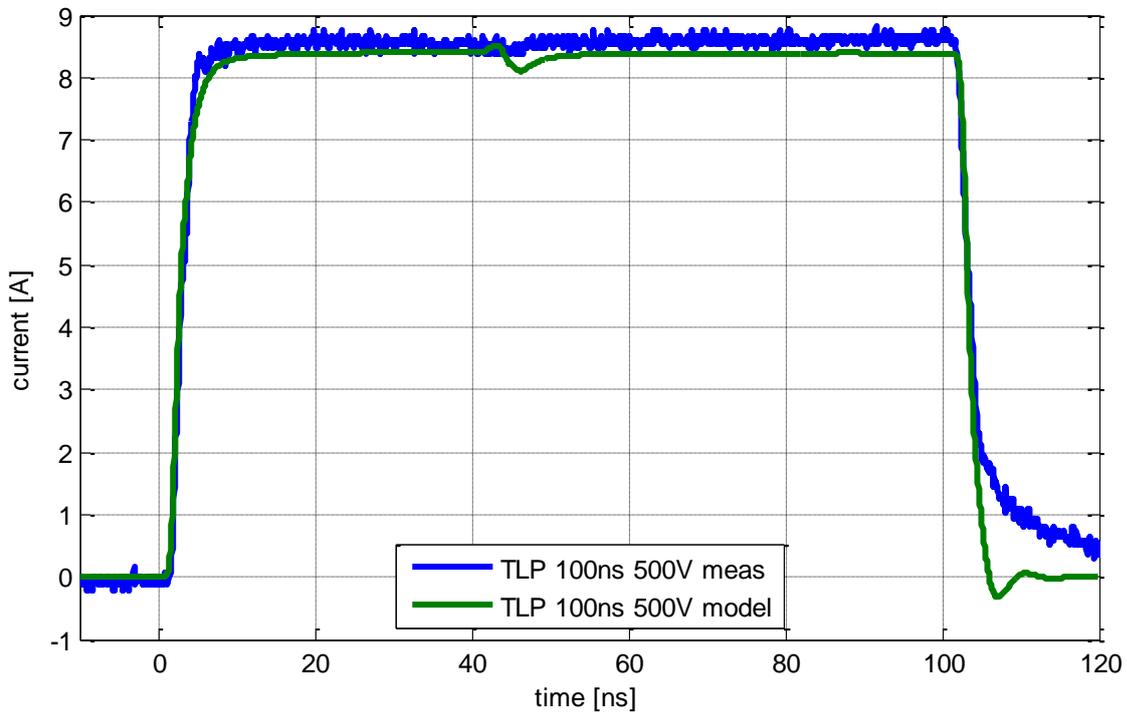


Figure 7.101: Comparison of measured and simulated critical current at TLE6251G Split pin

The simulated and measured discharge currents on demonstrator PCB at the connector pin are shown in Figure 7.102. The rise time and shape of the first peak of the curves are very similar. Permanent damage was measured for a 3.5 kV IEC generator discharge. The simulated energy in that case amounts only 34 μ J, which is

about twice as small as the critical energy for a 100 ns TLP discharge. The simulated model will withstand 5 kV IEC generator discharge. According to that result, an energy-based failure model is not suitable for Split pin. The maximum measured voltage on TLE6251G Split pin for a 25 ns TLP discharge was 436 V. The simulated voltage for a 3.5 kV IEC discharge was 518 V. Gateoxid-punch-through because of high voltage pulse can be the failure mechanism for TLE6251G Split pin.

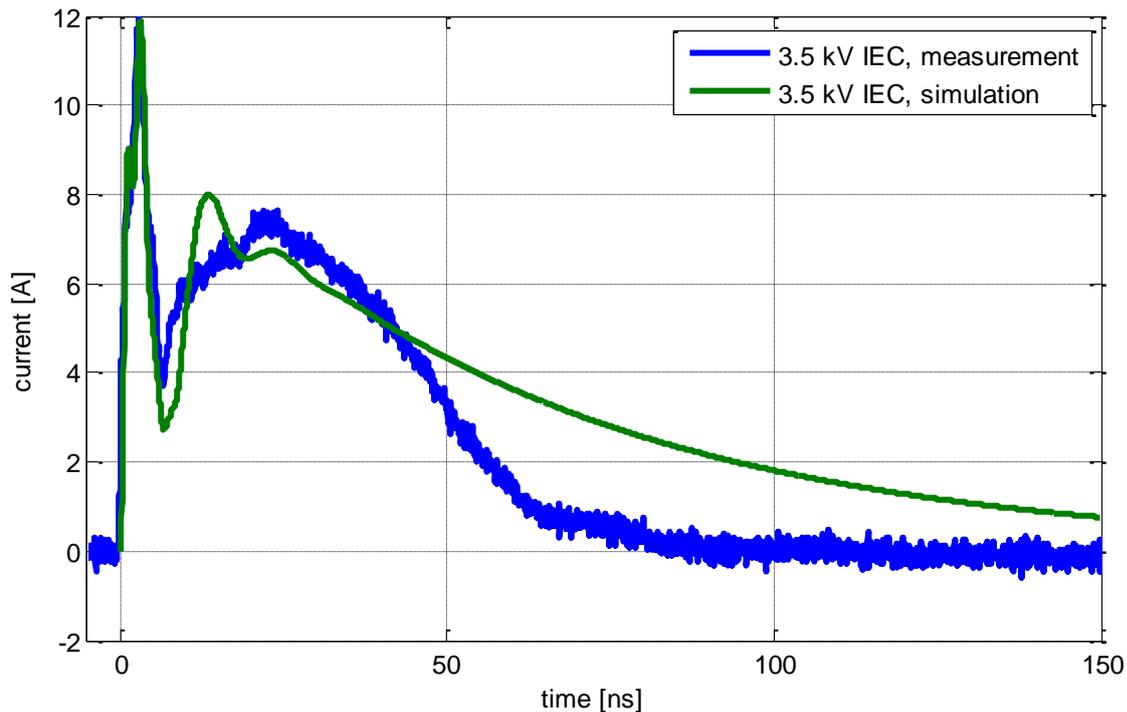


Figure 7.102: Simulated and measured current for TLE6251G Split pin at connector of demonstrator PCB

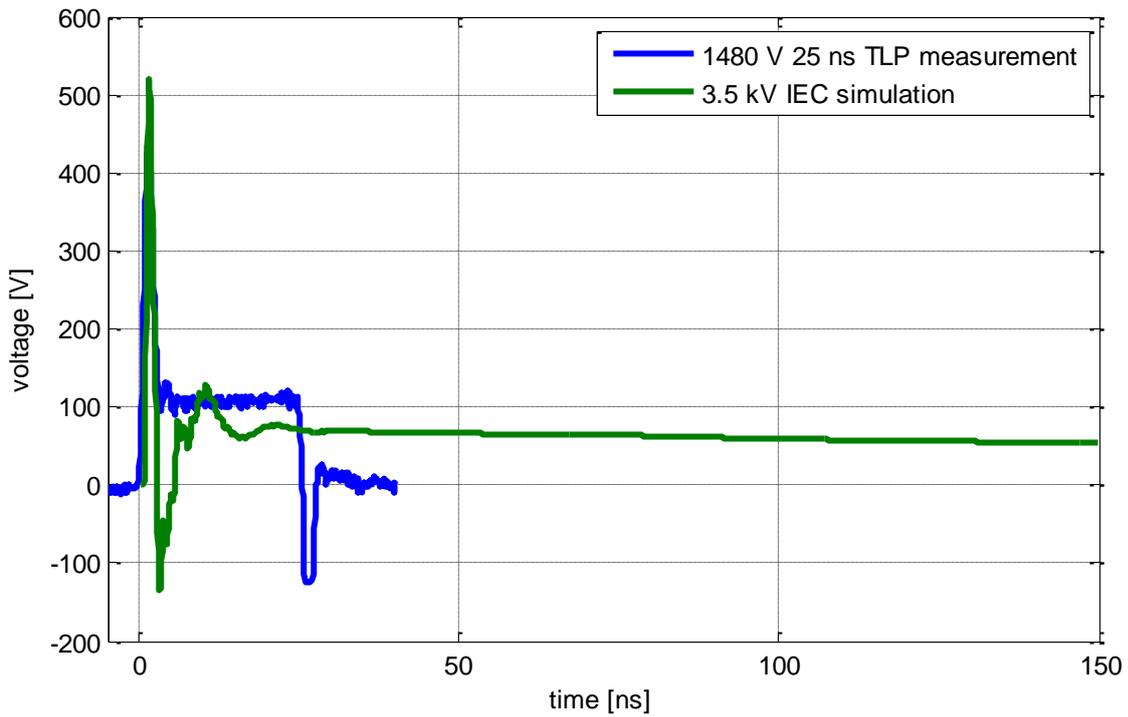


Figure 7.103: Maximum TLP voltage and IEC generator voltage at TLE6251G Split pin

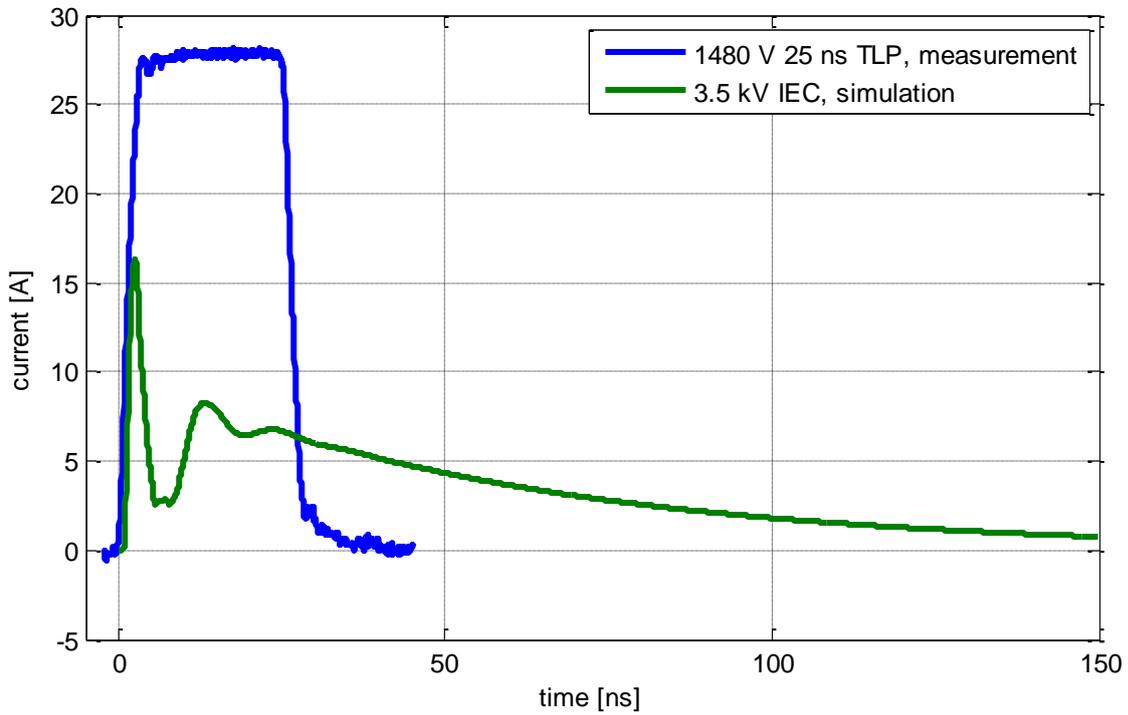


Figure 7.104: Maximum TLP current and IEC generator current at TLE6251G Split pin

ESD pulse	V _{ESD} [V]	V _{IC,max} [V]	I _{IC,max} [A]	E _{fail} [μJ]	Deviation [%]
IEC NoiseKen	3500	518	16.6	34	46
TLP 100 ns	500	179	8.6	65.79	0
TLP 25 ns*	1480*	436*	27.8*	75.06*	15*

Table 7.26: Comparison of IEC and TLP failure energies for TLE6251G Split pin (* = no failure could be detected)

7.6.6.3 Verification of LIN Transceiver Models

7.6.6.3.1 Verification of LIN Transceiver ATA6662C TxD Model

The measured and the modeled IV curves are compared in Figure 7.105. For the extension of the model's applicability the IV curve was extrapolated.

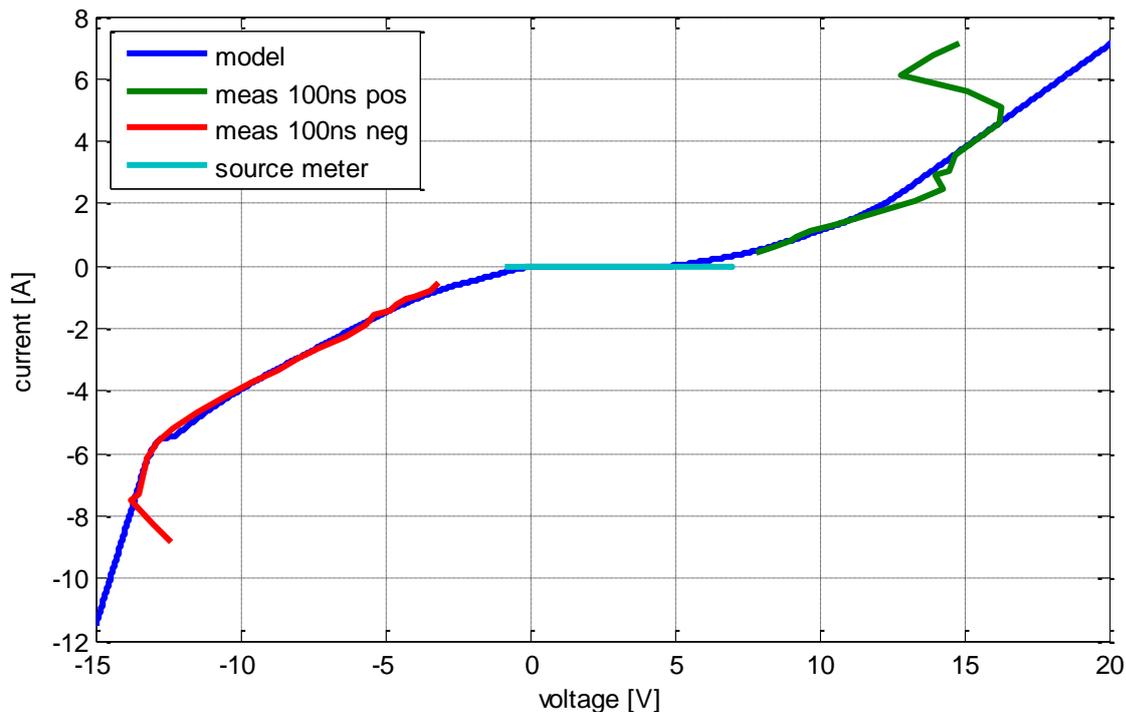


Figure 7.105: Comparison of measured and simulated IV curves of LIN TxD pin

The model is verified by a comparison of TLP measurement data and simulation of the TLP measurement setup including the IC model. Beside the TLP model described in section 7.3.4 a 10 nH inductor was added representing the inductance of the socket connected with the TLP testing board in the current return path of the IC.

The curves presented in Figure 7.106 and Figure 7.107 for 100 ns pulse width show a good matching. The voltage peak is simulated well. For a more accurate modeling of the setup additional parasitic elements should be considered.

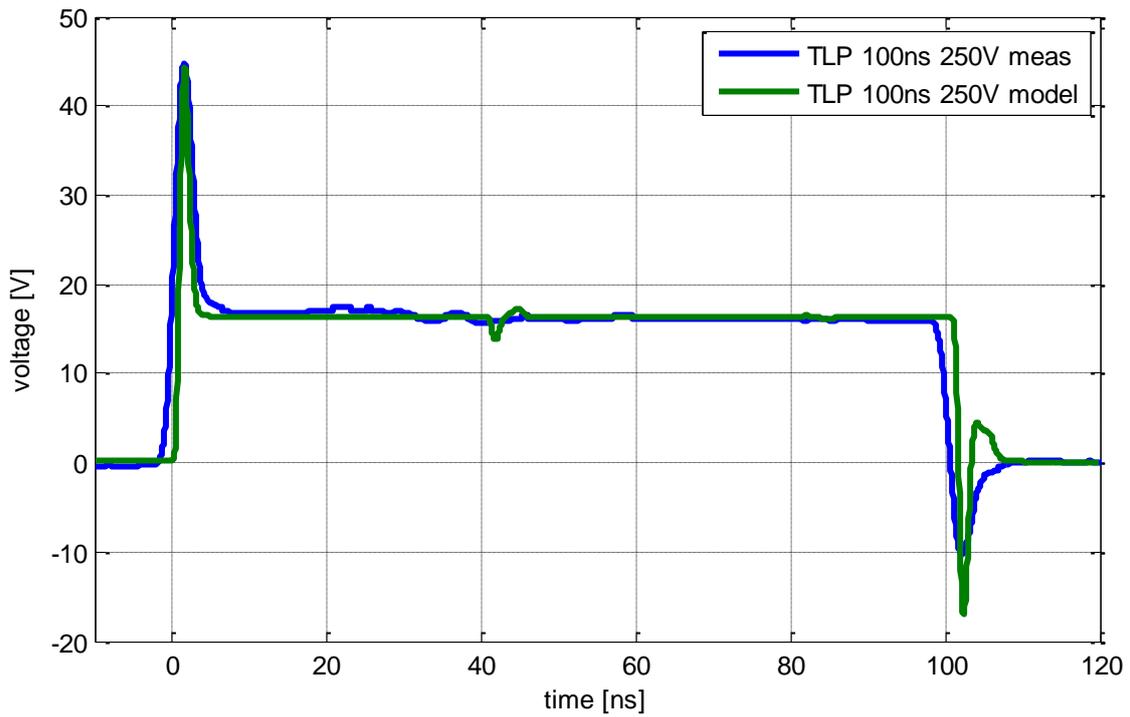


Figure 7.106: Comparison of measured and simulated critical voltage at ATA6662C TxD pin

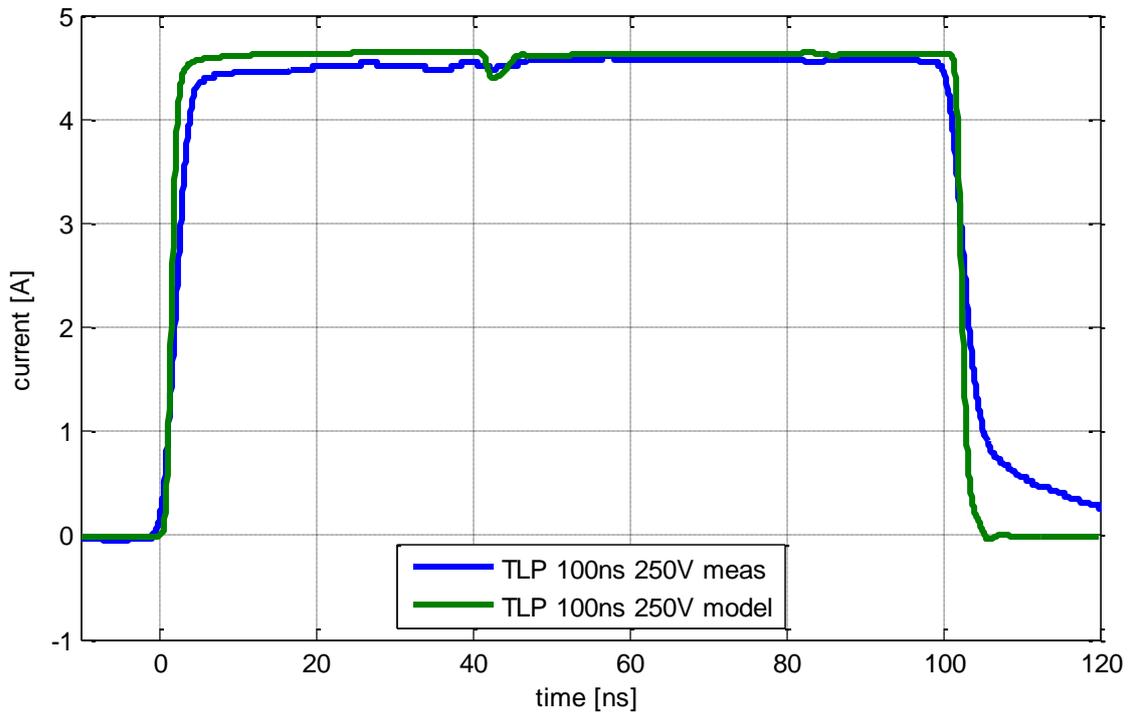


Figure 7.107: Comparison of measured and simulated critical current at ATA6662C TxD pin

The simulated and measured discharge currents at the connector pin are shown in Figure 7.108. Permanent damage was detected for a 3 kV IEC generator discharge. The rise time and shape of the first peak of the curves are very similar.

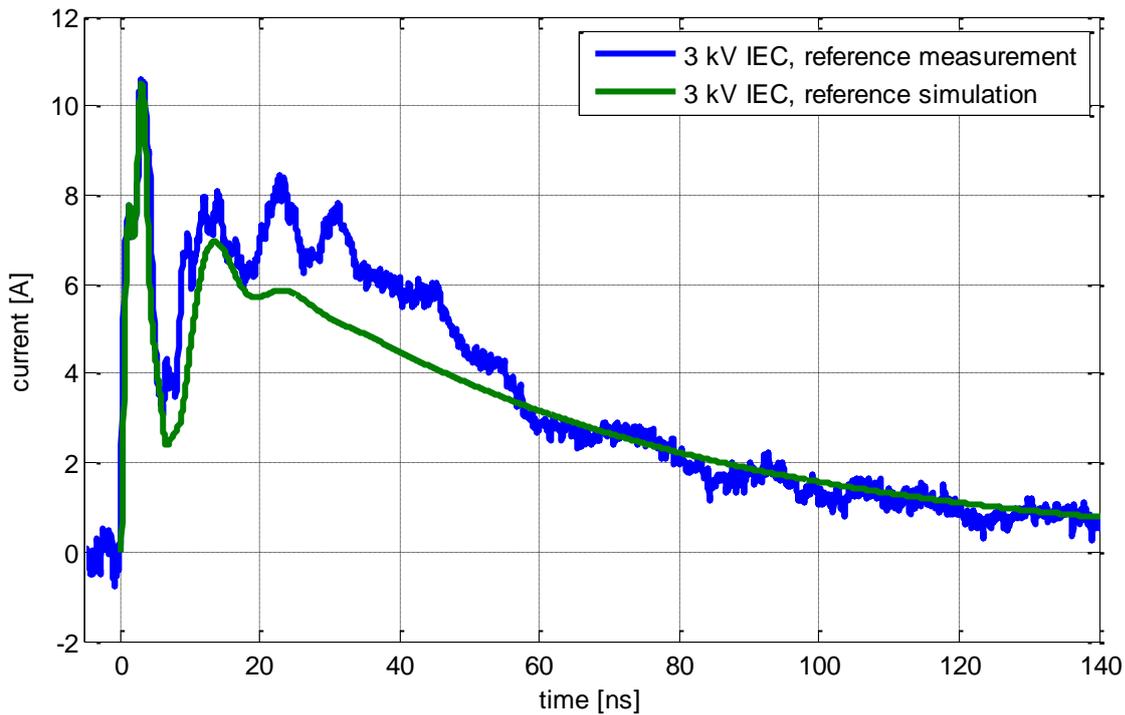


Figure 7.108: Simulated and measured current for LIN TxD pin at connector of demonstrator PCB

In Figure 7.109 and Figure 7.110 the maximum current and voltage amplitudes are compared for TLP and IEC ESD discharges at the detected failure levels. Because measurement of voltage and current at the IC pin on system level with IEC ESD generator is difficult without affecting the test result, the waveforms at the IC pin were simulated and compared to measured results taken with the TLP setup. Maximum TLP amplitudes which cause IC failure are obtained with 25 ns pulse width. In case of the LIN TxD pin the charging voltage was 525 V. The peak voltage of over 50 V was measured compared to 30 V simulated for the IEC generator. This proves that IC failure with IEC ESD discharges is not an overvoltage effect here. The current peak amplitude for 25 ns pulse width is 10 A and about 14 A for the simulated IEC discharge.

The IC models were implemented based on TLP data with 100 ns pulse width. The calculated failure energies of TLP and system level IEC discharges are compared in Table 7.27. Deviation of about 7 % between the energies is obtained. It is assumed that the IC failure can be referred to the same energy-based mechanism for TLP and IEC discharges.

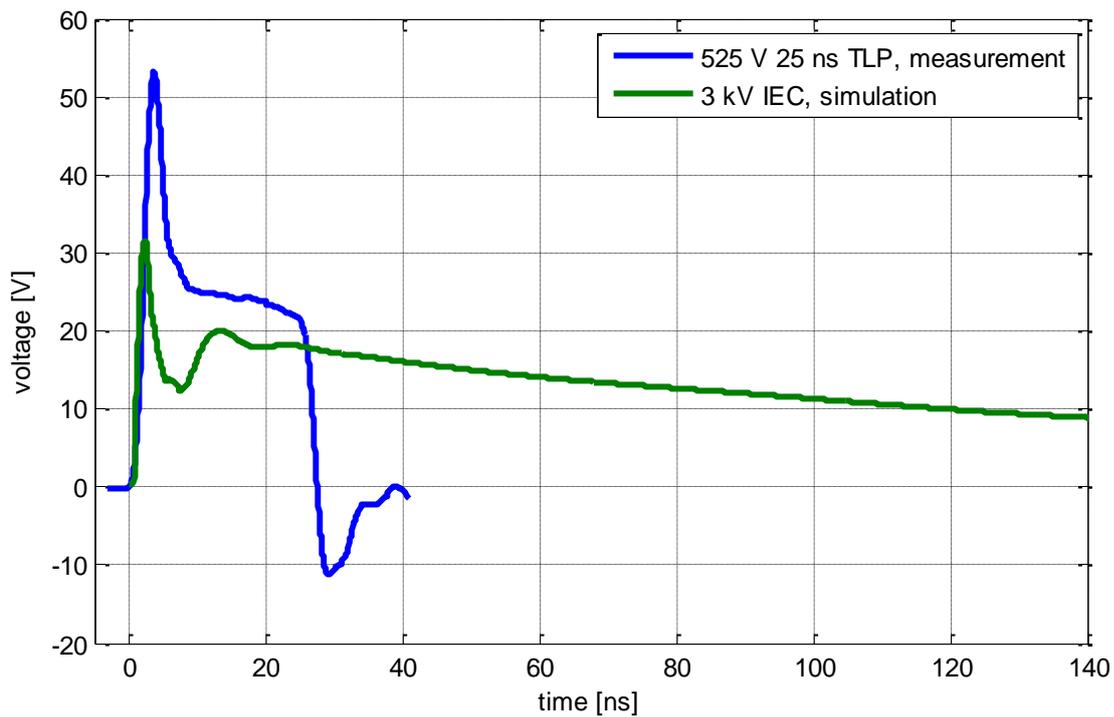


Figure 7.109: Maximum TLP voltage and IEC generator voltage at LIN TxD pin

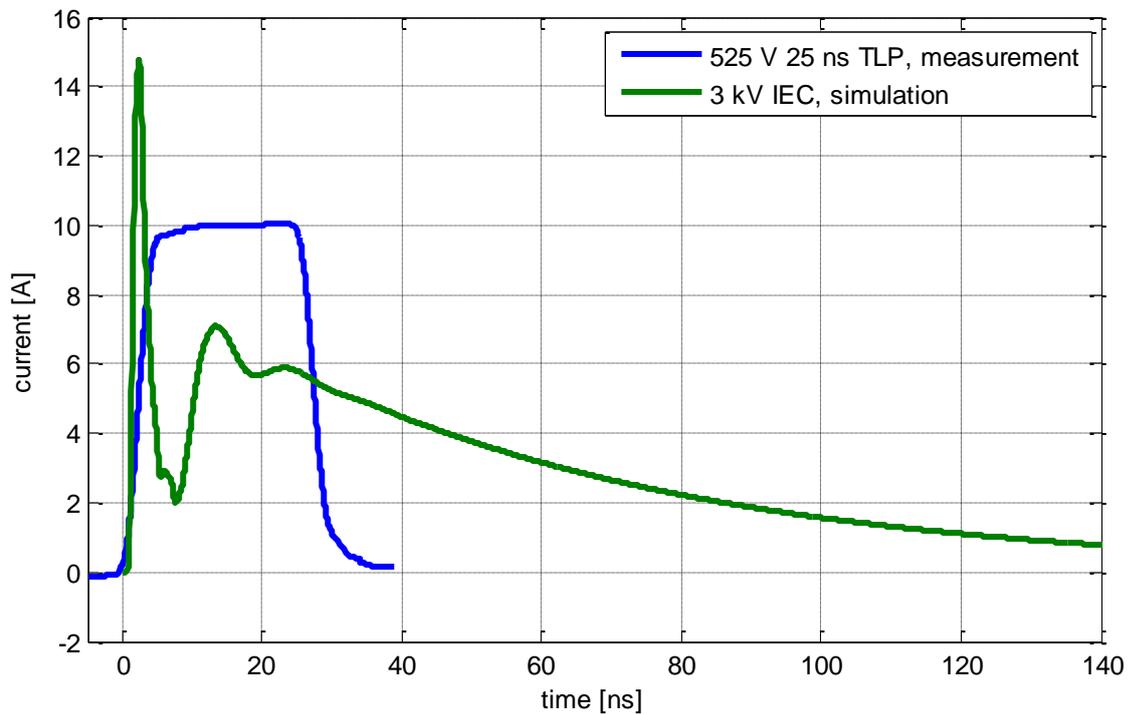


Figure 7.110: Maximum TLP current and IEC generator current at LIN TxD pin

ESD pulse	V _{ESD} [V]	V _{IC,max} [V]	I _{IC,max} [A]	E _{fail} [μJ]	Deviation [%]
IEC NoiseKen	3000	31.61	14.74	6.92	7
TLP 100 ns	250	44.8	4.6	7.4	0

Table 7.27: Comparison of IEC and TLP failure energies for ATA662C TxD pin

7.6.6.3.2 Verification of LIN Transceiver ATA6662C BUS Model

In Figure 7.111 the modeled IV curve is compared to the measured 100 ns TLP characteristics. A good matching is obtained for positive and negative charging voltages. Breakdown voltage for the model is chosen in respect to the source meter measurement.

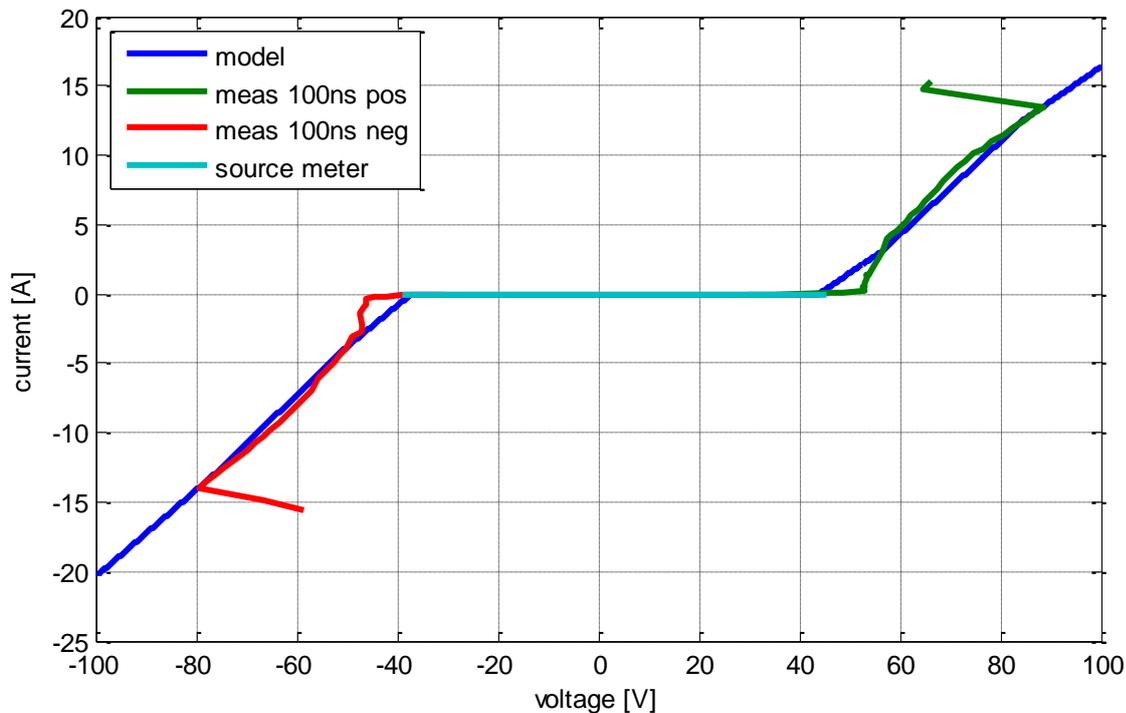


Figure 7.111: Comparison of measured and implemented IV-curves of ATA6662C BUS pin

The model is verified by a comparison of TLP measurement data and simulation of the TLP measurement setup including the IC model. Beside the TLP model described in section 7.3.4 a 10 nH inductor was added representing the inductance of the socket mounted on the TLP testing board in the current return path of the IC.

The voltage curves presented in Figure 7.112 for 100 ns are not overlaying. The model does not reflect the rise of the voltage with progress of the TLP pulse. Only the mean value is used in the IV curve. The simulated initial peak is about 30 V higher.

The current curves show a small deviation, this remains constant over the entire pulse length (see Figure 7.113).

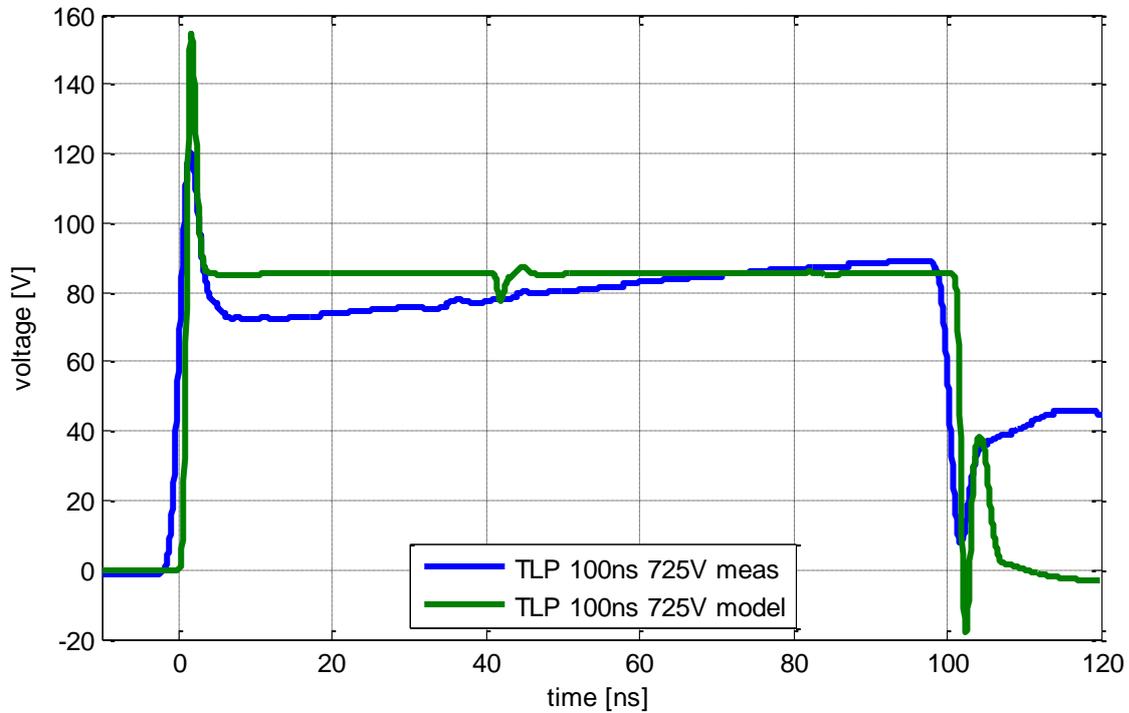


Figure 7.112: Comparison of measured and simulated critical voltage at ATA6662C BUS pin

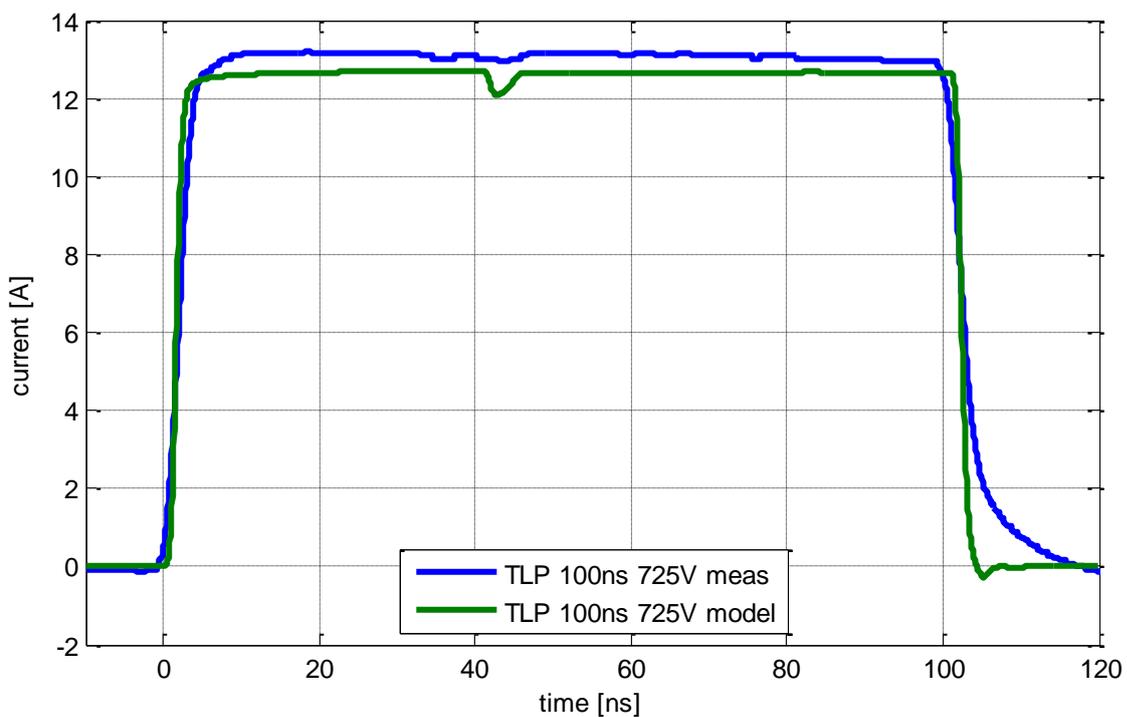


Figure 7.113: Comparison of measured and simulated critical current at ATA6662C BUS pin

The simulated and measured discharge currents at the demonstrator's connector pin are shown in Figure 7.114. Permanent damage was detected for an 8.5 kV IEC generator discharge in simulation and in measurement. Because measurement of voltage at the IC pin on system level with IEC ESD generator will affect the test results, the energy cannot be calculated. However, the simulated critical voltage for the BUS pin is 8.5 kV and the corresponding energy is 107 μJ .

The rise time and shape of the first peak of the curves are very similar. The measured curve is overlaid by an oscillation. To get a better match parasitic elements should be modeled.

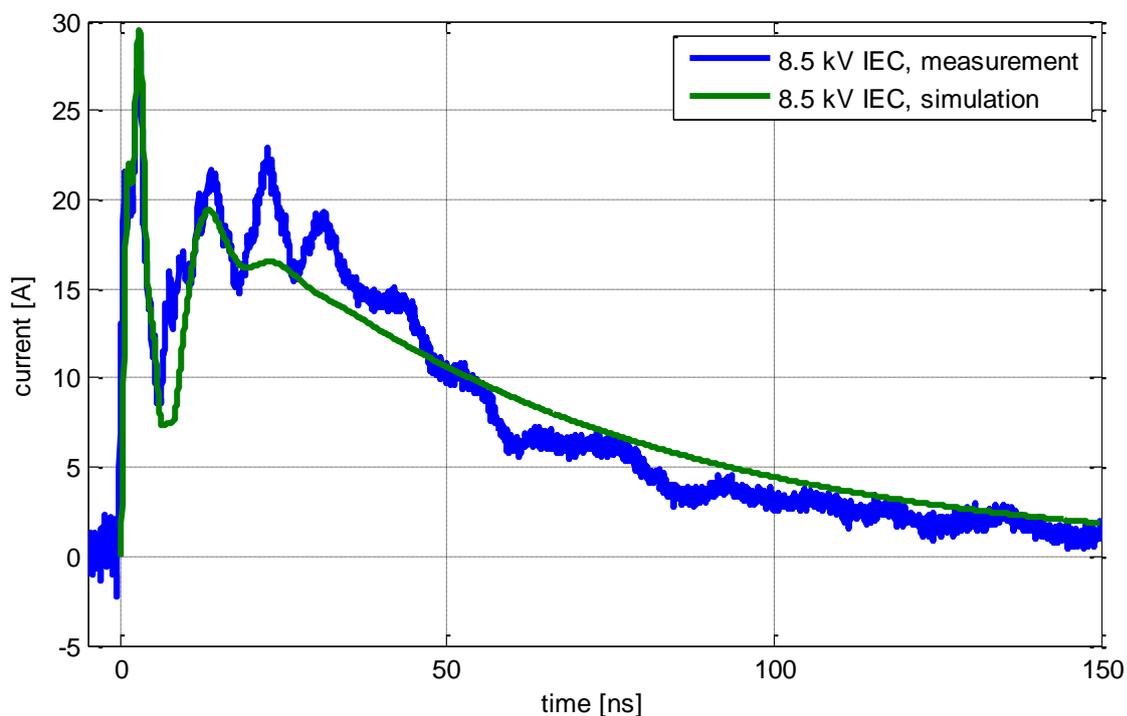


Figure 7.114: Simulated and measured current for ATA6662C BUS pin at connector of demonstrator PCB. $L_{\text{socket}}=10\text{nH}$

In Figure 7.109 and Figure 7.110 the maximum current and voltage amplitudes are compared for TLP and IEC ESD discharges at the detected failure levels. The waveforms at the IC pin were simulated and compared to measured results taken with the TLP setup. Maximum TLP amplitudes are obtained with 25 ns pulse width and 1480 V charge voltage. IC damage could not be detected. The peak voltage of about 140 V was measured compared to 200 V simulated for the IEC generator. This proves that IC failure with IEC ESD discharges is not an overvoltage effect here. The current peak amplitude for 25 ns pulse width is 28 A and about 41 A for the simulated IEC discharge.

The IC models were implemented based on TLP data with 100 ns pulse width. The calculated failure energies of TLP and system level IEC discharges are compared in Table 7.27. Deviation of about 12 % between the energies is obtained.

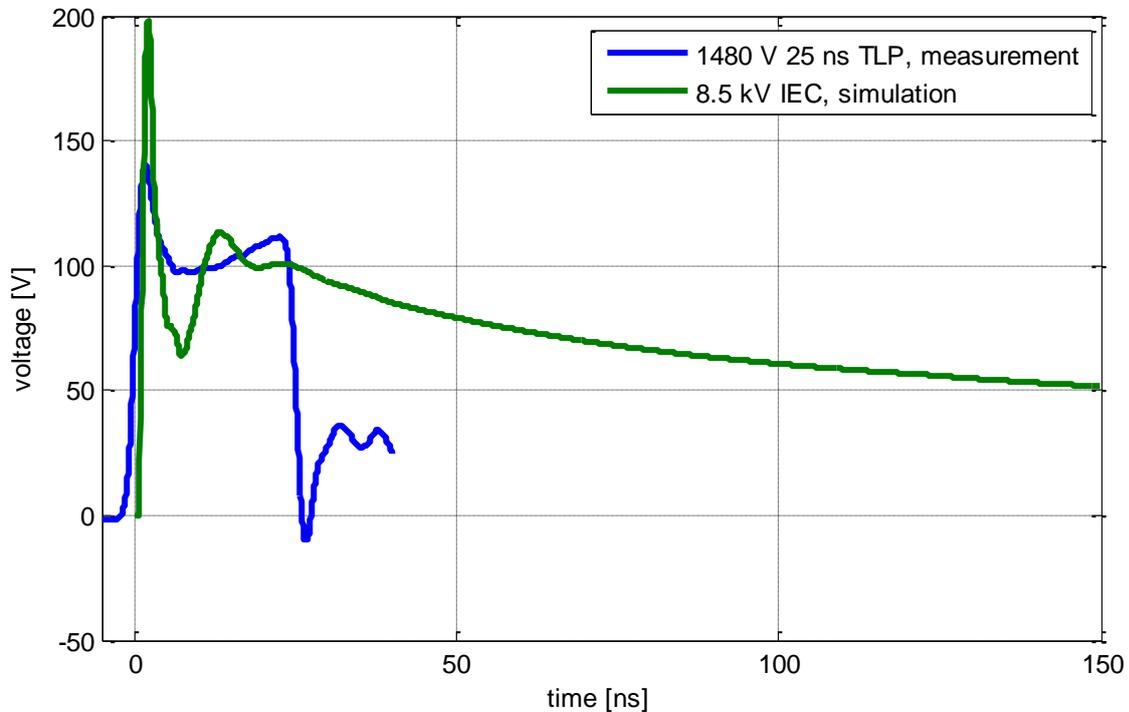


Figure 7.115: Maximum TLP voltage and IEC generator voltage at ATA6662C BUS pin

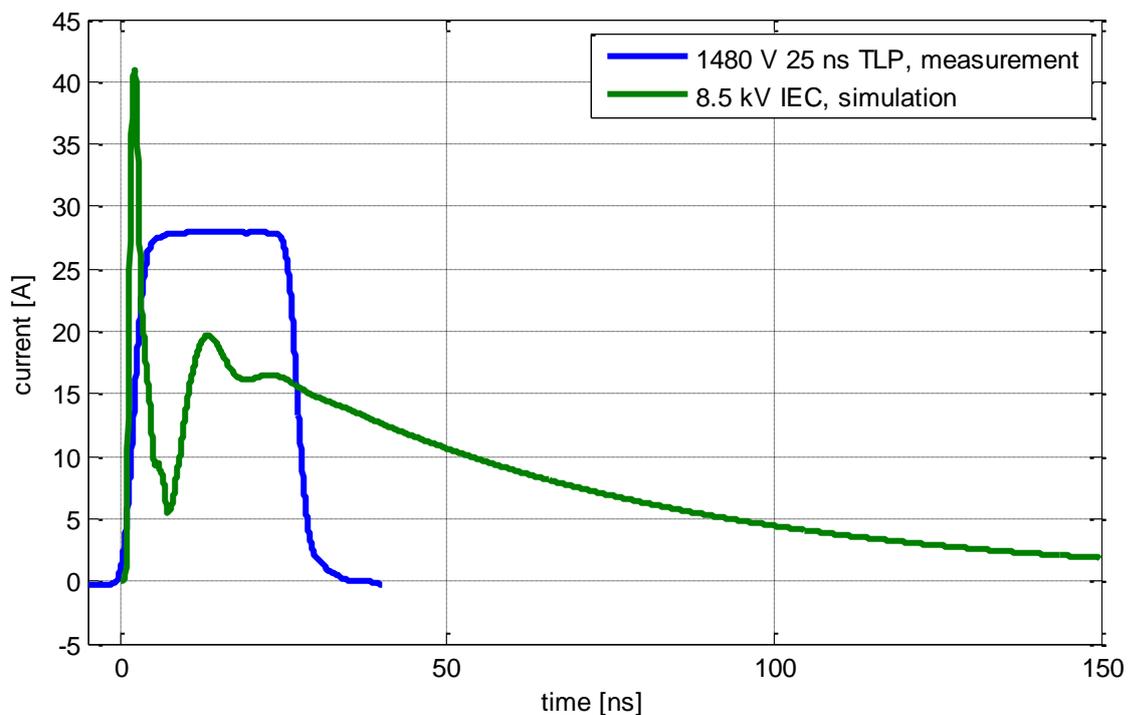


Figure 7.116: Maximum TLP current and IEC generator current at ATA6662C BUS pin

ESD pulse	V _{ESD} [V]	V _{IC,max} [V]	I _{IC,max} [A]	E _{fail} [μJ]	Deviation [%]
IEC NoiseKen	8.5	198	41	107	10
TLP 100 ns	120	13	112.71	120	0

Table 7.28: Comparison of IEC and TLP failure energies for ATA6662C BUS pin

7.6.6.4 Verification of μC Models

7.6.6.4.1 Verification of μC XC864 DATA Model

In Figure 7.117 the simulated and measured IV characteristics are compared for 100 ns pulse width.

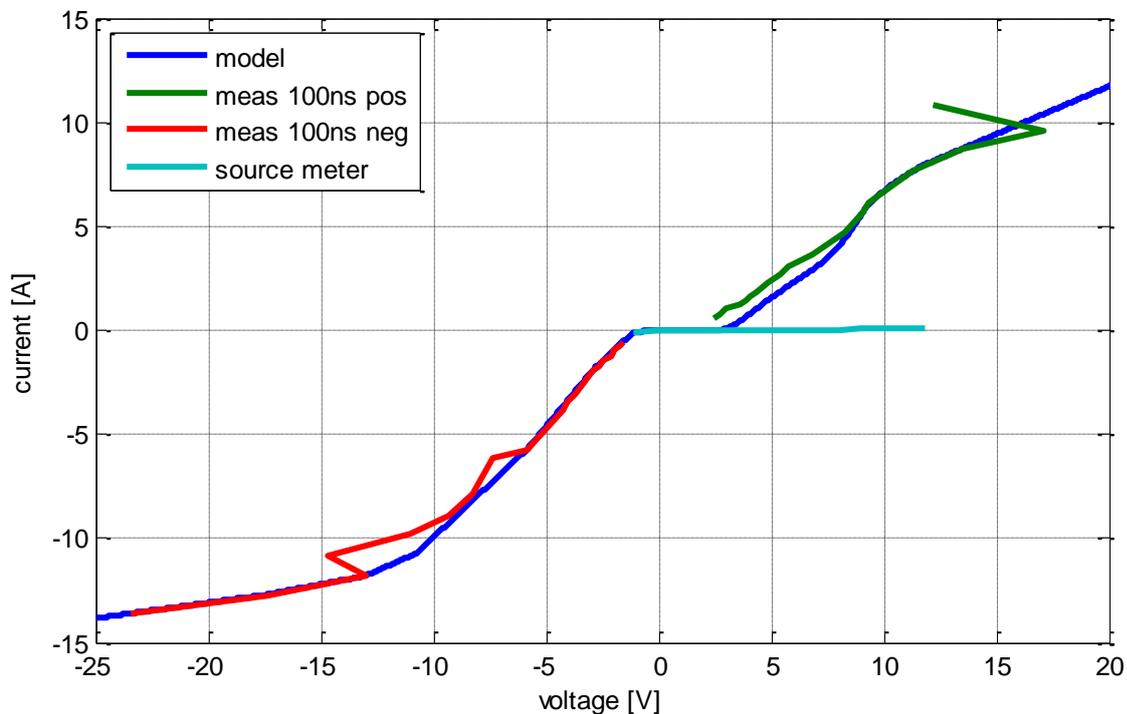


Figure 7.117: Comparison of measured and implemented IV-curves of μC DATA pin

A good matching was obtained comparing simulation and measurement data in Figure 7.118 and Figure 7.119. L_{socket} was set to 18 nH.

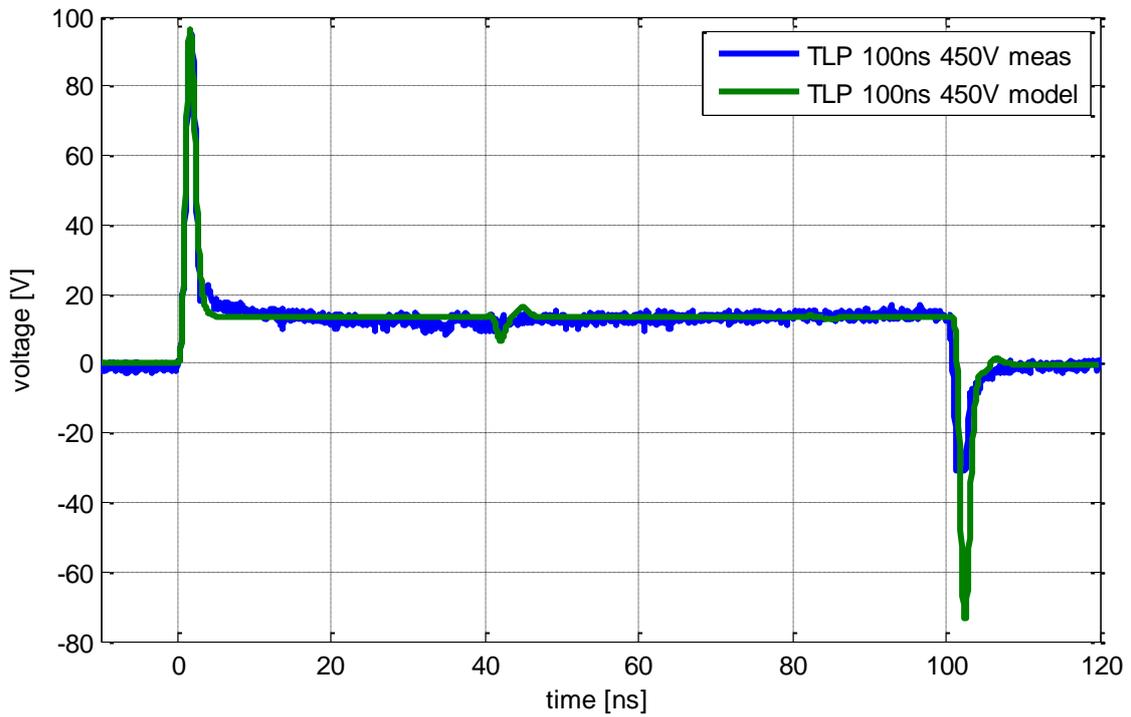


Figure 7.118: Comparison of measured and simulated critical voltage at XC864 DATA pin

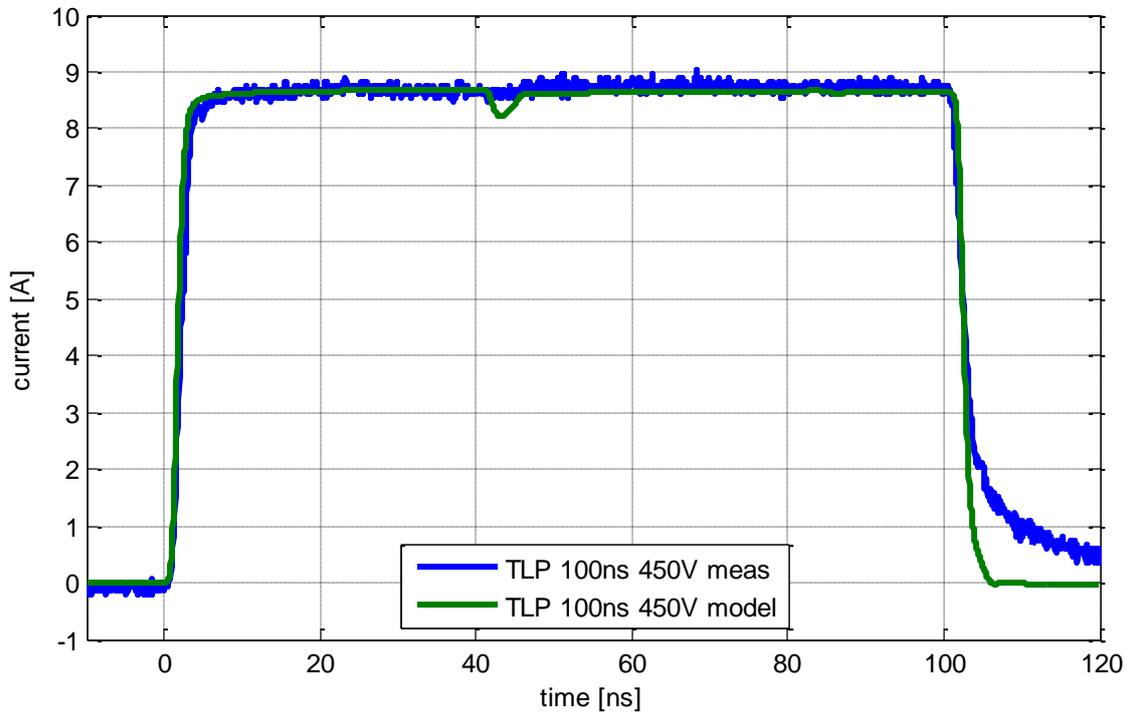


Figure 7.119: Comparison of measured and simulated critical current at XC864 DATA pin

Measured and simulated waveforms of the discharge current at the connector pin are very similar. In Figure 7.120 the curves for 5,5 kV charging voltage are presented.

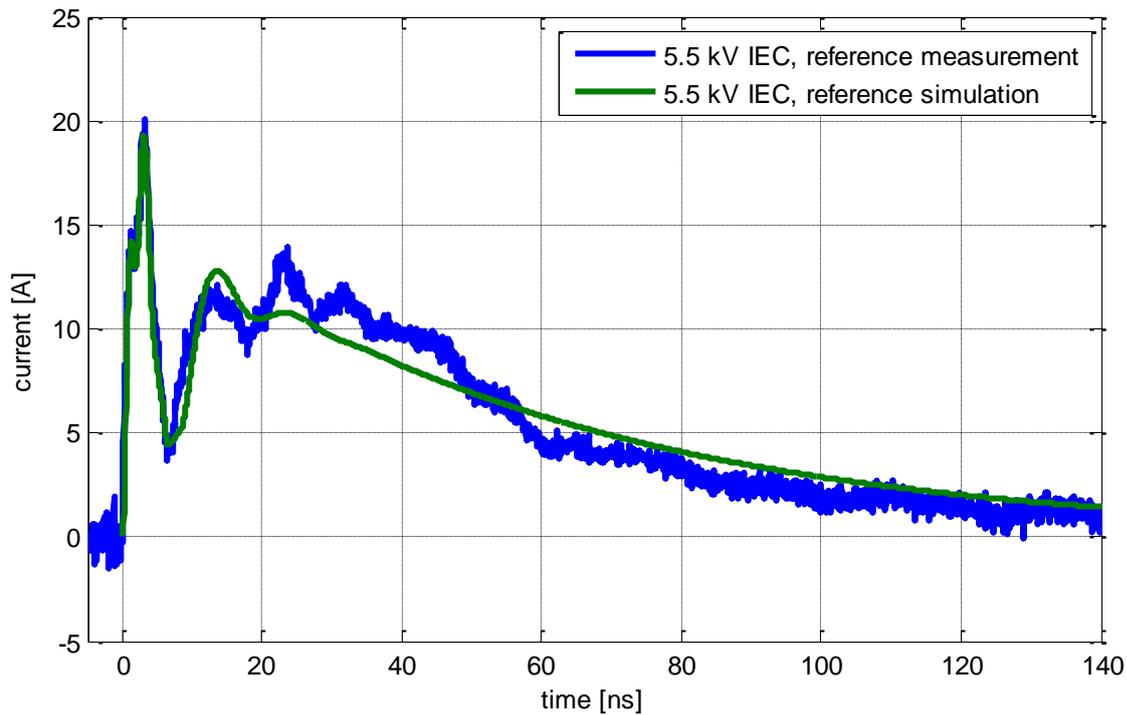


Figure 7.120: Simulated and measured current for μC DATA pin at connector of demonstrator PCB

In Figure 7.121 the voltage amplitude measured with the TLP setup increases by factor 3 compared to the IEC amplitude. Maximum TLP charging voltage before destruction was 850 V and pulse width was set to 25 ns. In Table 7.29 the parameters are compared for the 100 ns TLP measured dataset and the simulated data for the IEC discharge. The deviation between failure energies obtained with both setups is about 9 %. The failure mechanism is also here assumed to be energy-based.

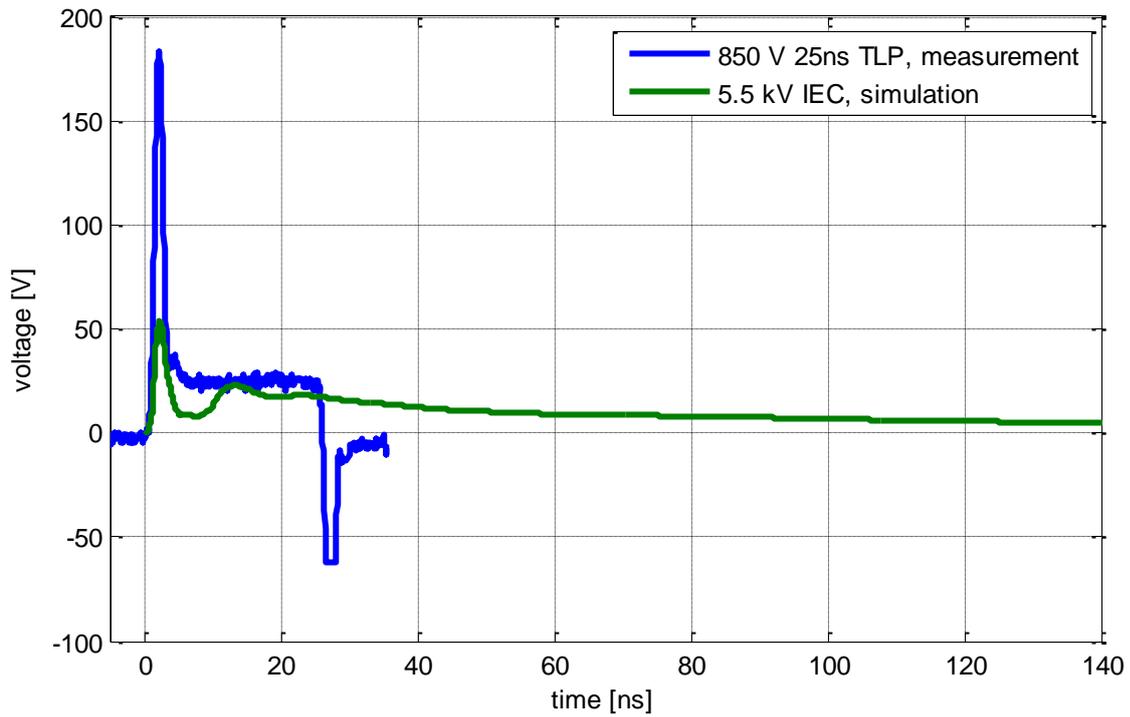


Figure 7.121: Maximum TLP voltage and IEC generator voltage at μC DATA pin

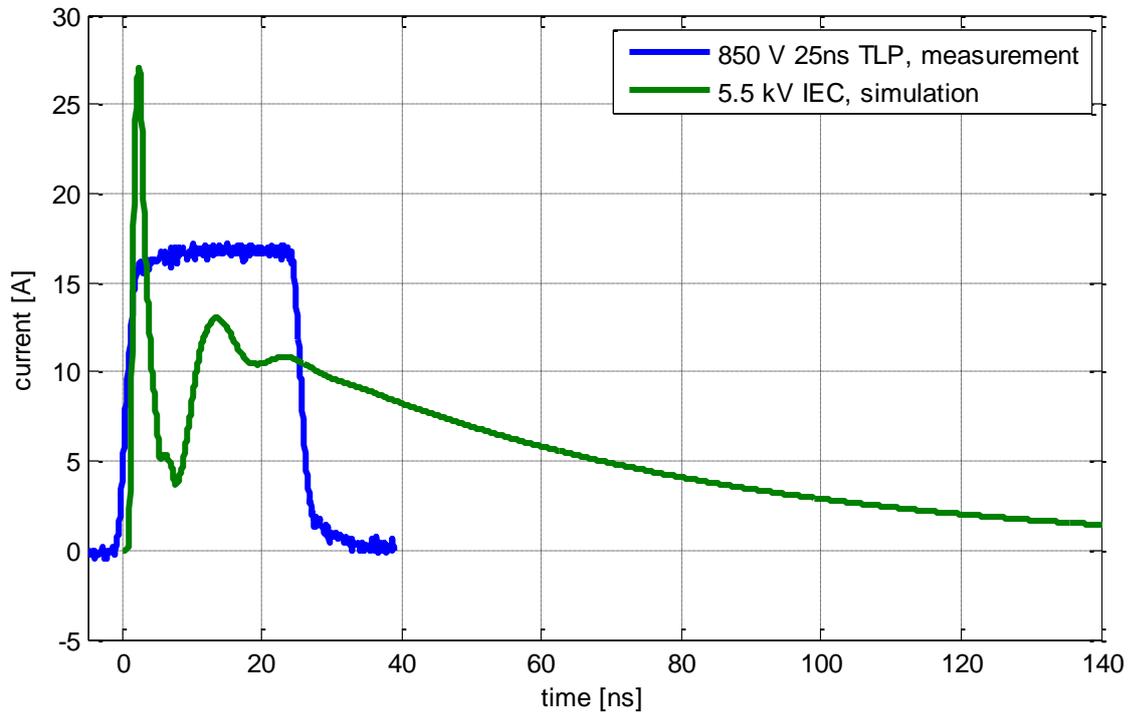


Figure 7.122: Maximum TLP current and IEC generator current at μC DATA pin

ESD pulse	V_{ESD} [V]	$V_{IC,max}$ [V]	$I_{IC,max}$ [A]	E_{fail} [μ J]	Deviation [%]
IEC NoiseKen	5500	53.42	27.07	11.30	8
TLP 100 ns	450	95.4	9.0	12.3	0

Table 7.29: Comparison of IEC and TLP failure energies for XC864 DATA pin

7.6.6.4.2 Verification of μ C XC864 VAREF Model

In Figure 7.123 the simulated and measured IV characteristics are compared for 100 ns pulse width. Snap back of the IC is not modeled.

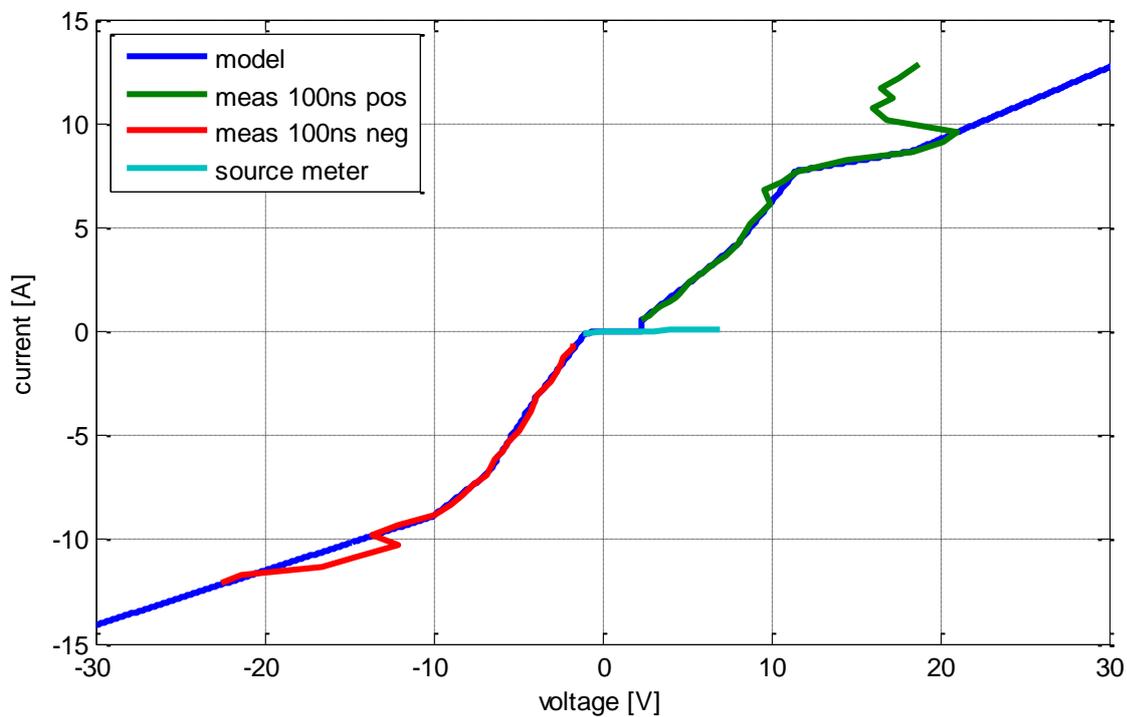


Figure 7.123: Comparison of measured and implemented IV-curves of XC864 VAREF pin

Comparing simulation and measurement data for a TLP discharge in Figure 7.124 and Figure 7.125 a good matching could be observed. Socket inductivity of 18 nH is used.

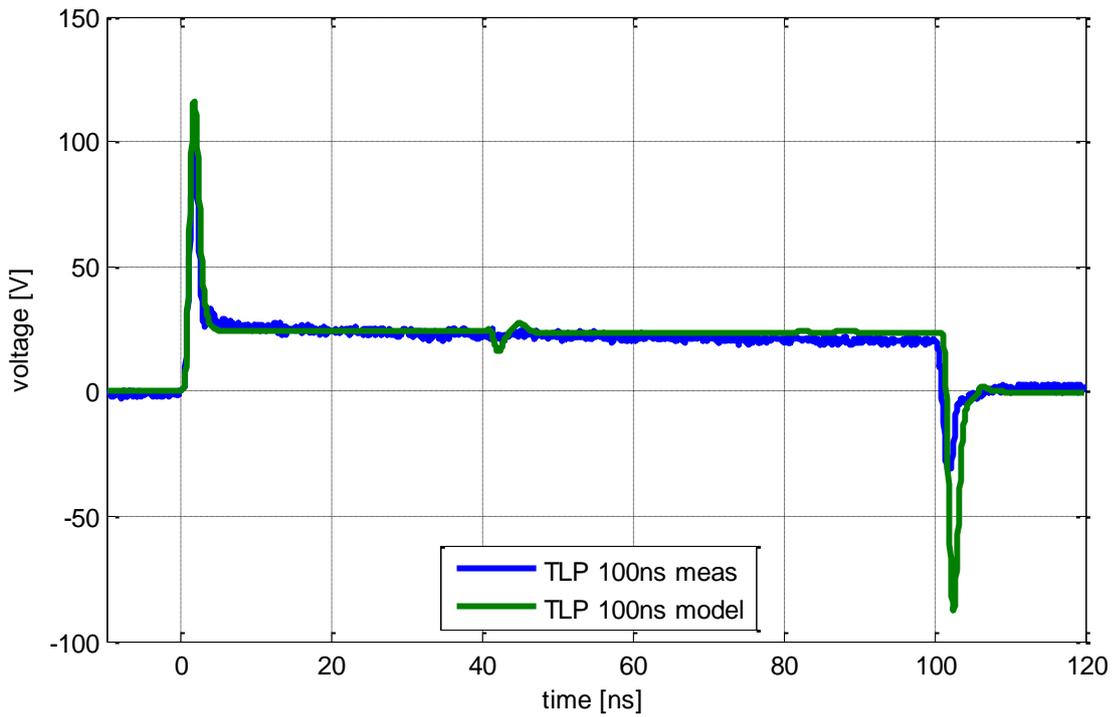


Figure 7.124: Comparison of measured and simulated critical voltage at XC864 VAREF pin

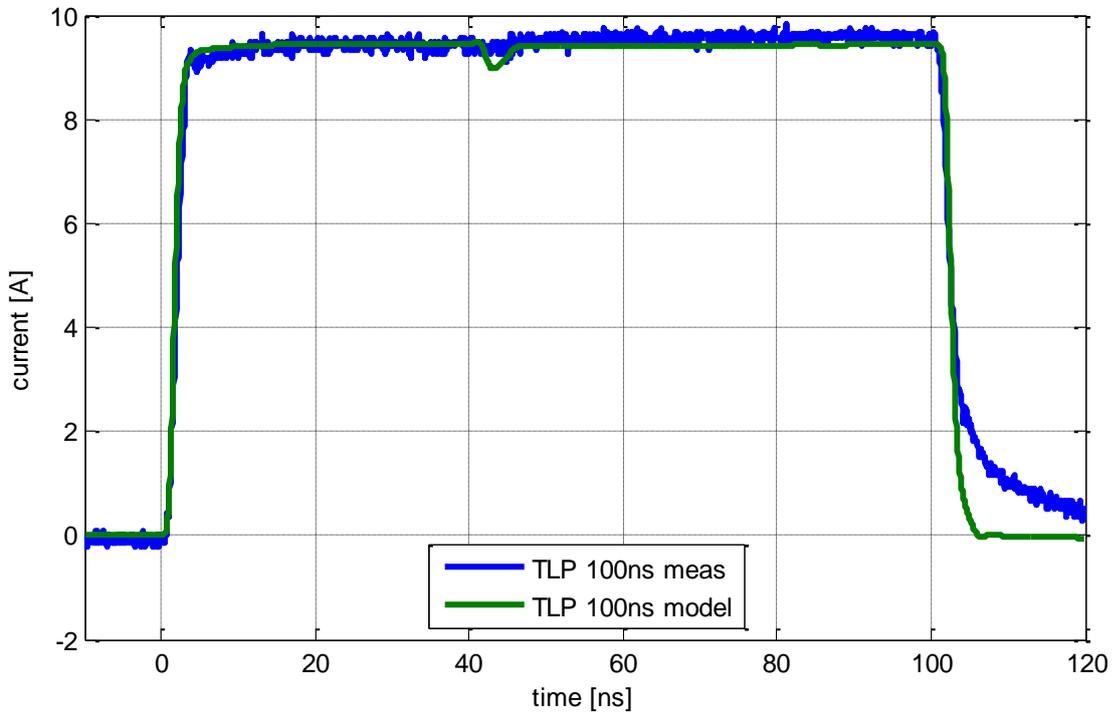


Figure 7.125: Comparison of measured and simulated critical current at XC864 VAREF pin

System level measured and simulated waveforms of the discharge current at the connector pin are very similar. Figure 7.126 shows the curves for a critical 6 kV IEC

discharge on the demonstrator board. A good match of the first peak may be observed.

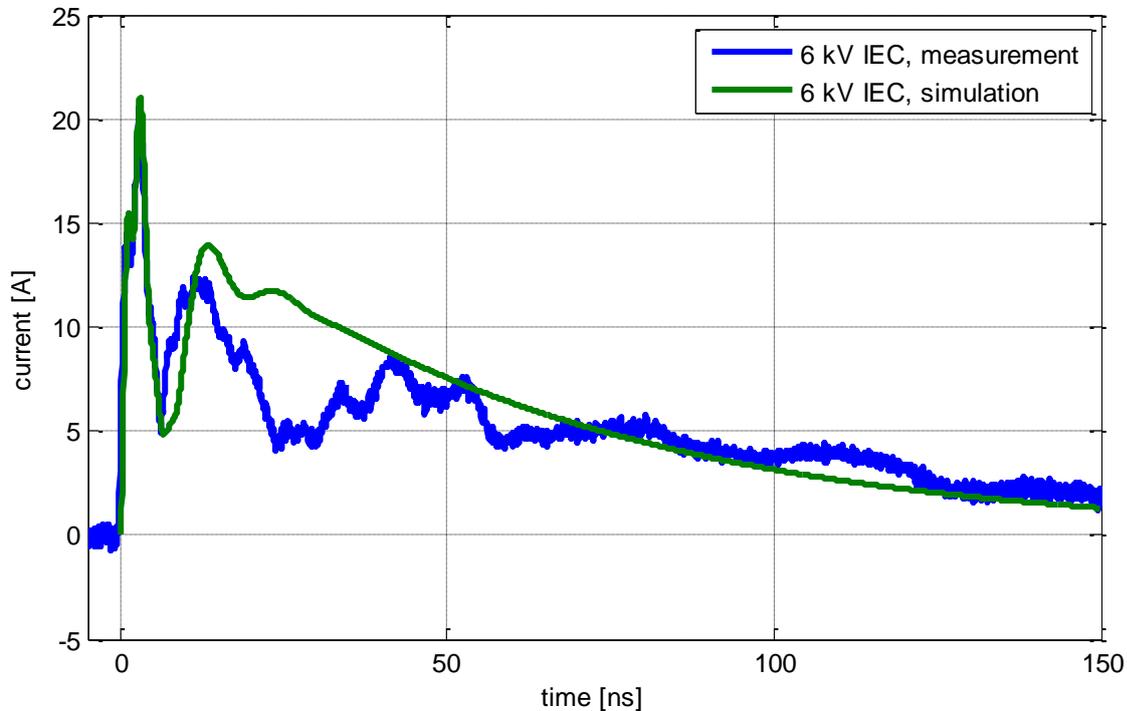


Figure 7.126: Simulated and measured current for XC864 VAREF pin at connector of demonstrator PCB

Figure 7.127 and Figure 7.128 compare critical amplitudes measured and simulated on the IC pin for different ESD stresses. It can be seen that the maximal voltage for a 25 ns TLP pulse is more than twice higher compared to IEC ESD generator. This proves that IC failure with IEC ESD discharges is not an overvoltage effect here. The current peak amplitude for 25 ns pulse width is 14.8 A and about 30 A for the simulated IEC discharge.

The VAREF pin model is implemented based on TLP data with 100 ns pulse width. The calculated failure energies of TLP and system level IEC discharges are compared in Table 7.30. Deviation of about 15 % between the energies is obtained. It is assumed that the IC failure can be referred to the same energy-based mechanism for TLP and IEC discharges.

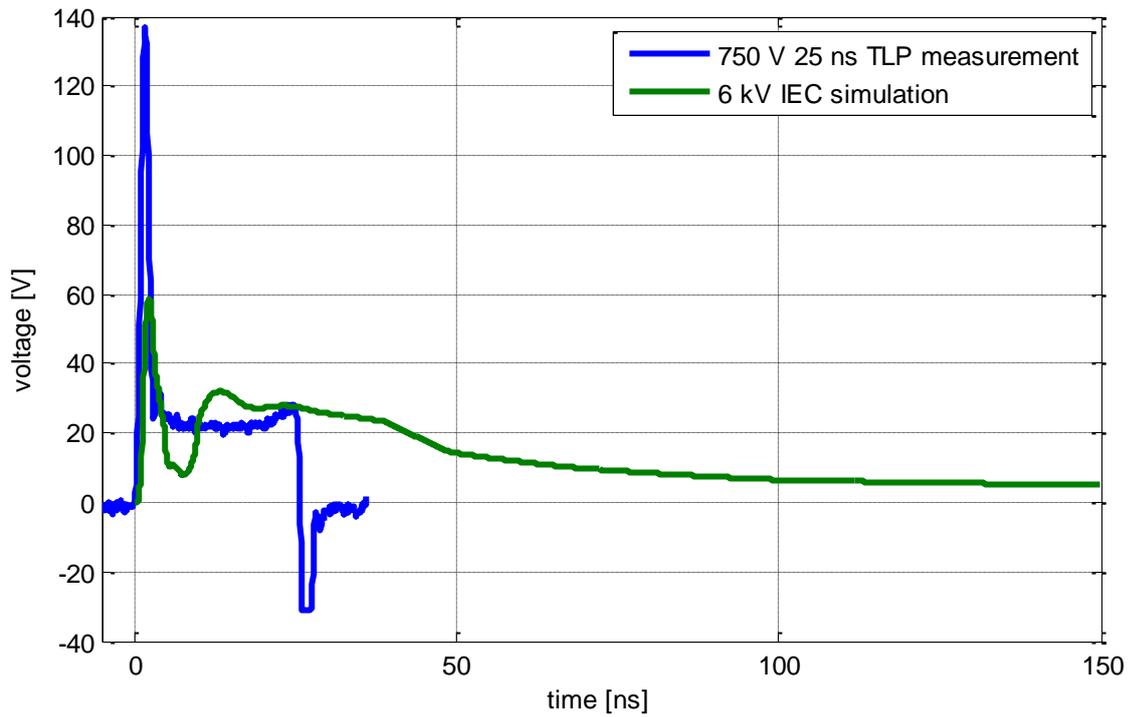


Figure 7.127: Maximum TLP voltage and IEC generator voltage at XC864 VAREF pin

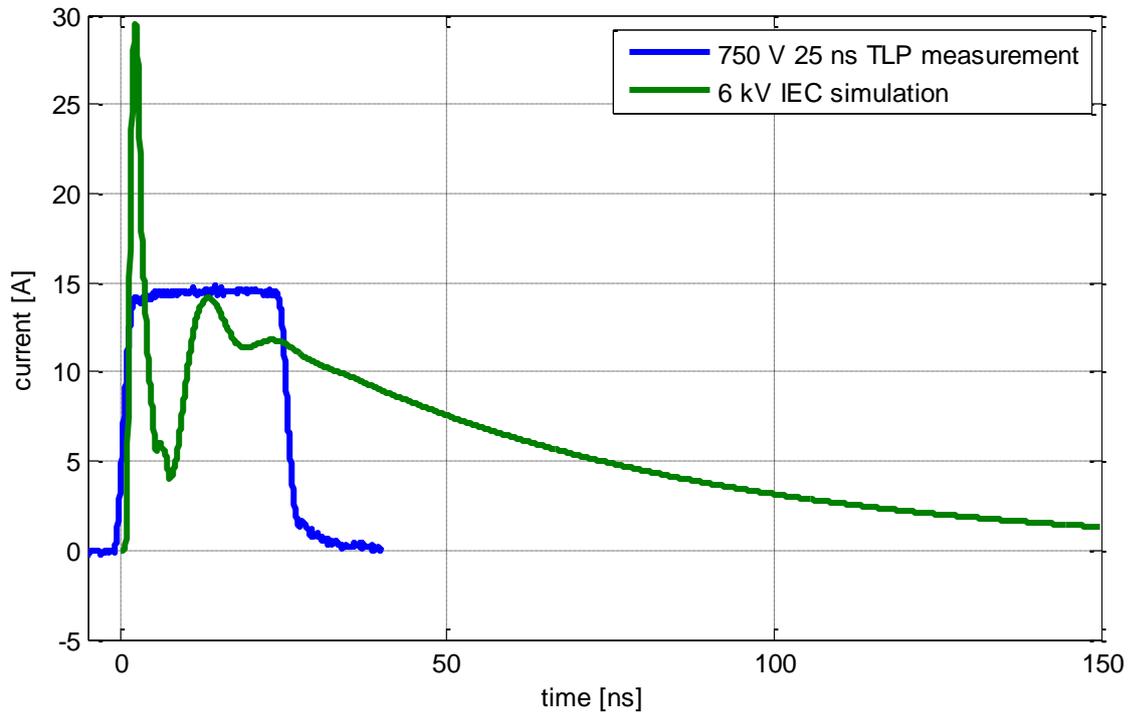


Figure 7.128: Maximum TLP current and IEC generator current at XC864 VAREF pin

ESD pulse	V _{ESD} [V]	V _{IC,max} [V]	I _{IC,max} [A]	E _{fail} [μJ]	Deviation [%]
IEC NoiseKen	6	59	30	17	15
TLP 100 ns	500	95	9.8	20.16	0
TLP 25 ns	750	136	14.8	7.90	60

Table 7.30: Comparison of IEC and TLP failure energies for XC864 VAREF pin

7.6.6.5 Diodes

7.6.6.5.1 Diode BAW156

The modeled IV curve is composed of 100 ns TLP data and source meter data. A good matching of the curves can be observed in Figure 7.129.

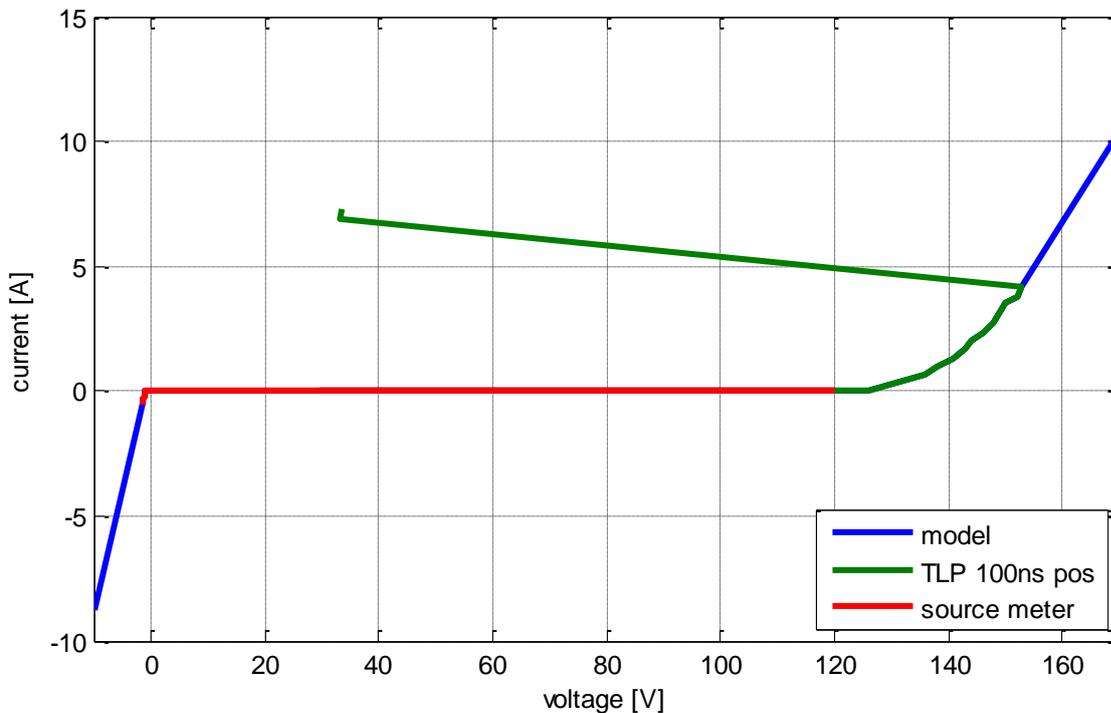


Figure 7.129: Comparison of measured and implemented IV-curve at BAW156 diode

Voltage measurement using the trailer ECU PCB is not possible due to additional parallel elements and oscilloscope ground connection. For a qualitative statement about potential threat of the ECU current waveform through the diode is measured. The curve can be transformed into voltage shape from the measured IV curve and the absorbed energy by the device can be calculated.

As verification step the proposed analysis method and energy-based failure mechanism are validated with IEC generator using the TLP-test-PCB. Here voltage and current acquisition is possible. Diode destruction is detected measuring leakage current. IEC generator charge voltage is increased in 500 V steps. The measured

critical IEC voltage is 3 kV. Measured, modeled and calculated voltage shapes are compared for IEC discharges in Figure 7.130 and Figure 7.131. The diode was soldered to the TLP-test-PCB without socket. No socket model was considered in simulation.

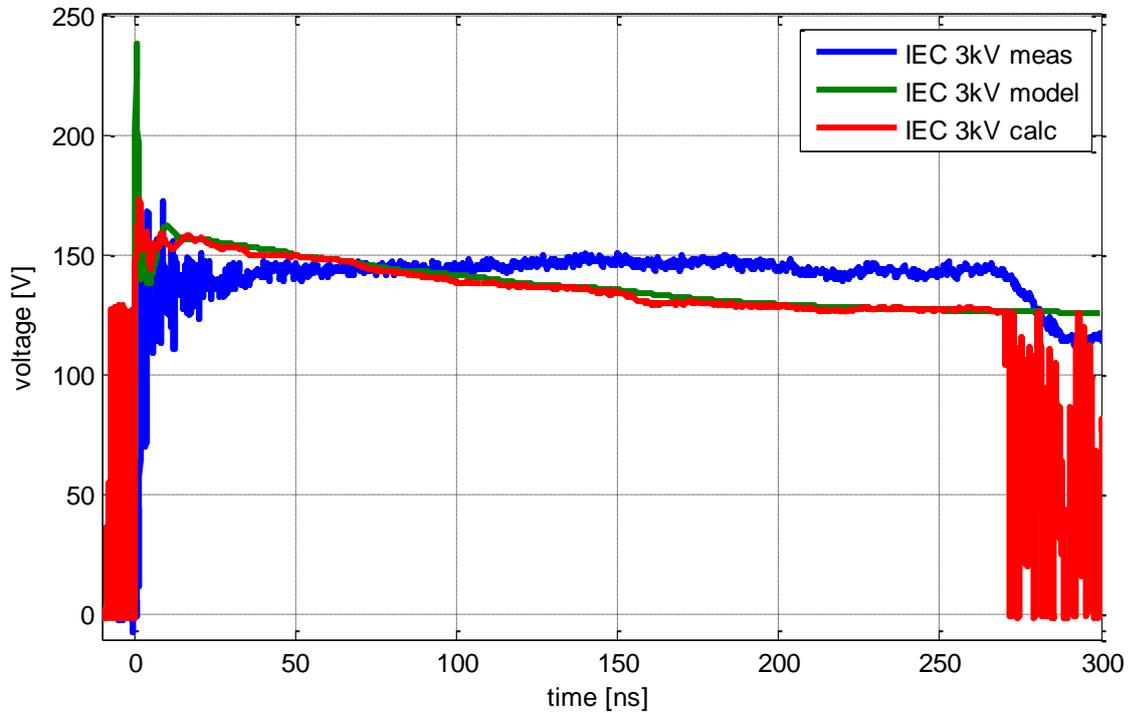


Figure 7.130: Simulated, measured and calculated voltage for BAW156 on TLP-test-PCB

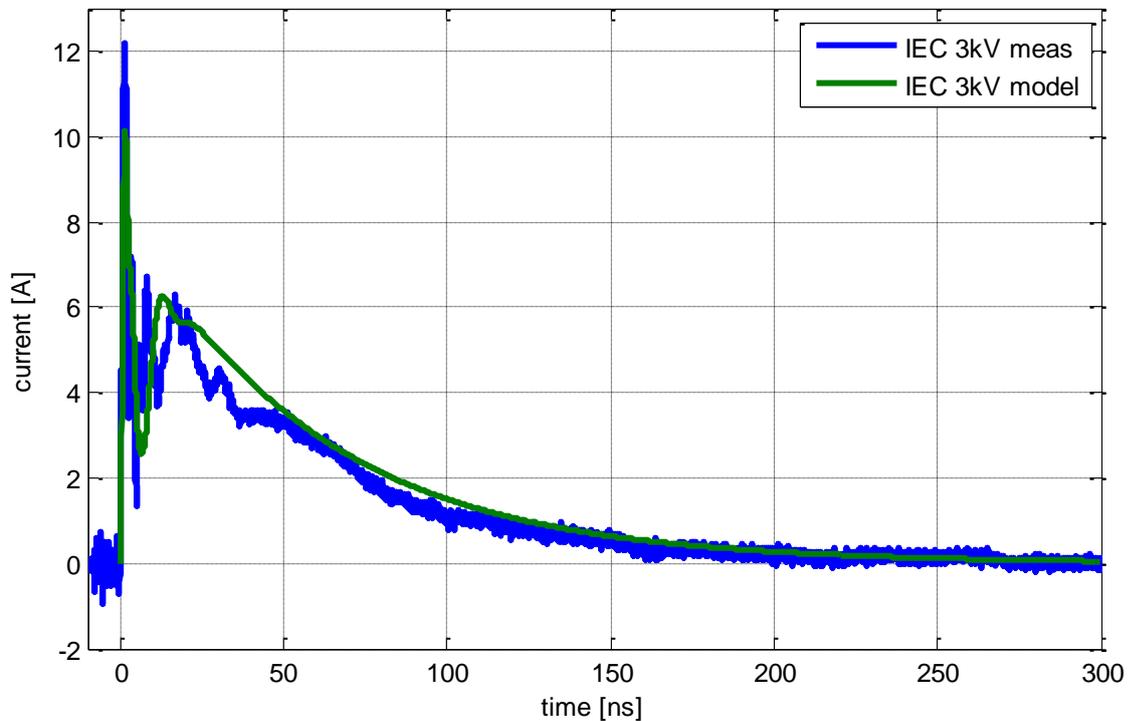


Figure 7.131: Simulated and measured current for BAW156 on TLP-test-PCB

Measured and simulated current and voltage waveforms for the TLP test boards are shown in Figure 7.132 and Figure 7.133.

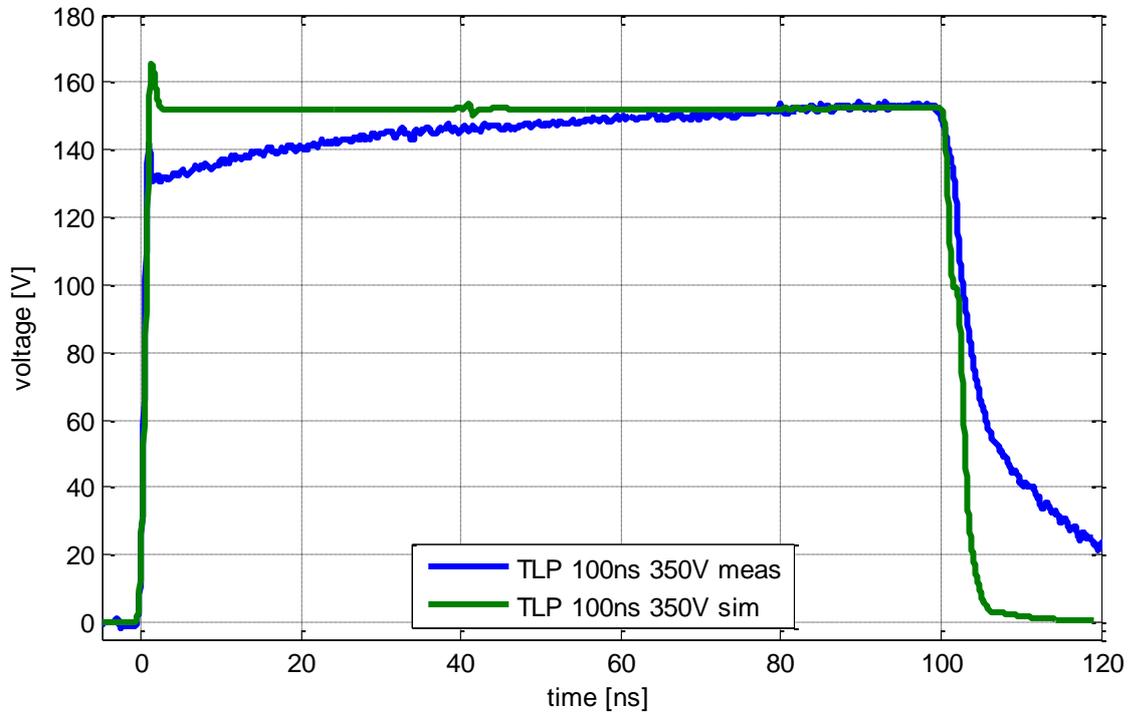


Figure 7.132: Comparison of measured and simulated critical voltage at BAW156 diode

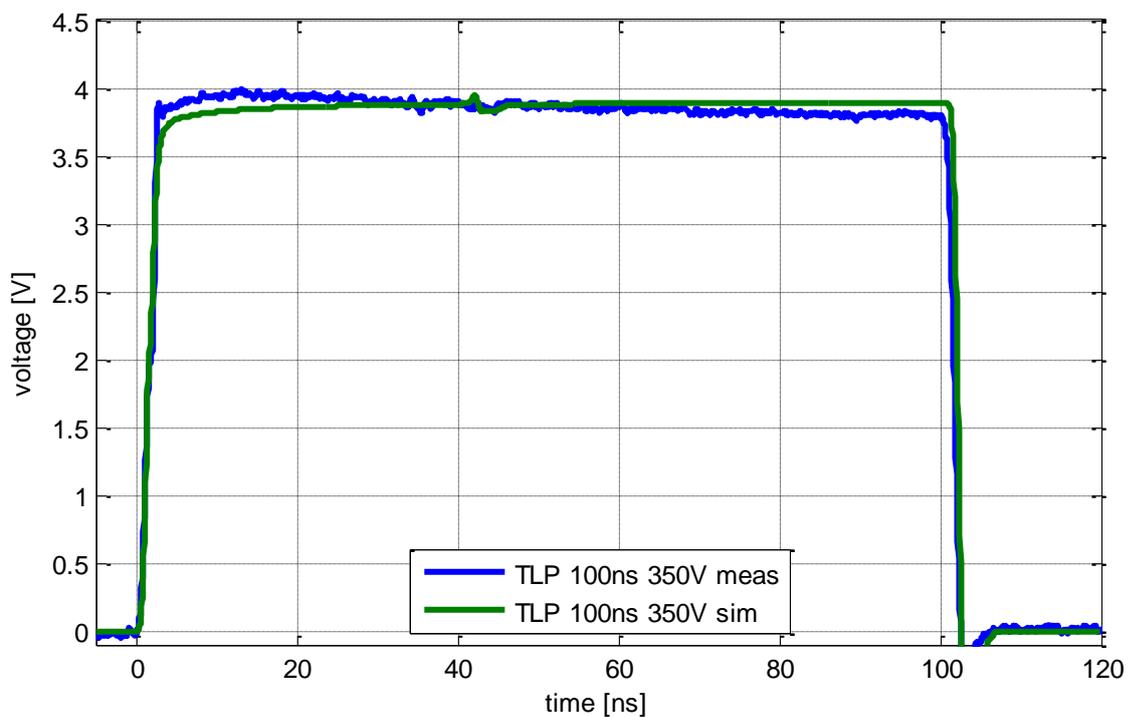


Figure 7.133: Comparison of measured and simulated critical current at BAW156 diode

In Table 7.31 critical signal amplitudes and energies are compared for 100 ns TLP and IEC discharges. Critical failure energies are similar in all cases and an energy based failure mechanism can be assumed.

ESD Generator	V _{charge} [V]	V _{max} [V]	I _{max} [A]	E _{crit} [μJ]
TLP 100ns	350	157	4.05	56.6
IEC	3000	175	12.2	57.6

Table 7.31: Comparison of the failure energy for BAW 156 diode

The calculated value from the measured current shape data shown in Figure 7.131 and the model IV curve is about 54 μJ. Deviation to the measured value is less than 5 %. However, critical energy of the model is set to 57 μJ.

7.6.6.5.2 Rear light LED

Measurement results and a simulated IV curve of the rear light LED are compared in Figure 7.134. Good matching can be obtained for positive and negative TLP charging voltages. The corresponding critical TLP simulation for 100 ns pulse width can be found in Figure 7.135 and Figure 7.136. No IC socket inductance was considered in simulation. For measurement device was mounted on PCB without socket. A good match of the current curve may be observed. The continuous rise of the measured voltage with progress of the TLP pulse is not modeled. A cause could be heating effects in the IC's current path.

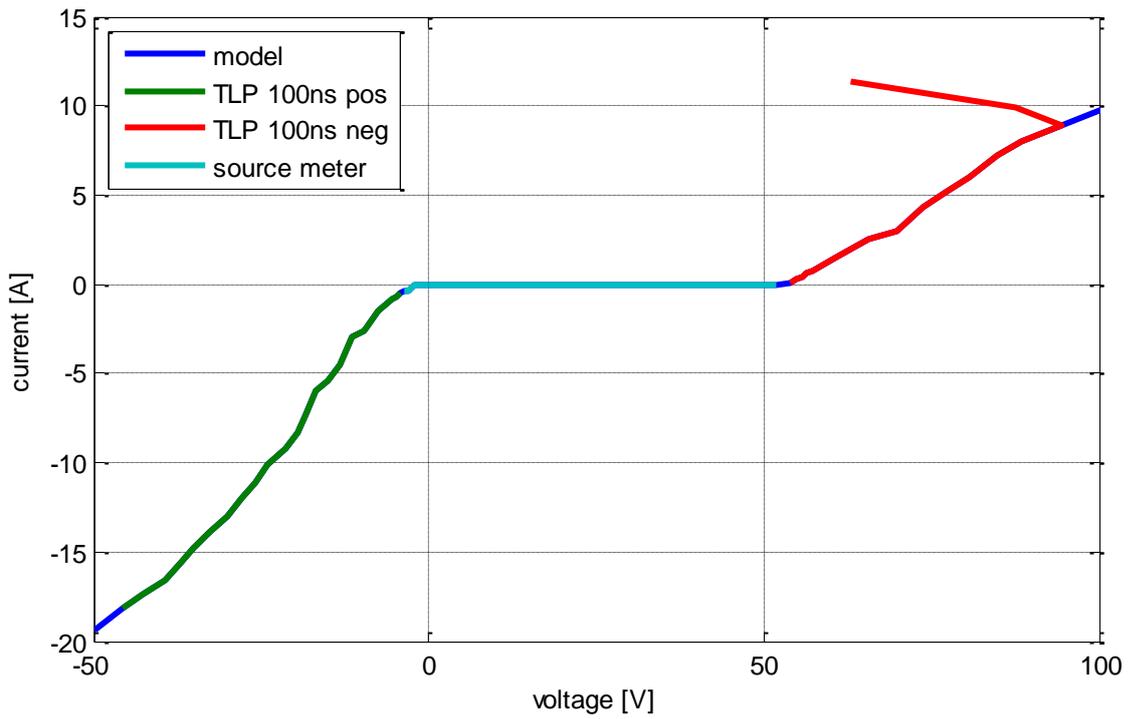


Figure 7.134: Comparison of measured and implemented IV-curve at rearlight LED

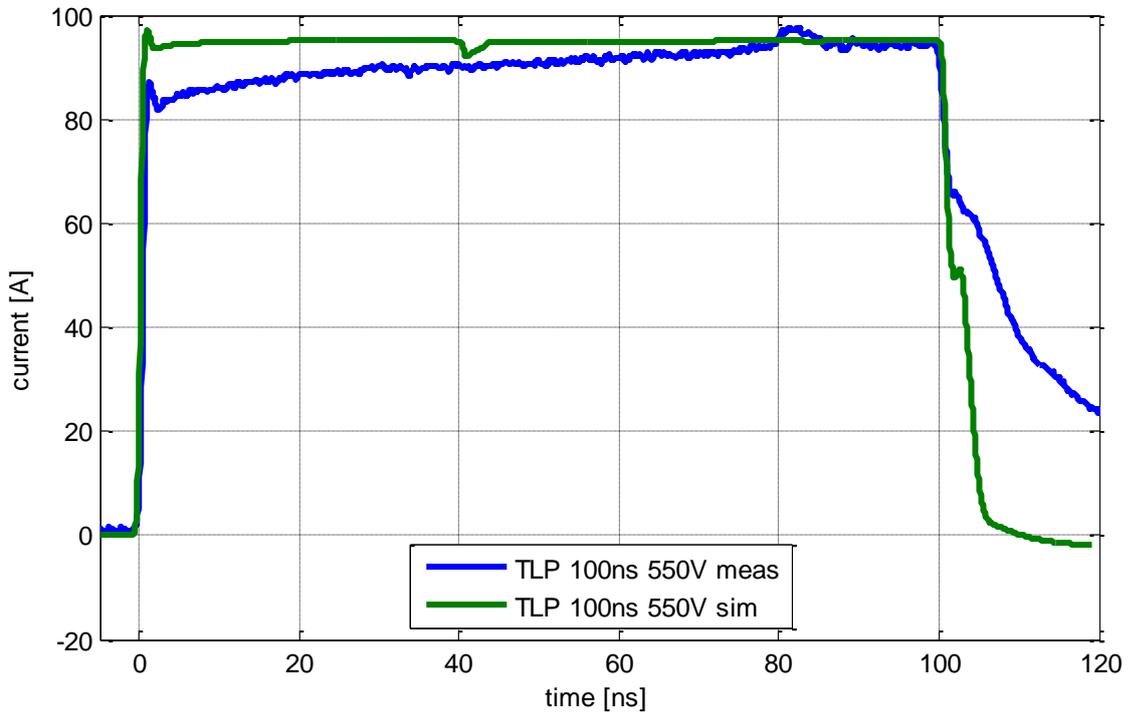


Figure 7.135: Comparison of measured and simulated critical voltage at rearlight LED

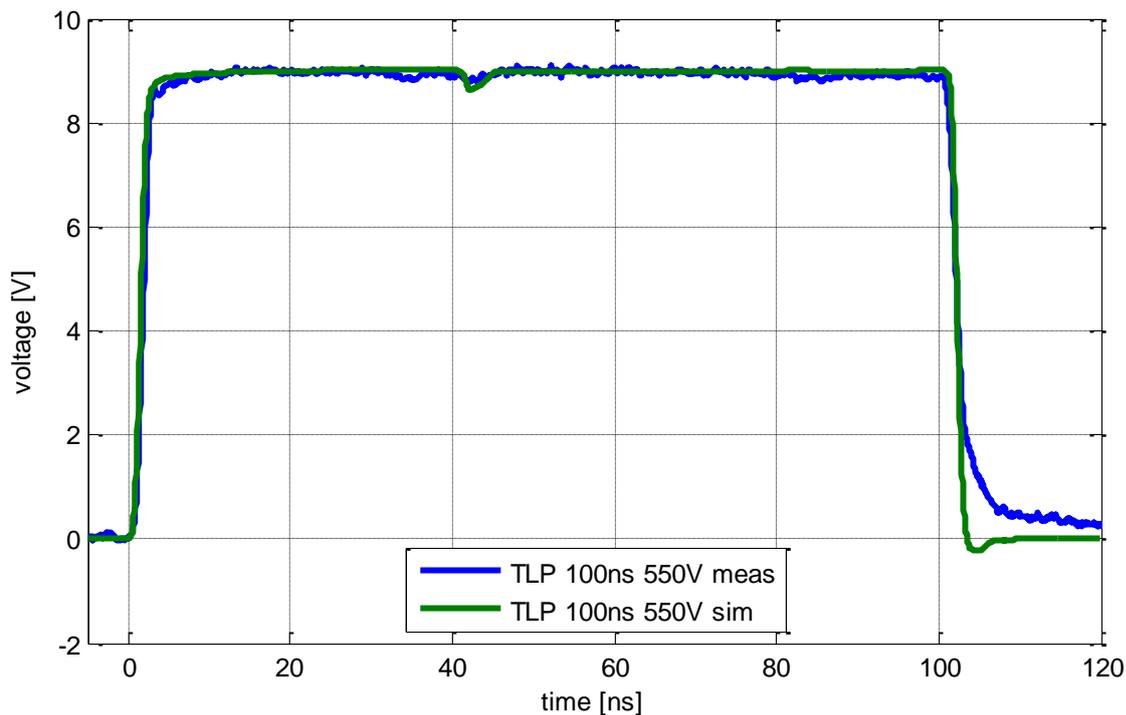


Figure 7.136: Comparison of measured and simulated critical voltage at rearlight LED

7.7 Modeling of Soft Errors

Soft errors are difficult to model in a general format, as they fall into many different classes. For each class a model needs to be derived after characterizing the IC for its soft failure sensitivity for conducted and field coupled noise. The characterization can be very difficult. Scanning methodologies in which fields are coupled into the ICs and currents injected onto PINs can be helpful.

As mentioned soft failures are diverse and triggered by a possibly very low energy portion of the ESD pulse. The underlying causes of soft-errors are often not known. However, one can categorize soft errors by different criterion as given in the next section.

7.7.1 In Band / Out Of Band with Respect to Voltage

For an in band error the noise voltage needs to be larger than VSS and less than VDD, or, for differential signals within the allowed common mode and differential mode voltage swing range. Thus, within the normal operating range of the input. In general, in band errors with respect to voltage add noise and cause signal integrity violations, but the voltages stay within normal operating limits. For an output the current forced into the output needs to be less than the maximal allowed current, and the voltage at the output must be maintained within the normal range of voltages. Most in band errors are caused by voltage changes that allow noise to be confused with legal data. If, for example, the ESD causes the common mode level of a differential mode signal to swing up beyond the maximal common mode range of the

differential input, then this would be considered an out of band soft-error with respect to voltage. If the common mode would swing below VSS or above VDD, then the ESD protection circuit can inject currents into VSS, VDD or the substrate. If the voltages are forced below VSS or above VDD, ESD protection diodes or other ESD protection structures can be forward biased, injecting current into the VDD system, the VSS system or the substrate. Negative voltage pulses will inject into the VSS and/or the substrate, while positive pulses will inject current into the VDD system.

7.7.2 In Band / Out of Band with Respect to Pulse Width

If the intended minimal pulse width is for example 2 ns and an ESD pulse with 2 ns width arrives at the receiver the receiver will confuse the ESD induced voltage for valid data. However, if the same receiver is able to react to a 200 ps wide pulse, although the fastest system signal would have > 2 ns pulse width, then the 200 ps receiver can react to the 200 ps pulse. Such a pulse is considered as an out of band signal with respect to pulse width, as its width is more narrow than the most narrow intended pulse within the system. These types of errors are very common for reset and other status lines, as the input buffers are often much faster than they need to be. Together with long traces, poor routing of status lines over connectors etc., strong coupling paths are formed between the ESD pulse and the receiver causing the receiver to react to a very narrow pulse. Low pass filters at the IC input can help to improve the situation.

A couple of mechanisms can potentially lengthen the pulse width of ESD pulses. For example, the interconnect inductance together with the input capacitance forms a linear low pass filter. Furthermore, reverse recovery of forward biased diodes, especially if they are forward biased by a large ESD current are examples of such mechanisms.

7.7.3 Local vs. Distant Errors

A local error is caused by changes in the IO buffer which receives the ESD, a distant error is caused by changes far away from the IO buffer that received the ESD. For example, if a negative pulse opens a PN diode and leads to an injection of charge carriers into the substrate, and this current disturbs an XTAL input PIN at a different IO, then this would be considered a distant error. The same is true for a positive pulse injected into an output which forces current into VDD. This current leads to voltage drops within the VDD system and can cause an error at a level translator, or a PLL away from the output.

7.7.4 Amplified / Non-Amplified Soft Errors

Amplified soft errors involve transient latch-up, or the trigger of power clamps, while non-amplified soft errors are caused by voltage changes, IR drop, cross coupling without triggering high current devices. Ringing pulses can lead to fast transient latch-up. The fast transient latch-up can have many different consequences, from

increased current consumption with no direct effect on functionality, to increased current consumption with soft error, to destruction of the IC. Another example of an amplified soft error is the trigger of a power clamp. This can again have multiple consequences. If the holding voltage is higher than VDD, the power clamp will recover after some time. During this time VDD is reduced, the ICs logic can be disturbed, but the IC will survive. If the holding voltage is below VDD the IC will try to pull VDD down. Depending on the power supply this can destroy the IC.

8 Analysis of ESD-Critical Configurations

8.1 Cable Discharges

Many ESD failures, occurring during automotive manufacturing process or during application by the end-user, cannot be associated with a human discharge. The attempt to handle the problem by increasing ESD testing levels can lead to overdesign and high costs if individual characteristics of ESD events are neglected. During production electronic systems can be affected by Cable Discharge Events (CDE), which can occur when charged cable bundles from the automotive cable harness are connected to electronic devices.

8.1.1 Cable Discharge Parameters

8.1.1.1 Rise Time

The rise time is an important criterion of the pulse. Rise time of the pulse is responsible for e.g. capacitive coupling. Protection element response for a fast slope may be delayed according to its parasitic inductance and a critical voltage peak may reach a sensitive IC pin. The rise time for IEC discharges is given in the ISO/IEC standards with a range from 0.7 to 1 ns. Cable discharges show rise times of much less than 0.5 ns [6]. The rise time is mainly limited by the inductance of the discharge tip.

8.1.1.2 Pulse Width

The pulse width for a cable discharge depends on the wire length l and the relative permittivity of dielectric ϵ_r [6].

$$t_{pulse} = \frac{2 \cdot l_{wire} \cdot \sqrt{\epsilon_r}}{c} \quad 9$$

Figure 8.1 evaluates equation 9 for different wire parameters.

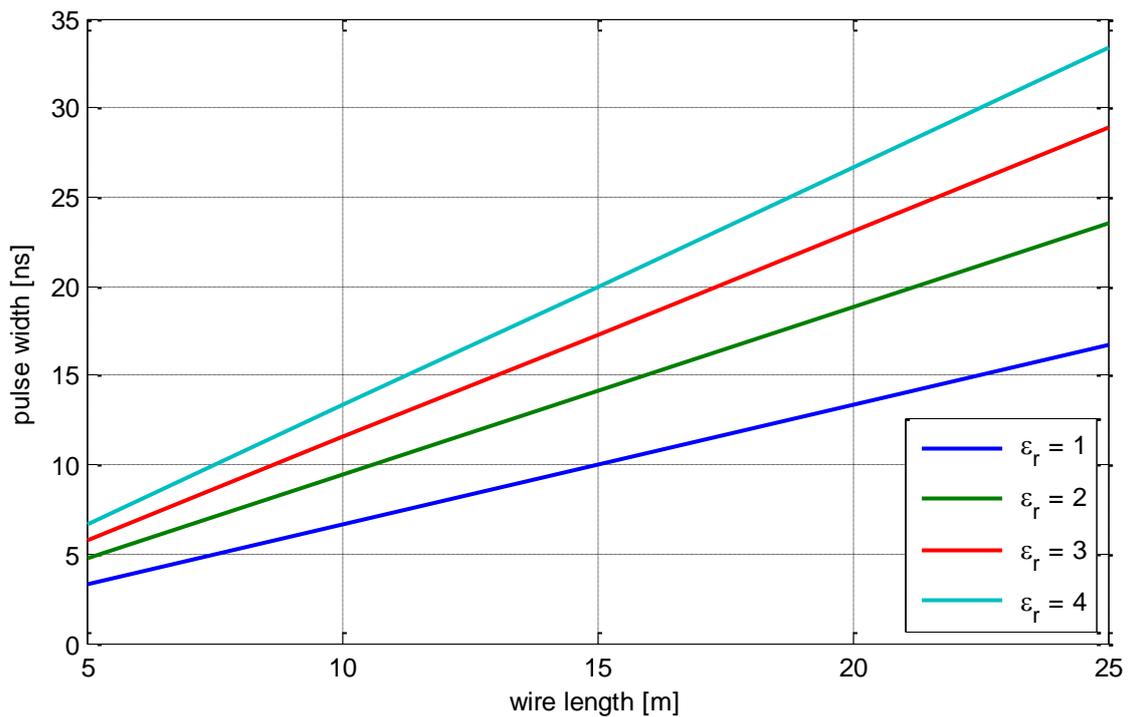


Figure 8.1: Pulse width for different cable parameters

8.1.1.3 Energy

For thermal failure mechanism of an IC the amount of absorbed energy is important. If the impedance of the DUT is equal to the wire impedance no reflections occur and the energy can be absorbed by the DUT in only one pulse duration. Otherwise reflections will occur. The energy of the first pulse of a lossless wire can be approximated with assumption that no energy is radiated:

$$E_{DUT_wire} = \int V_{DUT} \cdot I_{DUT} dt$$

$$E_{DUT_wire} = \int V_{DUT} \cdot \frac{V_{DUT}}{Z_{DUT}} dt$$

10

$$\text{with } V_{DUT} = V_{wire} \cdot \frac{Z_{DUT}}{Z_{DUT} + Z_{wire}}$$

$$E_{DUT_wire} = \left(V_{wire} \cdot \frac{Z_{DUT}}{Z_{DUT} + Z_{wire}} \right)^2 \cdot \frac{1}{Z_{DUT}} \cdot t_{pulse}$$

The parameters are:

- V_{wire} wire voltage
- Z_{DUT} DUT impedance
- Z_{wire} cable impedance
- t_{pulse} pulse width

Equation 10 can be simplified for a matched DUT impedance.

$$\text{with } Z_{DUT} = Z_{wire}$$

$$E_{DUT_wire} = \left(\frac{V_{wire}}{2}\right)^2 \cdot \frac{1}{Z_{DUT}} \cdot t_{pulse} \quad 11$$

The line impedance of wires within a harness can vary in a wide range. A value of 260 Ω with a relative permittivity $\epsilon_r \approx 1$ can be seen as typical. For a 260 Ω DUT no reflections will occur and the discharge energy will be transported in one pulse.

The energy of an IEC generator is stored in the capacitor of the discharge network:

$$E_{GEN} = \frac{1}{2} C_{GEN} V_{GEN}^2 \quad 12$$

If the radiated energy and other losses are not considered, the energy absorbed by a DUT can be expressed by equation:

$$E_{DUT_IEC} = \frac{1}{2} C_{GEN} V_{GEN}^2 \cdot \frac{R_{DUT}}{R_{GEN} + R_{DUT}} \quad 13$$

For a 8 kV IEC discharge with 330 Ω/ 150 pF network into a 260 Ω DUT the calculated discharge energy is:

$$E_{DUT_IEC} = 2.115 \text{ mJ} \quad 14$$

To provide the same energy on the 260 Ω DUT as an IEC generator either the wire length or the charge voltage can be adjusted. Figure 8.2 compares energies of cable discharges to an IEC discharge. The curve of a 260 Ω, 5 m wire matches well the IEC curve. For a charge voltage of 4 kV, 20 m wire length is required.

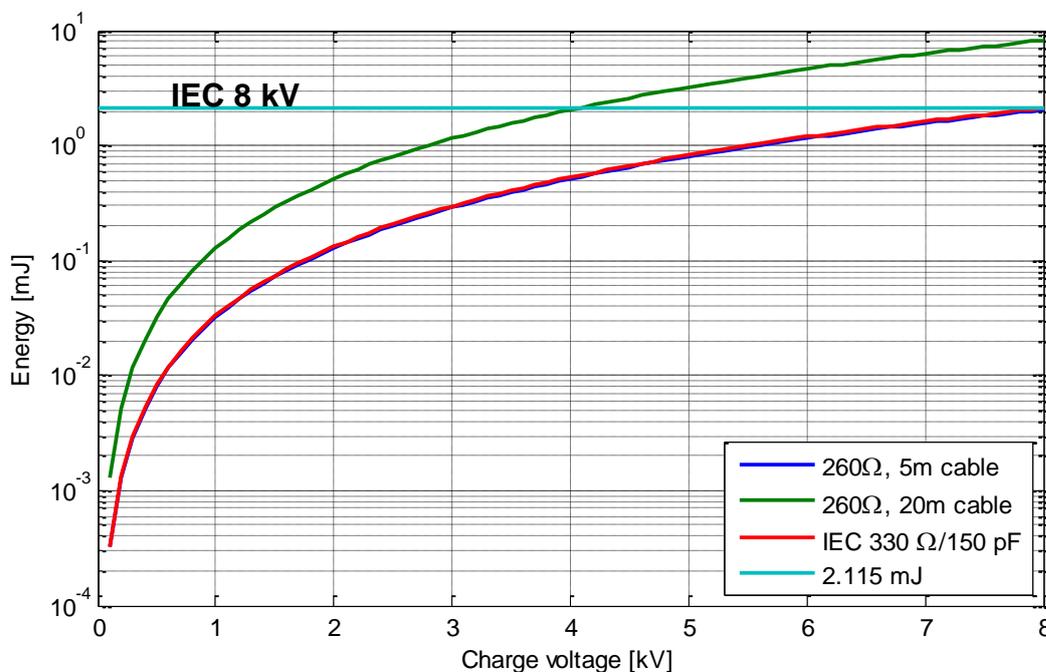


Figure 8.2: Energy of cable discharges (260 Ω impedance) over charge voltage compared to an IEC discharge on 260 Ω DUT

8.1.2 Cable Discharge Generator

The cable discharge characteristics can be reproduced with a cable discharge board. For easy handling the dimensions of the board are minimized using a single-sided PCB with a meander-shaped trace instead of a straight wire. Copper trace of 35 μm thickness and 5 mm width is used. The overall length is 1.4 m. Rectangular trace routing is avoided to minimize reflections. The trace is charged by a high voltage DC source over a large resistor (here 20 M Ω were used, larger values might be better). The resistor decouples the DUT from the source when discharging. A 25 mm discharge tip with a spring establishes connection to the DUT without causing mechanical tension. Figure 8.3 shows the generator.

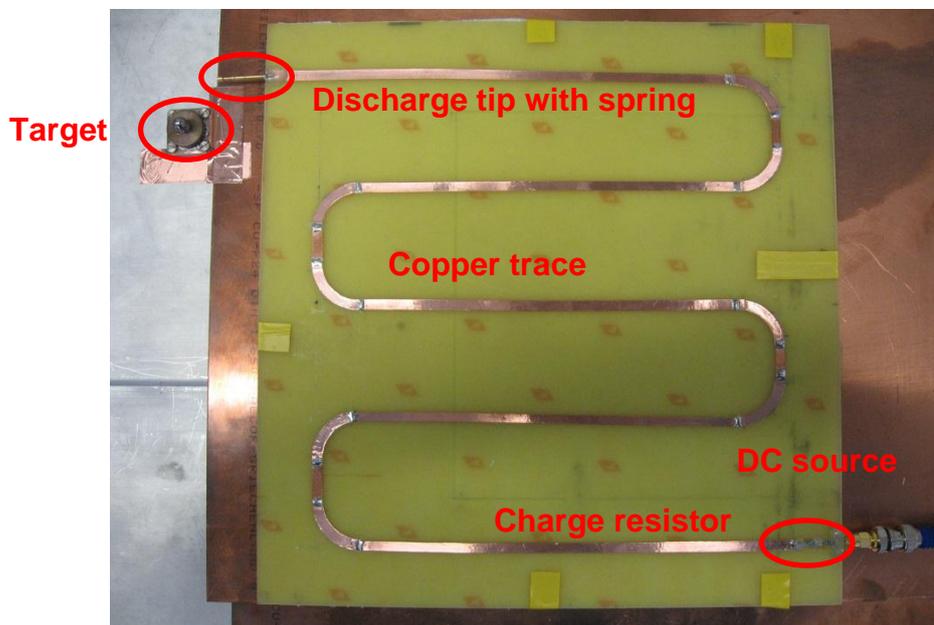


Figure 8.3: Cable discharge generator

8.1.3 Test Set Up

For measurements the cable discharge generator is positioned on styrofoam isolated from HCP. The height over the HCP is 12 mm. The trace impedance of 176 Ω is calculated with an analytical formula. A DC high voltage source charges the trace. The pulse is acquired by a shunt current target with a resistance of 2 Ω and a 6 GHz oscilloscope. Figure 8.4 gives an overview of the used set up. The pulse is triggered by manually moving the PCB to the current target.

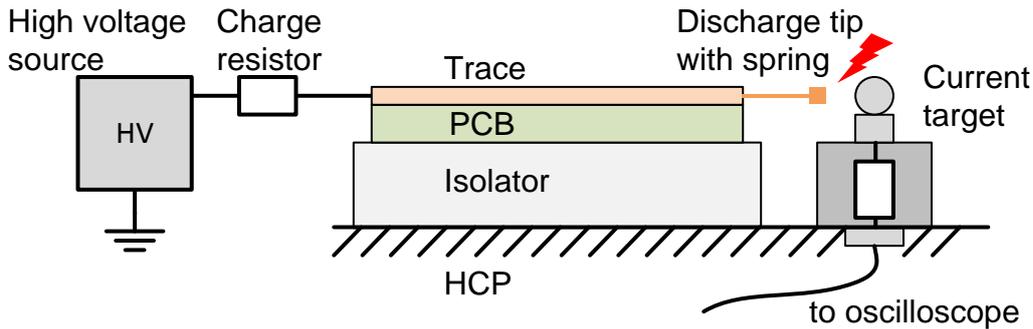


Figure 8.4: Test set up for cable discharge

8.1.4 Measurement Results

8.1.4.1 Rise Time

Figure 8.5 shows the first slope of the three measured discharges. The measured rise time is about 125-200 ps, this is ca. 5 times faster as the IEC discharge. Good reproducibility of the curve shape is given for 1 kV discharge.

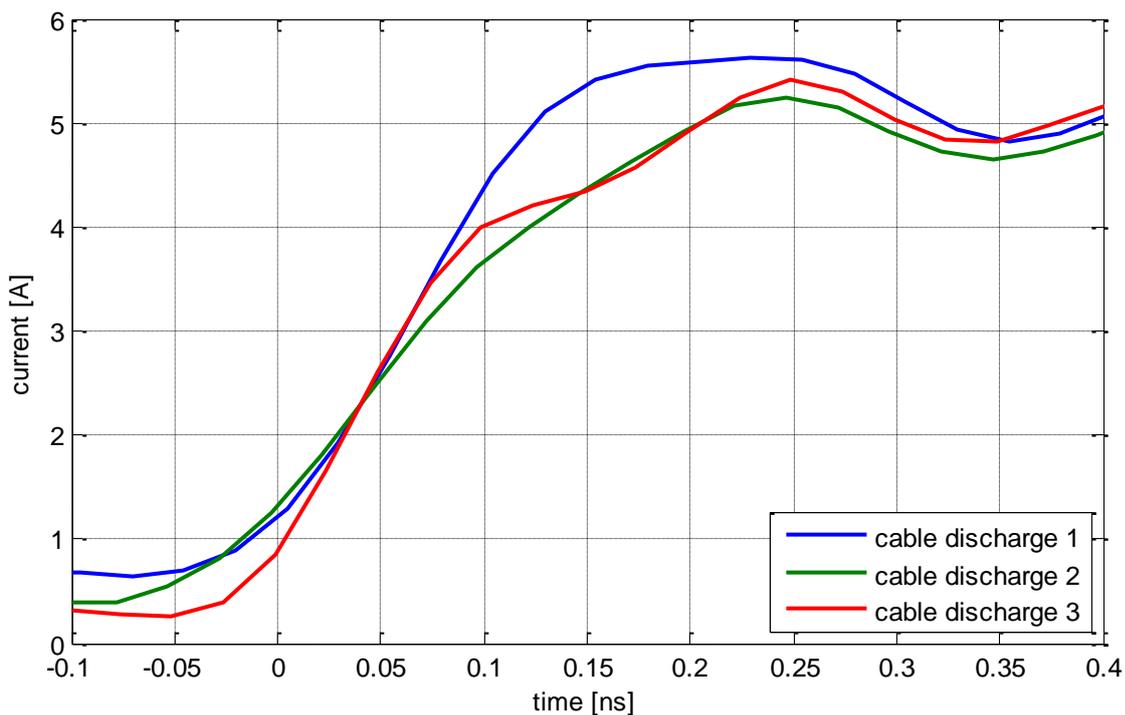


Figure 8.5: Rise time reproducibility of a 1 kV cable discharge measured on 2 Ω target

8.1.4.2 Energy

The current shapes of three 1 kV demonstrator discharges are compared in Figure 8.6. Because of difference in demonstrator impedance and current target impedance reflections can be seen. The maximum current amplitude is 6.4 A.

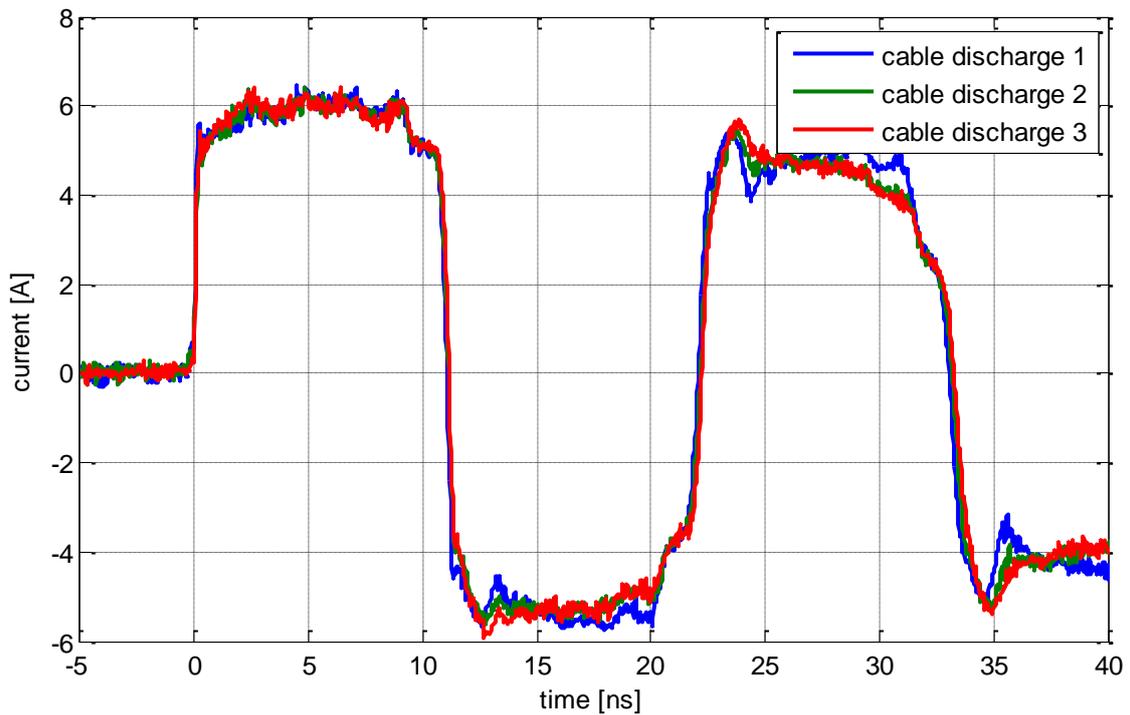


Figure 8.6: 1 kV demonstrator discharge on 2 Ω current target

The energy of the first pulse can be calculated by equation 10. Table 8.1 compares the measured energy of the first pulse to the estimation. The maximum difference is only 3.4 %.

	Measurement			Estimation
	1	2	2	
Energy	714.0 nJ	706.9 nJ	719.6 nJ	694 nJ
Deviation	2.9 %	1.9 %	3.4 %	0 %

Table 8.1: Comparison of estimated and measured energy of the first pulse of cable discharge

8.1.5 Conclusions

The electronic devices of an automotive control unit can be disturbed by cable discharges. Wire length up to several meters can be found in vehicle harnesses. For a 5 m, 260 Ω wire the energy is comparable to an IEC discharge. Parasitic inductances can make filters inefficient for a cable discharge because of fast rise times smaller than 200 ps. These characteristics can be a serious threat to electronic devices.

8.2 ESD-Field-Coupling into Cable Harness

Due to short rise times and high amplitudes an ESD event is attended by strong electromagnetic fields. Especially in case of direct discharge of a charged part into a car body or trailer body critical voltages can couple in wires close to the discharge point. Usually pulse energy and amplitudes are lower than in case of a direct ESD. But very short rise times and sequences of positive and negative current amplitudes of typical waveforms conducted to an ECU can cause soft errors in communication systems or transient latch-up.

8.2.1 Field Coupling between ESD Generator and Transmission Line

IEC 61000-4-2/ISO 10605 ESD generators are widely used for testing. Characteristics of the waveform are standardized representing a discharge of a human via a piece of metal as a typical ESD event. The immunity of electronic systems to ESD field coupling can be tested using an ESD generator which is discharged on a coupling plane or housing. In the testing standard ISO 10605 a powered-up test for indirect ESD is described [5].

Field coupling between ESD generators and cables can be simulated using a multi-port model which is described in section 7.5. In the setup shown in Figure 8.7 an ESD generator is discharged on a coupling plane. Coupled currents flow in a transmission line of 1 m length which is located 3 cm above the ground plane and 3 cm away from the discharge point. One ending of the cable is permanently connected to 50 Ω. The second ending can be used for attaching arbitrary loads.

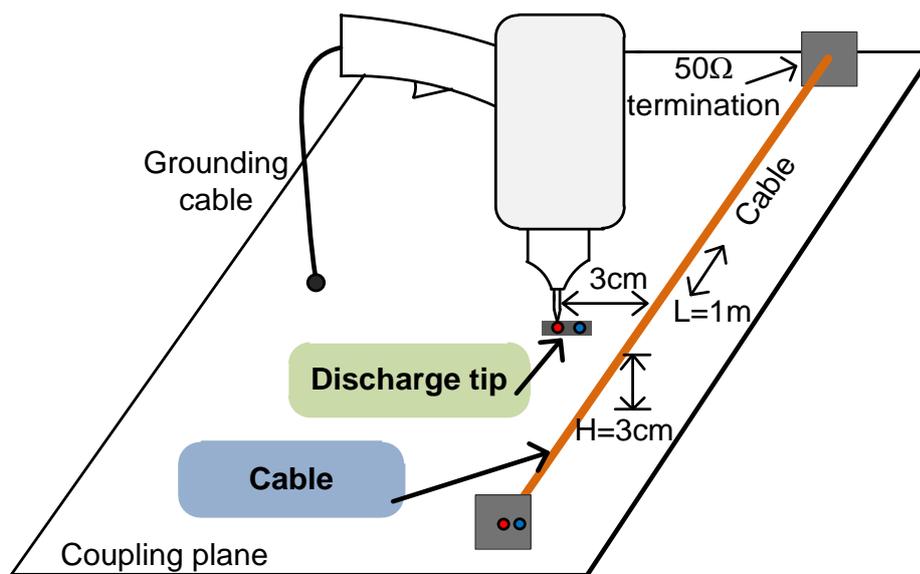


Figure 8.7: ESD generator-cable configuration for ESD coupling simulation

8.2.1.1 Investigation of RLC Circuit as Termination

A circuit consisting of serial resistor, inductor and capacitor can be used to estimate possible disturbance of communication systems by ESD field generated currents. Current through and voltage over a 10 pF capacitor representing the capacitance of e.g. a logic input are simulated with the configuration shown in Figure 8.8.

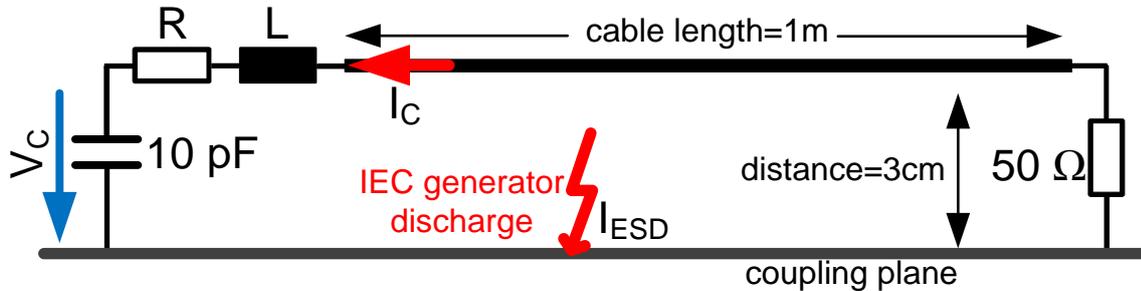


Figure 8.8: Simulation setup for analysis of ESD field induced currents in a cable

The waveforms at the capacitor are simulated for different values of the IC input resistance represented by R. The inductor L was set to 5 nH. Plots for voltage and current shapes at 10 pF and resistance of 10 Ω to 10 kΩ are shown in Figure 8.9 and Figure 8.10 for 1 kV charging voltage. Highest amplitudes around 10 V and 180 mA are obtained in case of R = 10 Ω. Rise times around 500 ps – 1 ns are simulated.

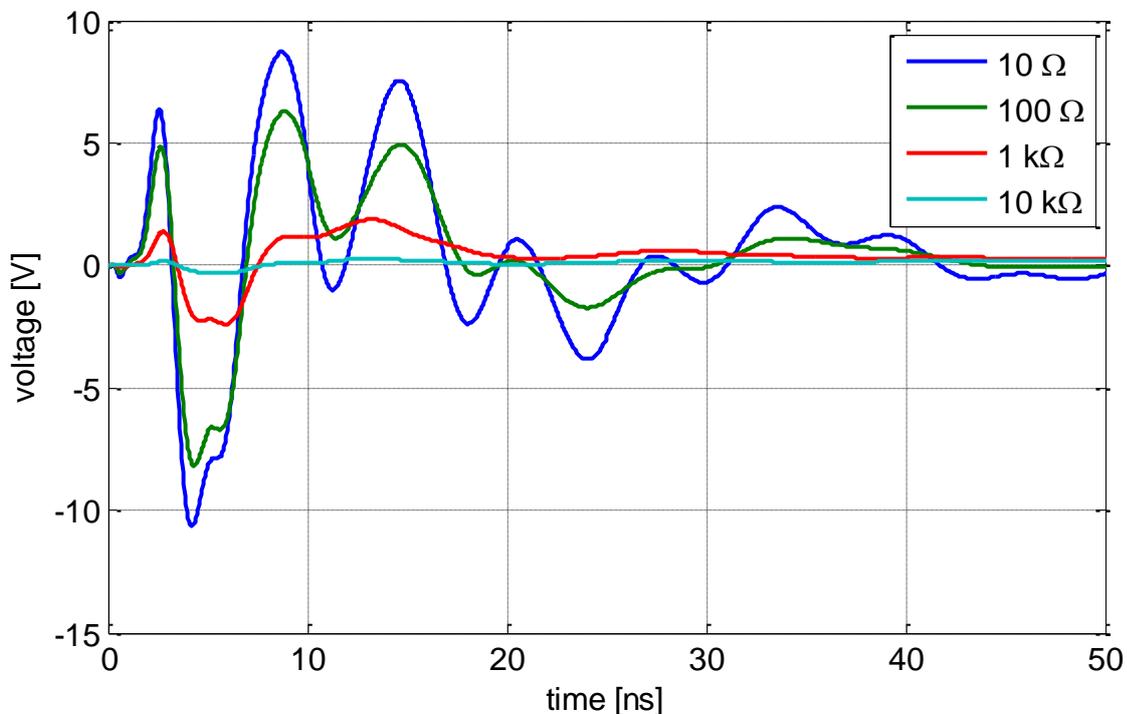


Figure 8.9: Simulated voltage over 10 pF and different resistance values for 1 kV charging voltage

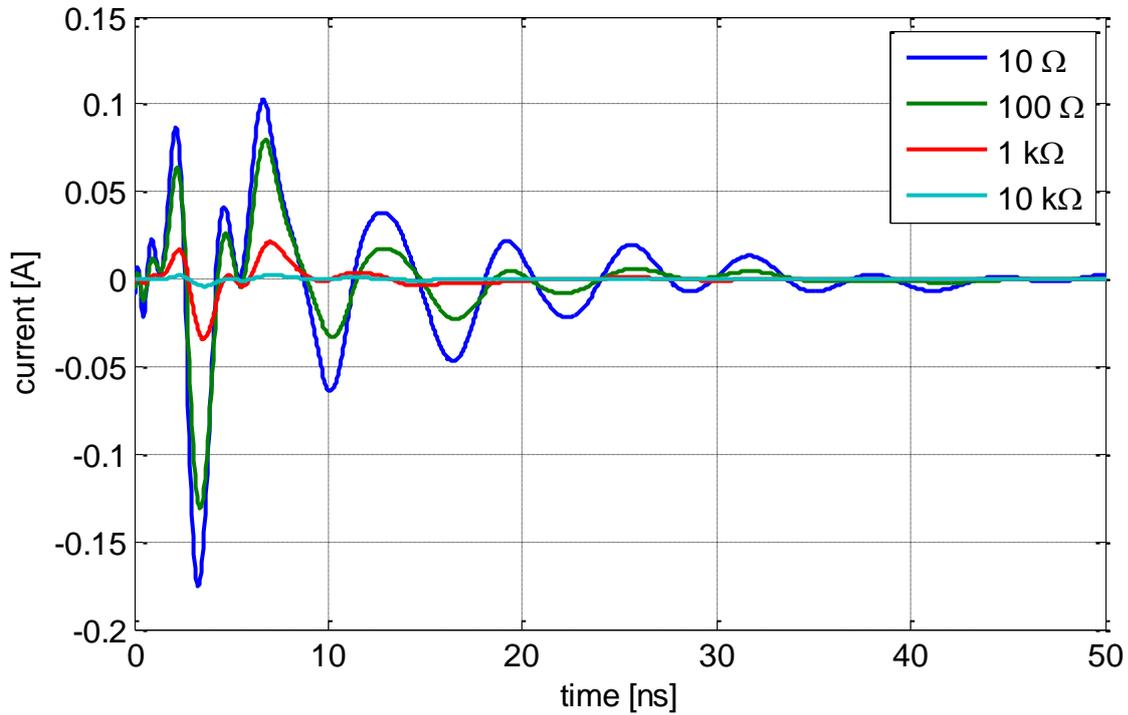


Figure 8.10: Simulated current at 10 pF and different resistance values for 1 kV charging voltage

Maximum amplitudes at the capacitor are presented for different charging voltages in Figure 8.11 and Figure 8.12. All amplitudes increase linear with charging voltage for different values of R. In case of R = 10 kΩ 1,5 V and 20 mA were simulated for 5 kV charging voltage. If R is set to 1 kΩ, voltage level reaches more than 10 V. Disturbance of electronic systems is possible at this level.

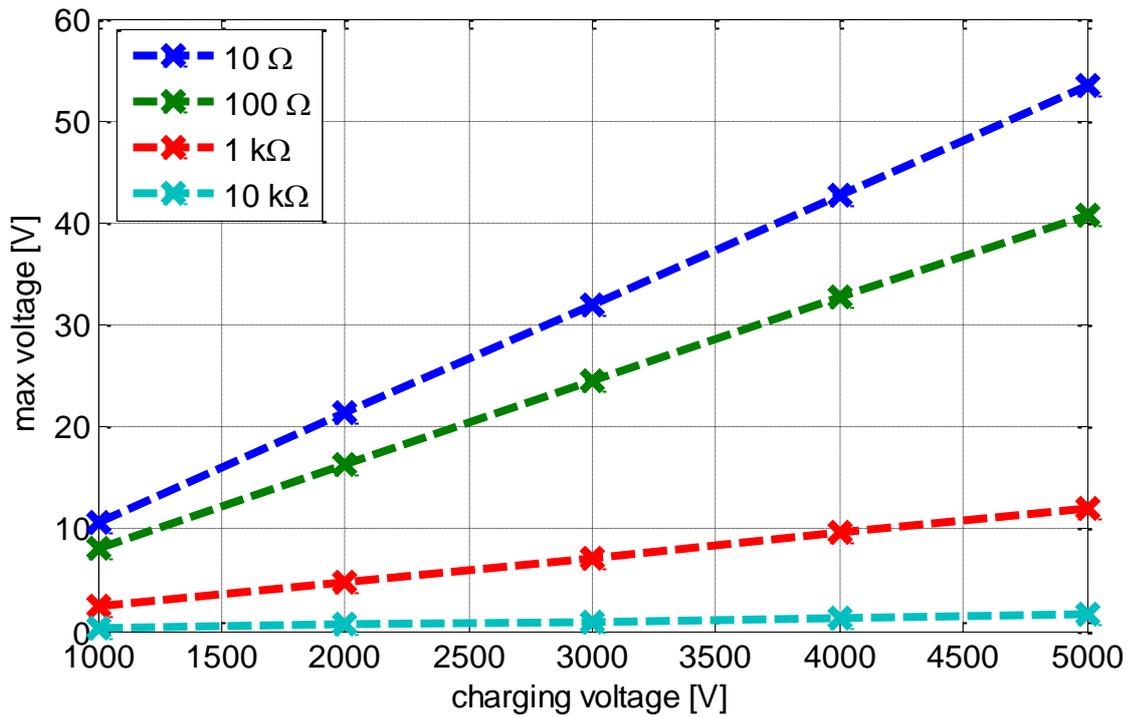


Figure 8.11: Maximum voltage over 10 pF and different resistance values over charging voltage

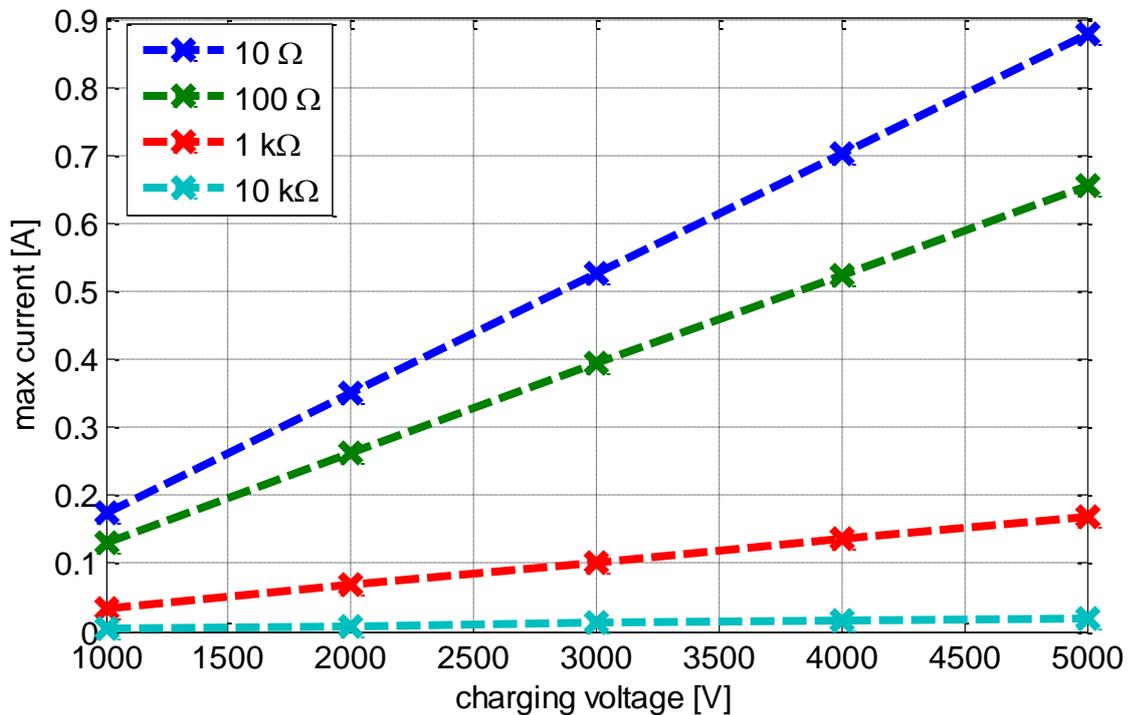


Figure 8.12: Maximum current at 10 pF and different resistance values over charging voltage

8.2.1.2 Impact of Inductance on Field Coupling

The influence of inductance L on the voltage and current at the 10 pF capacitor in Figure 8.8 in case of ESD field coupling is analyzed. Simulated waveforms are given in Figure 8.13 Figure 8.14 for $R = 10 \Omega$ and variation of L between 5 nH and 1 μH .

Amplitudes decrease with rising inductance. Rise times are increased from 500 ps to few ns for high inductance value. Peaks of wave shapes are delayed.

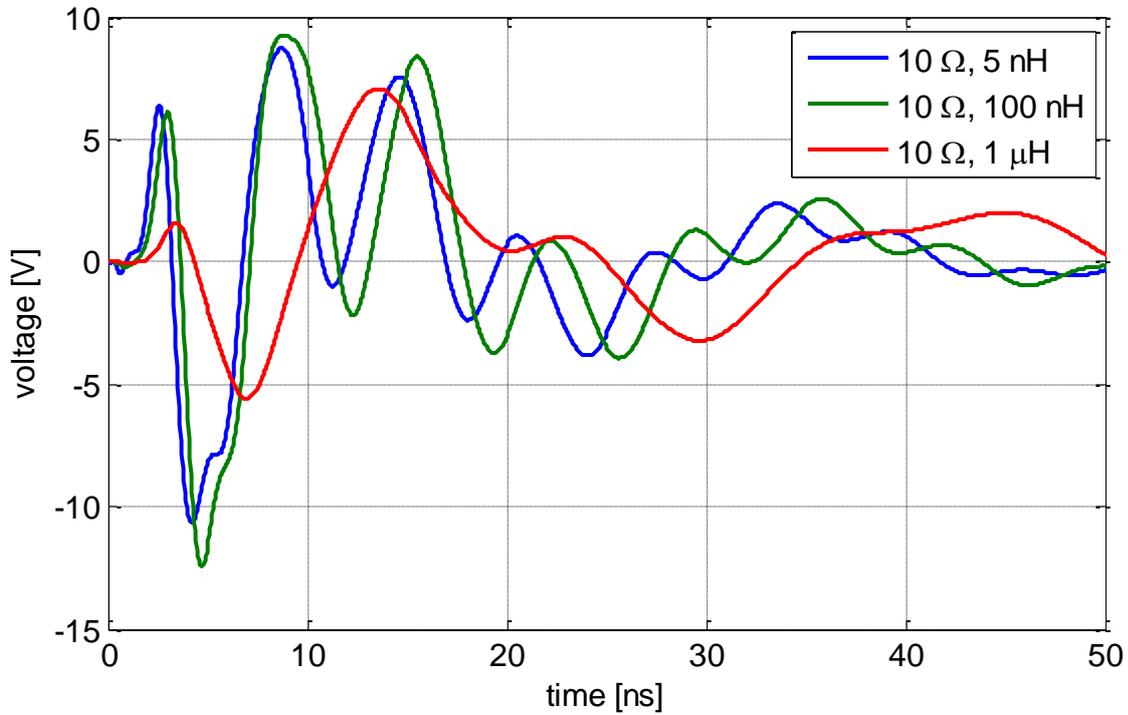


Figure 8.13: Simulated voltage over 10 pF and different inductance values for 1 kV charging voltage

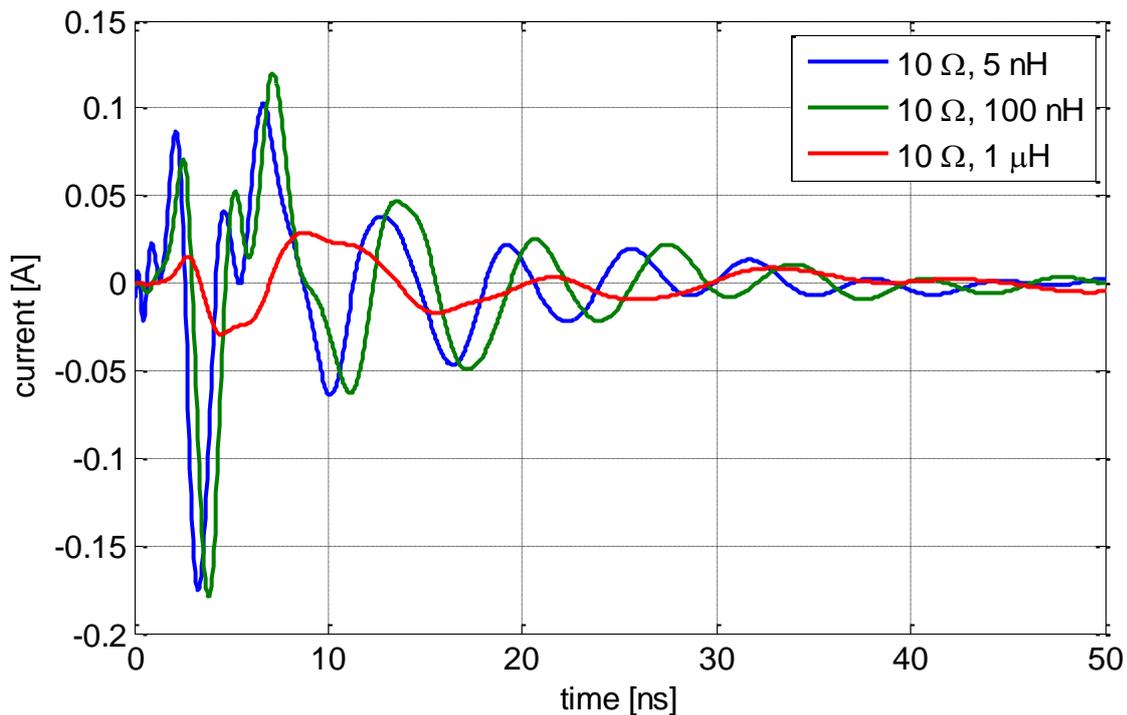


Figure 8.14: Simulated current at 10 pF and different inductance values for 1 kV charging voltage

Maximum voltage and current values are given in Figure 8.15 Figure 8.16 for the 10 Ω and different inductances. Similar to variation of values of R amplitudes are increasing linear with the charging voltage of the ESD generator that is discharged into the coupling plane. For R = 10 Ω the simulated voltage could be decreased by 50 % to 35 V for 5 kV charging voltage if L is increased from 5 nH to 1 μH. In case of the current a factor 6 was obtained.

Very low impact of the inductance on the peak value was observed for high input resistance. Maximum amplitudes over charging voltage are given in Figure 8.17 and Figure 8.18 for 10 kΩ and different values of L. Deviation between amplitudes is less than 4 %.

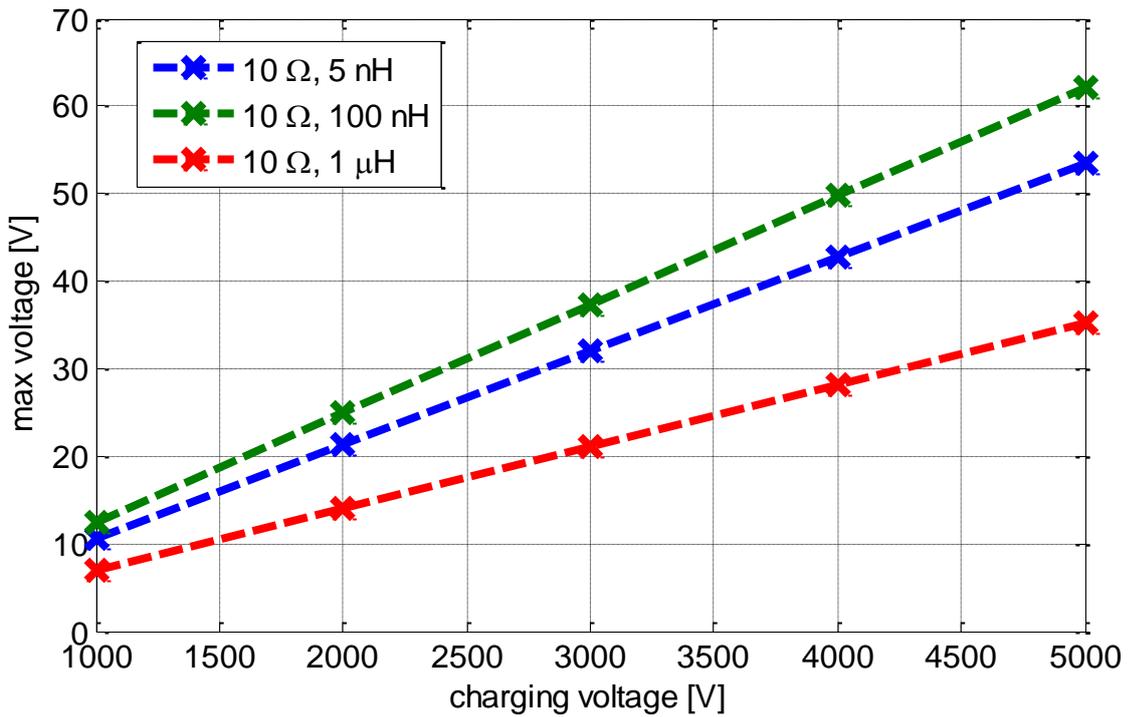


Figure 8.15: Maximum voltage amplitude for different inductance over charging voltage

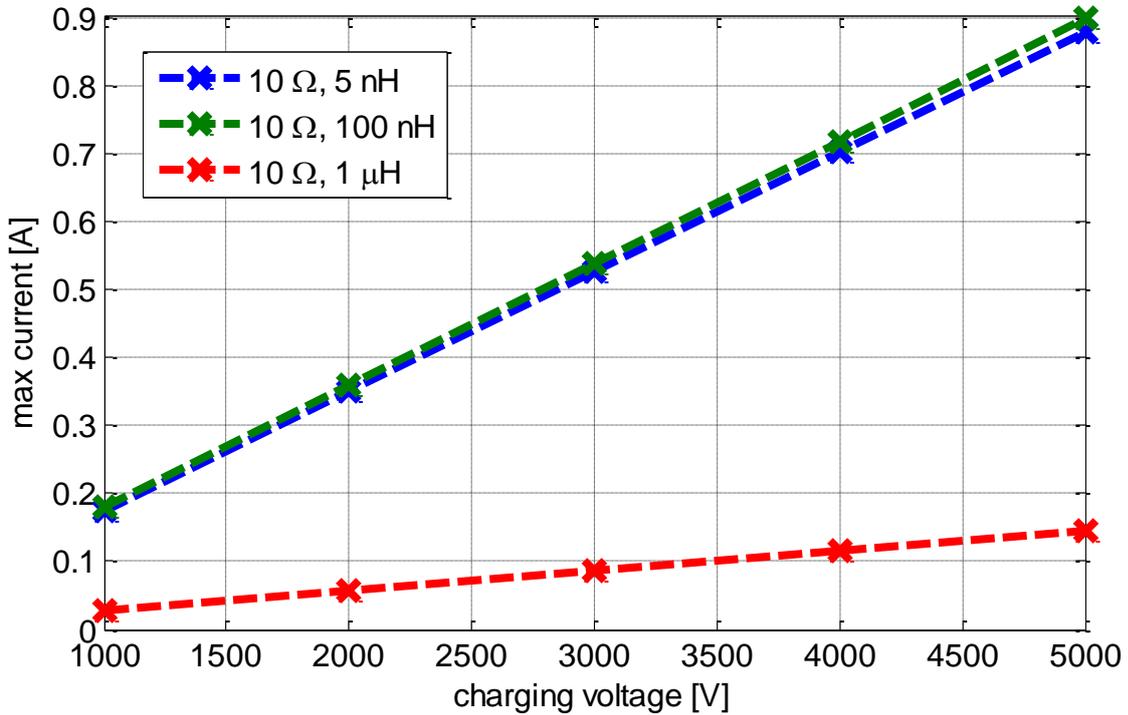


Figure 8.16: Maximum current amplitude for different inductance over charging voltage

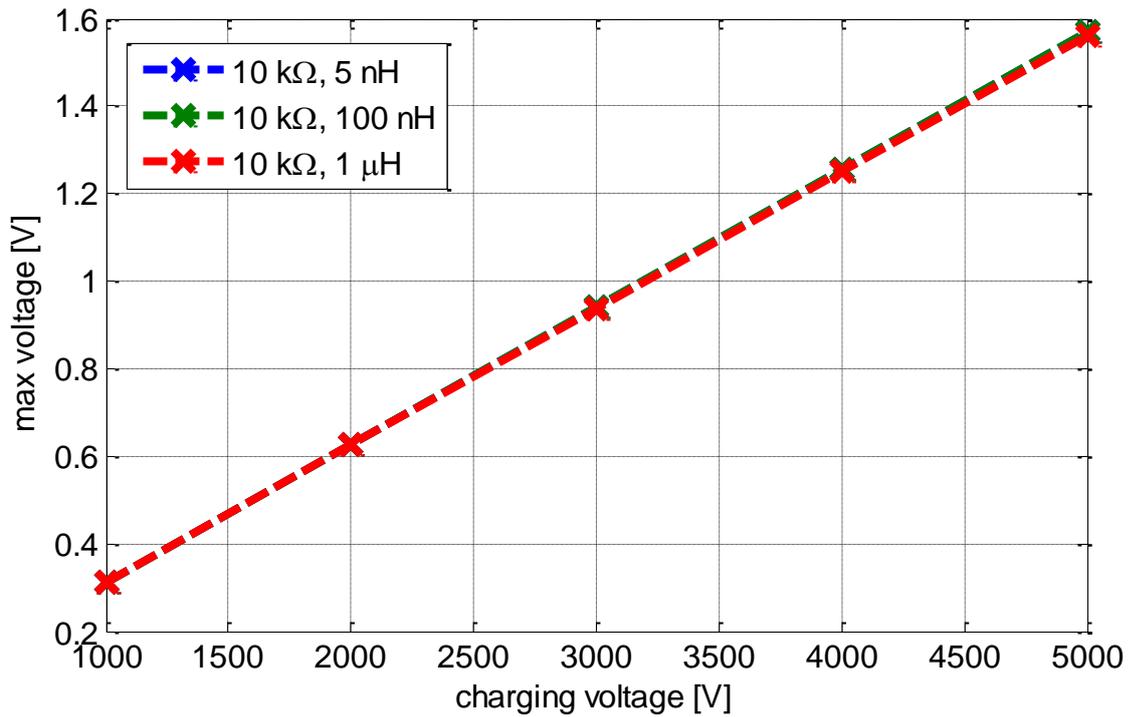


Figure 8.17: Maximum voltage amplitude for different inductance and $R = 10\text{ k}\Omega$

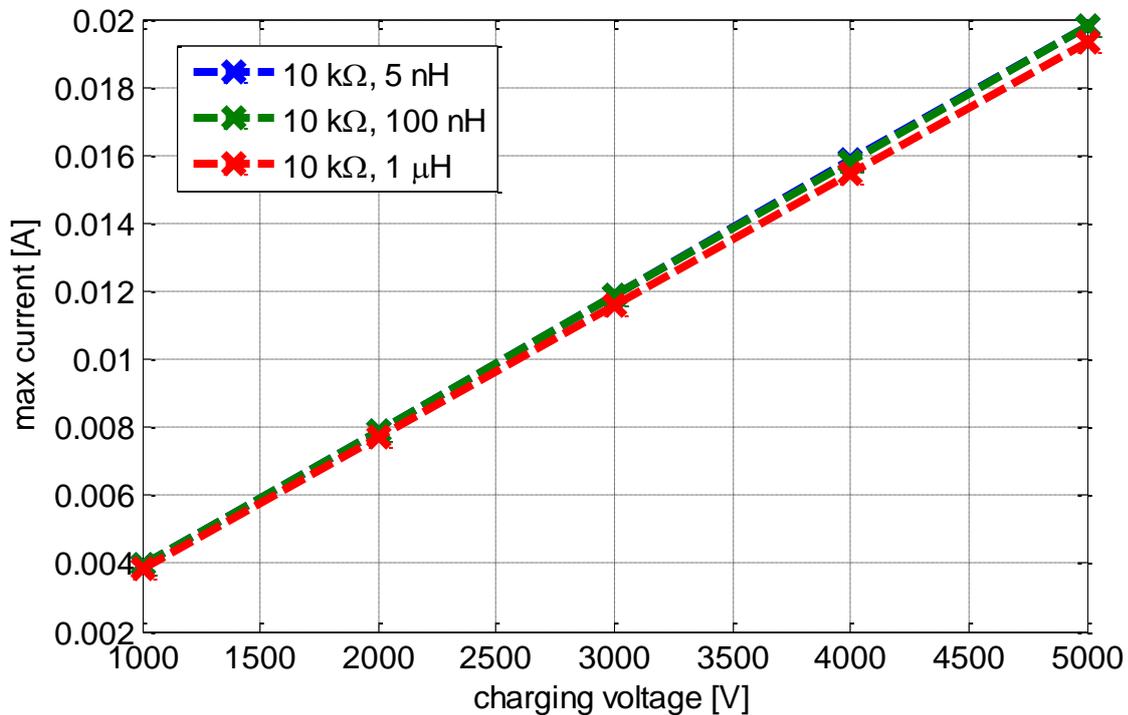


Figure 8.18: Maximum current amplitude for different inductance and $R = 10\text{ k}\Omega$

8.2.1.3 Simulation with IC Models

ESD field coupling is simulated using models of TJA1041T CANH pin and $\mu\text{C XC864}$ data pin which are connected to the cable ending. Details of IC models can be found in section 7.6.5. A sketch of the setup is shown in Figure 8.19.

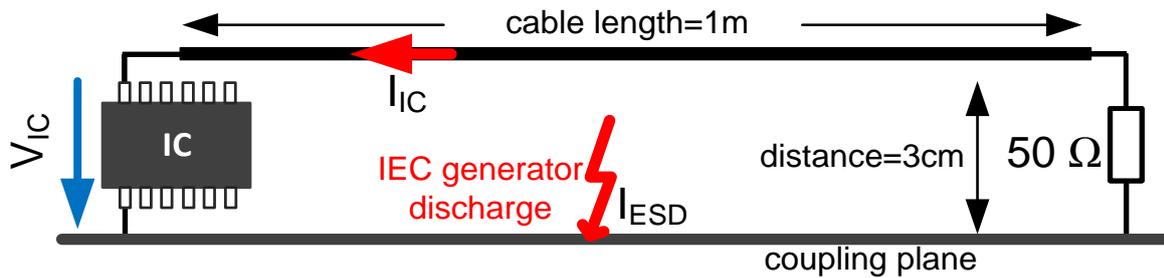


Figure 8.19: Setup with IC models connected to the cable

In the electrical domain of the used IC model as shown in Figure 8.20 the capacitor C_{IC} is a parallel element of the resistive IV-table. Similar to previously shown results voltage and current shapes are simulated for 5 kV charging voltage at the capacitor of the model. Capacitor size is 7,6 pF for μC and 10,5 pF for CANH pin.

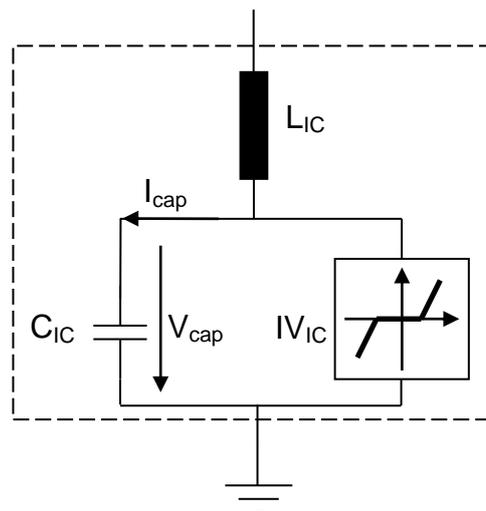


Figure 8.20: Electrical domain of IC model

Waveforms for two configurations with IC model and one with serial RLC circuit are given in Figure 8.21 and Figure 8.22. Considering IC dynamic behavior and IV-curves, shape characteristics are different for all configurations. If an IC model is used clamping effects for maximum amplitudes can be observed. Rise times of the voltage curve obtained with μC IC model are shorter (200 ps) than for 1 k Ω , 5 nH and 10 pF circuit because of dynamic behavior and smaller capacitance. The current shape at IC input is characterized by short positive and negative peaks.

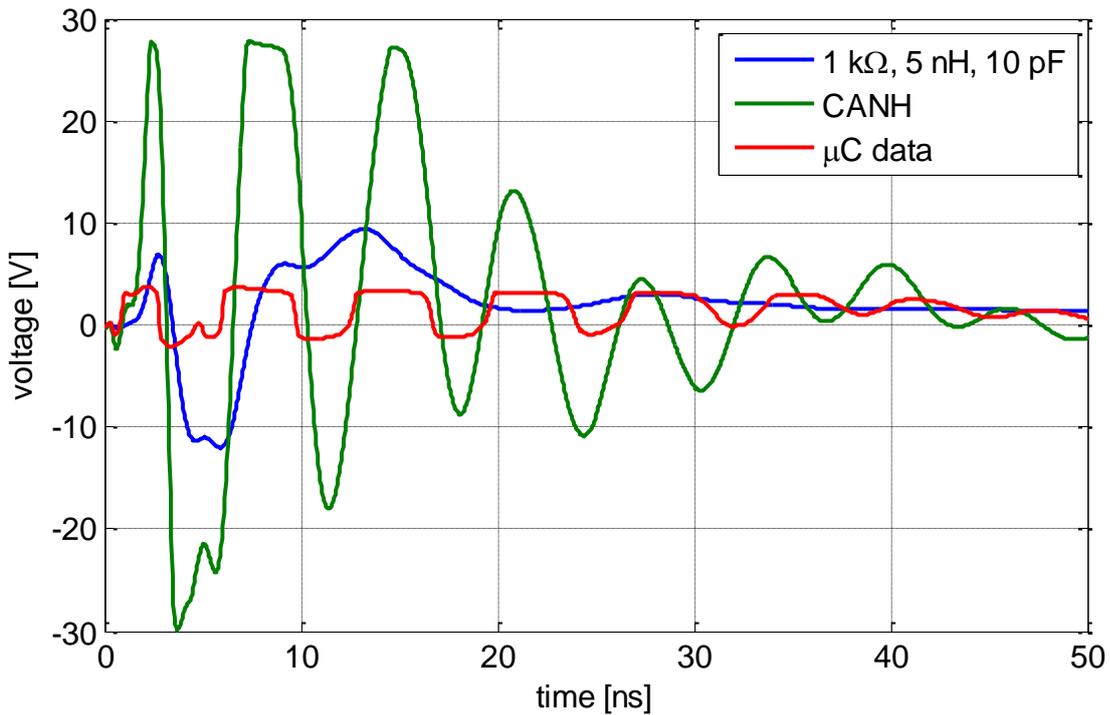


Figure 8.21: Voltage waveform at capacitor for 5 kV charging voltage

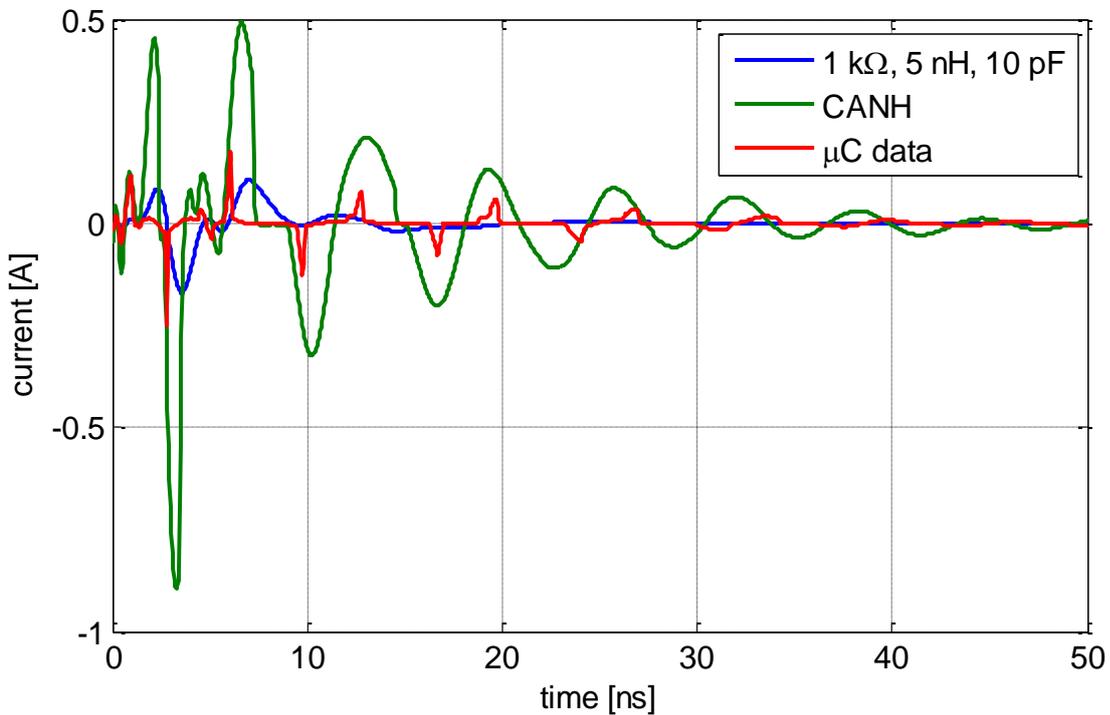


Figure 8.22: Current waveform at capacitor for 5 kV charging voltage

In Figure 8.23 and Figure 8.24 maximum amplitudes of the configurations are compared for different charging voltages. The breakdown voltage of 27 V of the model IV curve is reached at 3 kV charging voltage in case of the CANH pin. Clamping voltage of the μC pin is reached already at 1 kV charging voltage of the

ESD generator. Curves for current amplitudes rise linear with the charging voltage. Highest currents of about 1 A were observed for CANH pin and 5 kV charging voltage.

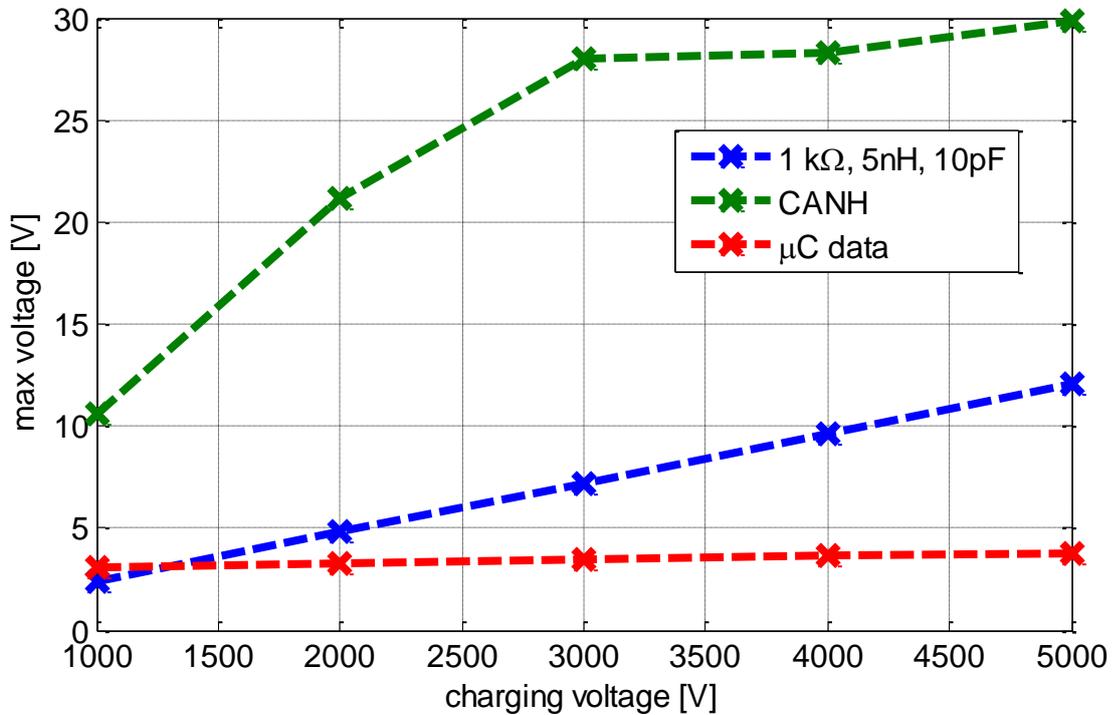


Figure 8.23: Peak voltage at IC capacitor over charging voltage

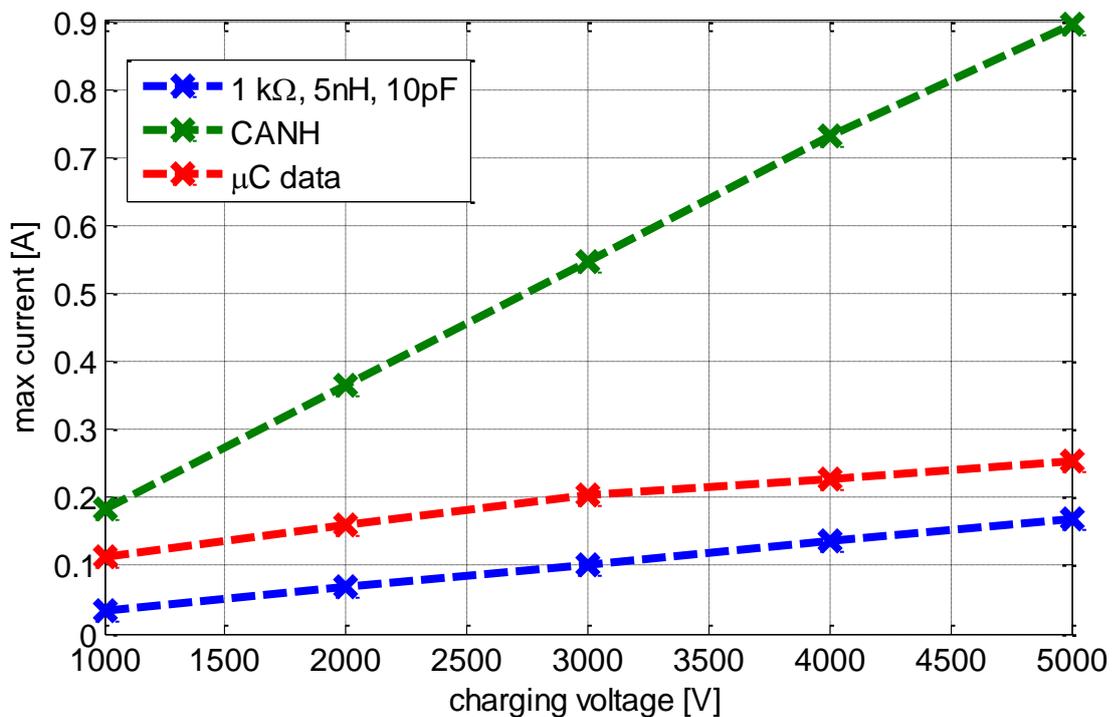


Figure 8.24: Peak current at IC capacitor over charging voltage

8.2.1.4 Conclusion

In the setup an ESD generator discharge into a coupling plane close to a cable was simulated. For estimation of possible disturbance of IC inputs due to ESD field coupling, signals current and voltage waveforms at a 10 pF capacitor were analyzed. Coupled voltages and currents increase with smaller input resistance. Amplitudes increase linear with charging voltage level of the ESD generator. An assumed critical level of 10 V is exceeded for an input resistance of 1 k Ω and 5 kV charging voltage. In a second step different values for serial inductance were simulated. An effect of the inductance could be only observed for small input resistances. Inductors can be useful as ESD protection only in case of low input resistance.

Simulations using IC models are compared to the 1 k Ω , 10 pF, and 5 nH serial circuit. Simulated rise times are shorter using IC models due to different dynamic behavior. Voltage waveforms at the IC capacitor are limited in most cases to breakdown voltage level of IV curves. In case of CANH pin this level is exceeded for charge voltage of 3 kV.

8.3 ESD-Current-Coupling into PCB Structures

In this section the demonstrator PCB is used to build up several measurement setups for estimation of coupling characteristics of IEC generator and TLP testing pulses. First the parameterization of the VHDL-AMS multi conductor transmission line model is verified in frequency domain. In section 8.3.2 signals from IEC generator and TLP discharges are measured for two load conditions. In section 8.3.4 a protection element was connected to a PCB trace (transmission line-TL).

8.3.1 Coupling Between Striplines in Frequency Domain

In section 7.4 the multi conductor transmission line model was verified by comparison to a highly accurate 3D simulation. The parameterization of the model has to be adapted to the structures on the demonstrator PCB. Values for common and differential mode impedances are calculated using theoretical equations for stripline configurations which are implemented in the freeware tool [49]. For the investigations a coupled multi stripline configuration over a ground plane is selected.

8.3.1.1 Setup

The impedances Z_{even} and Z_{odd} can be calculated with TXLINE tool for given geometry values and material parameters. It is assumed that the transmission line parameters are frequency independent. In Figure 8.25 and Figure 8.26 the parameters extracted from the PCB design presented in chapter 6 are used. The relative permittivity ϵ_r was set to 4,55.

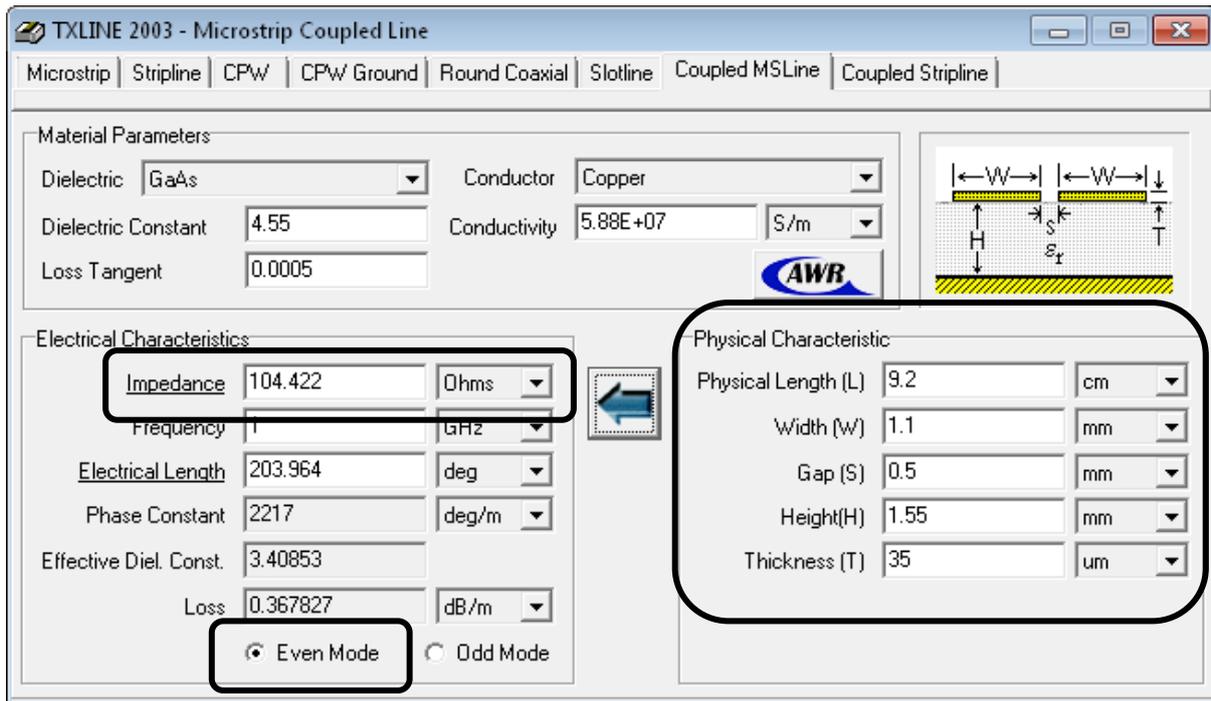


Figure 8.25: Parameter set for VHDL-AMS model in Even Mode

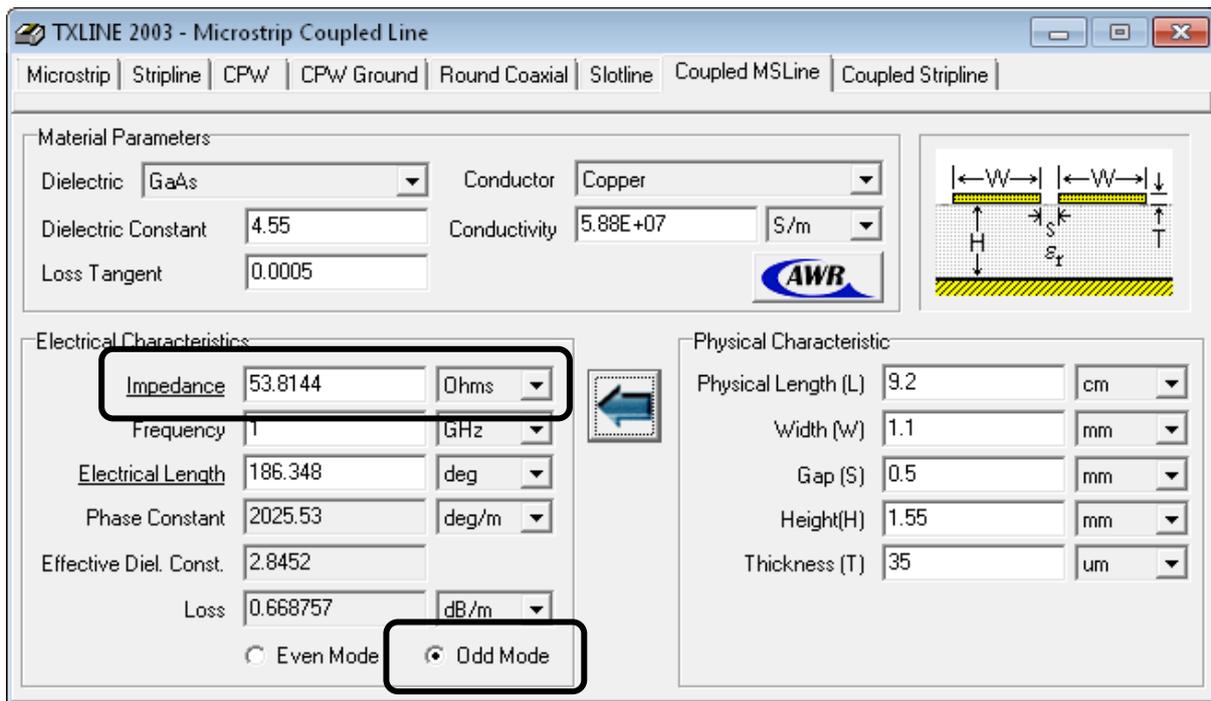


Figure 8.26: Parameter set for VHDL-AMS model in Odd Mode

For verification of the parameter set S-parameters were measured from the crosstalk section on the demonstrator PCB with a network analyzer. A sketch of the measurement setup is shown in Figure 8.27. Both transmission lines are terminated

with 51Ω at nodes N3 and N1 and with the 50Ω source impedance at nodes N2 and N4. The bandwidth was 300 kHz to 1,2 GHz.

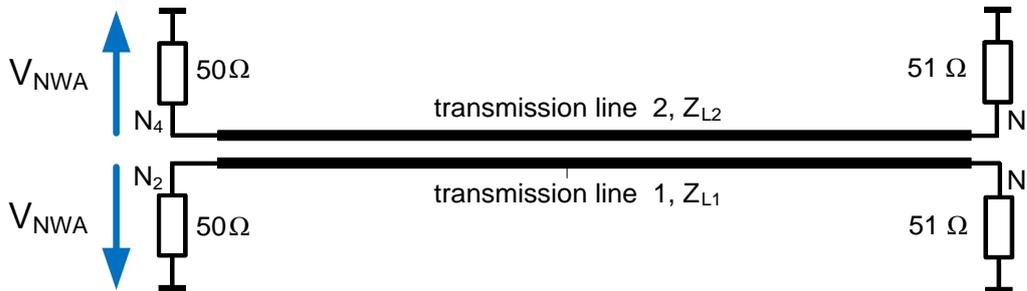


Figure 8.27: Measurement setup with network analyzer

8.3.1.2 Comparison with Simulation and Verification of the Transmission Line Model

The measurement setup was simulated with the calculated impedances. A transmission line length of 9,2 cm was selected. The propagation speed was not adjusted because the influence was negligible.

-- Parameters of MTL

```
constant Zdiff : Real := 2*53.8144; -- Z_diff =2*Z_odd
constant Zcom : Real := 104.422/2.0; -- Z_com =0.5*Z_even
Lossless : ENTITY MTL_common_differential_lossless(lossless)
    generic map (Zdiff => Zdiff, -- differential mode line impedance
                Zcom => Zcom, -- common mode line impedance
                vdiff => 172.9e6, -- diff propagation speed
                vcom => 172.9e6, -- common propagation speed
                length => 0.092) -- line length [m]
```

Simulation and measurement results are compared in Figure 8.28. Resonances of transmission and reflection S-parameters are simulated with good accuracy. Deviations of less than 10 % between the amplitudes are obtained.

The simulation results can be improved if the gap S in the physical parameters is decreased to 0,45 mm. The impedances in the transmission line model are modified to $Z_{\text{odd}} = 52.5059$ and $Z_{\text{even}} = 105.219$. In Figure 8.29 the measured and simulated curves are very similar with maximum deviation of about 3 %. For further investigations the original parameter set will be chosen. The influence of the differences between the parameter sets on simulation results is very low.

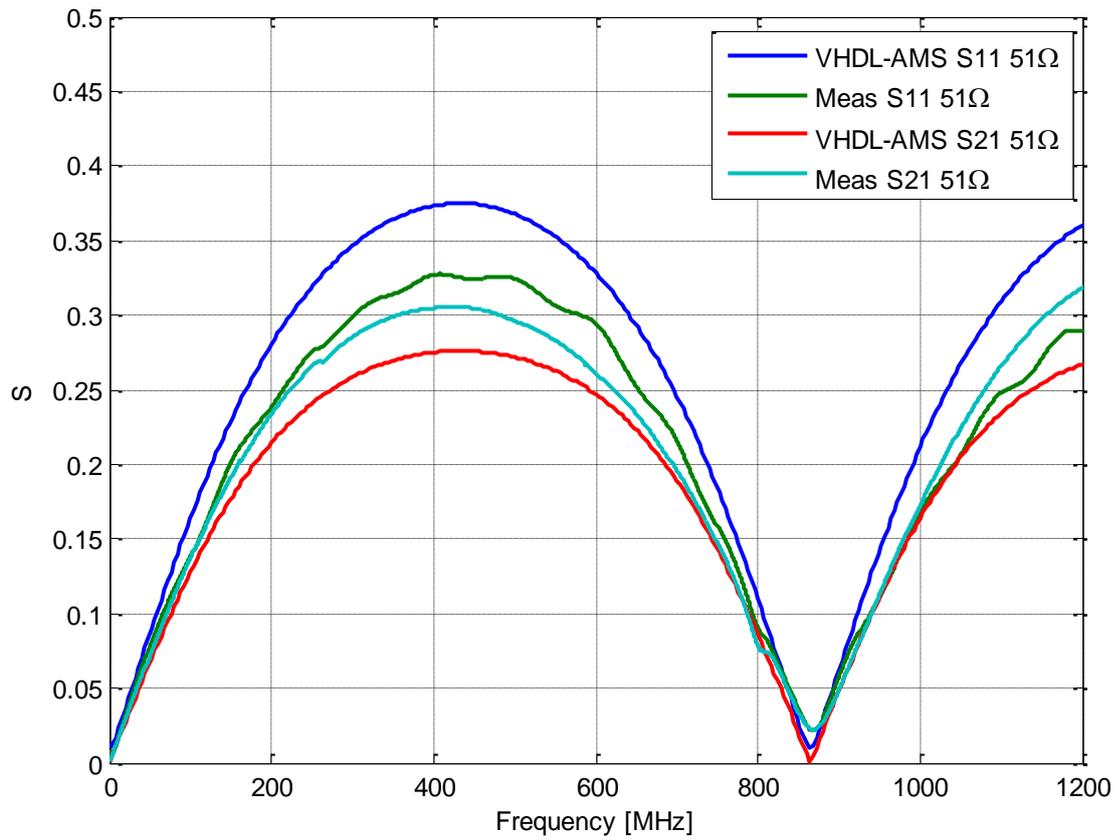


Figure 8.28: Simulation and measurement results with gap = 0,5 mm

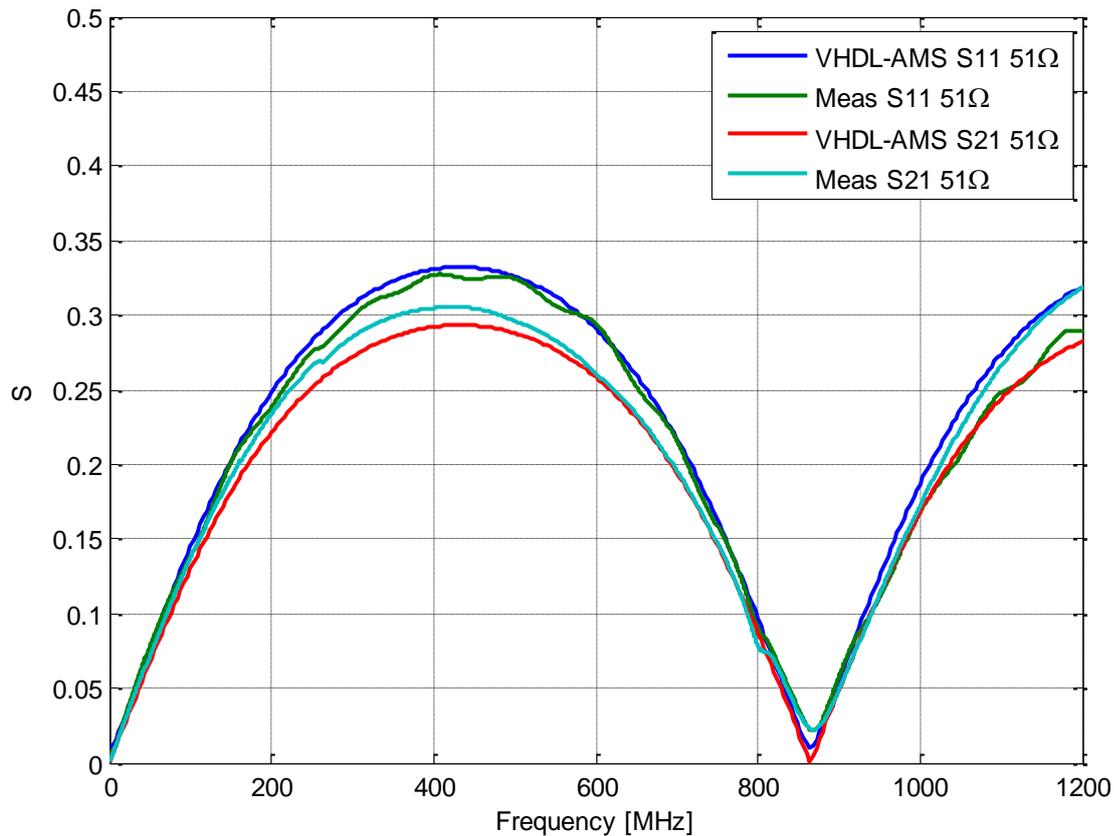


Figure 8.29: Simulation and measurement results with gap = 0,45 mm

8.3.2 Measurement of Cross-Talk Signals in Time Domain

In this section the simulation model of the coupled PCB trace set is verified in time domain. Two pulse generators are discharged into the PCB traces. Two configurations with low and high load resistances of the coupled traces on the cross-talk section on the demonstrator PCB are considered to cover capacitive and inductive coupling effects.

8.3.2.1 IEC ESD Generator

Figure 8.30 shows the measurement setup for the IEC generator. The current through both conductors is measured via Tektronix CT1 sensors and voltages are measured at 50Ω instrument impedance of the oscilloscope. Both traces are terminated on the side of the discharge point with SMD devices to ground. The IEC generator is discharged via a soldering pad close to the SMD device of one transmission line. The charging voltage is set to 1 kV.

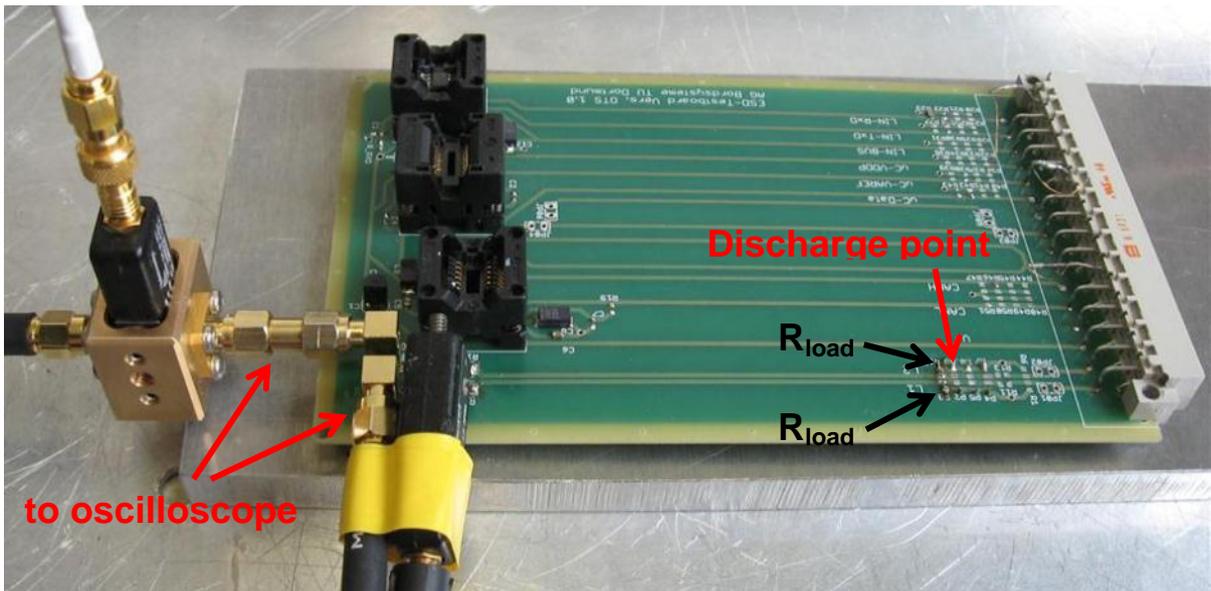


Figure 8.30: Measurement setup with CT1 current sensors for IEC generator discharge

8.3.2.1.1 Measurement and Simulation Results for $R_{load} = 1\text{ k}\Omega$

The measurement and simulation results are presented for $R_{load} = 1\text{ k}\Omega$ at nodes N1 and N3 defined in the sketch in Figure 8.31.

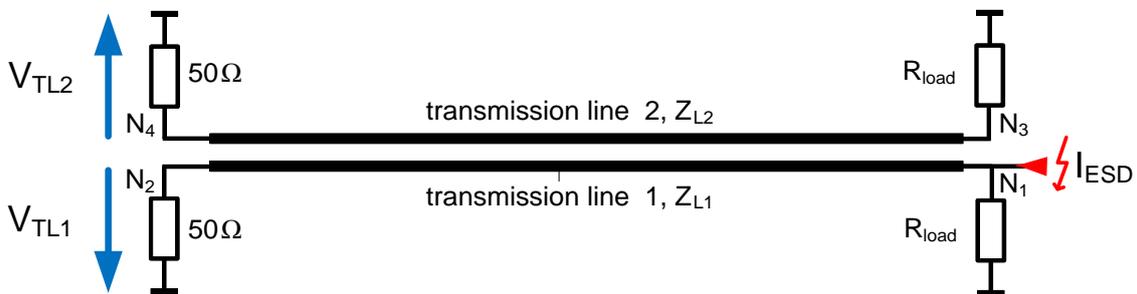


Figure 8.31: Measurement setup for cross-talk test with IEC generator on demonstrator PCB

Results for voltage and current at node N2 are shown in Figure 8.32 and Figure 8.33. The simulated coupled signals at node N4 are compared to the measured shapes in Figure 8.34 and Figure 8.35.

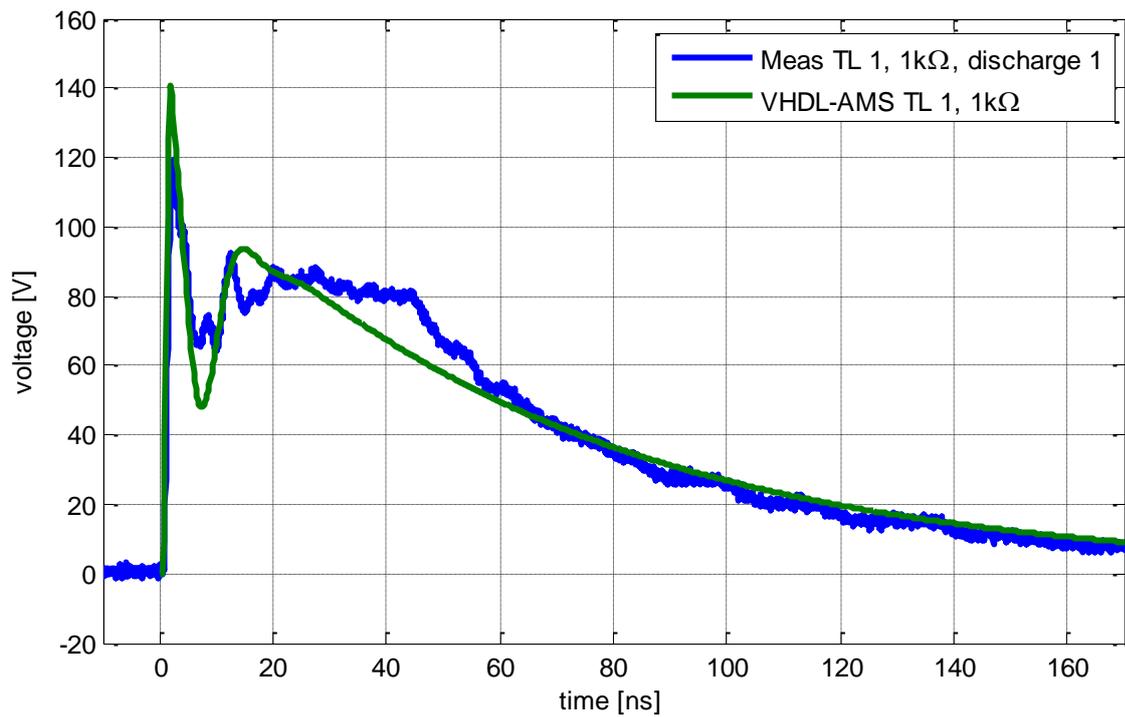


Figure 8.32: Measured and simulated voltage for 1 kV IEC generator discharge on TL1

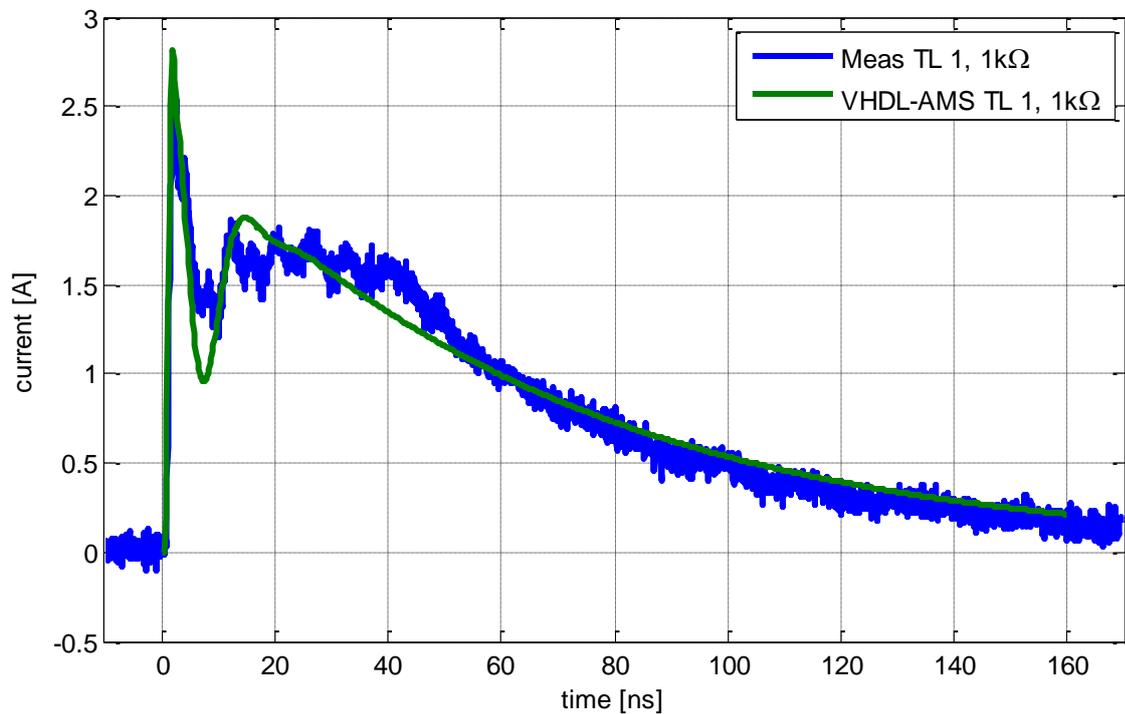


Figure 8.33: Measured and simulated current for 1 kV IEC generator discharge on TL1

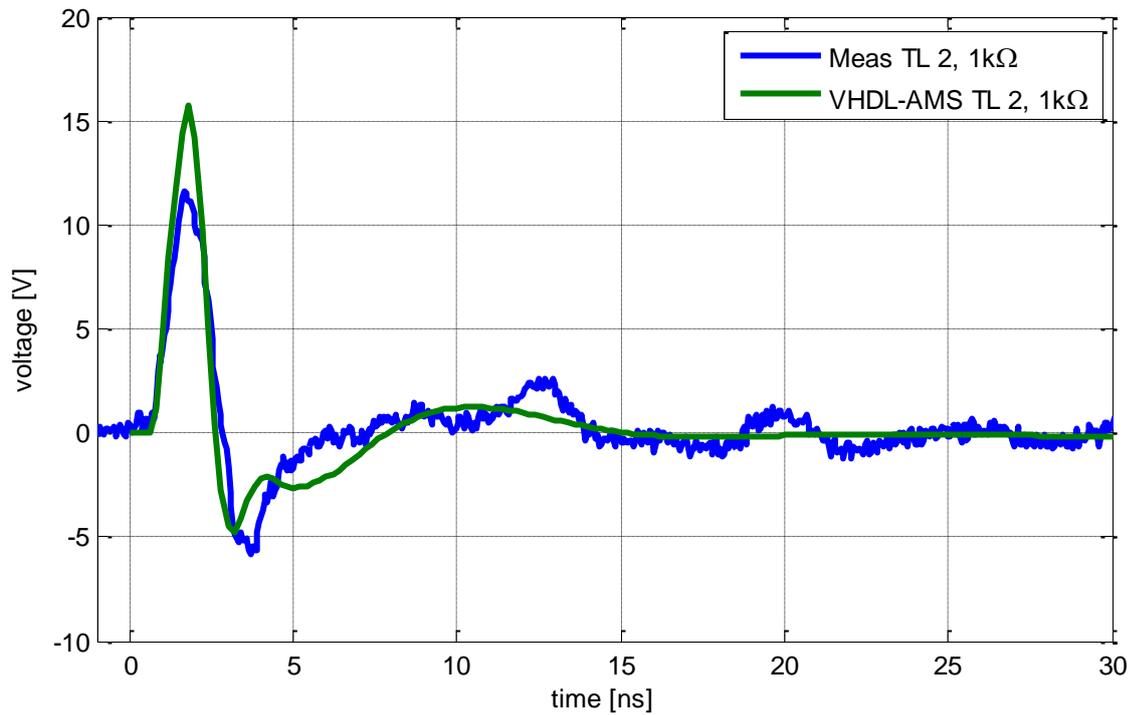


Figure 8.34: Measured and simulated voltage for 1 kV IEC generator discharge on TL2

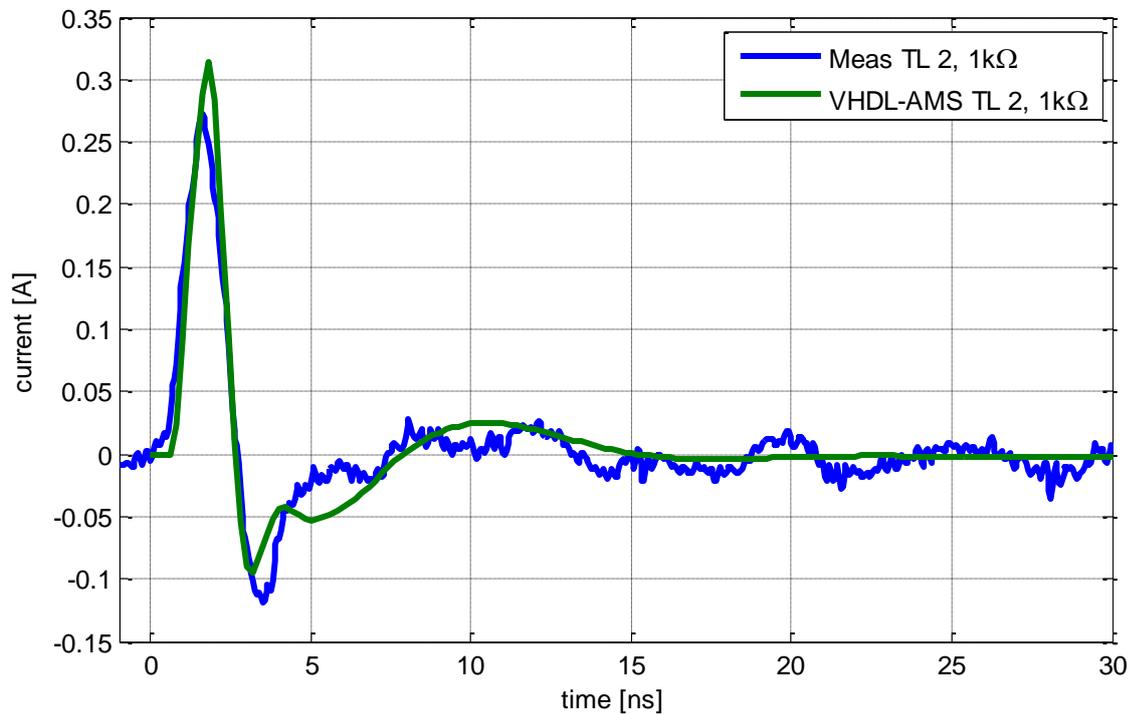


Figure 8.35: Measured and simulated current for 1 kV IEC generator discharge on TL2

All presented curves show a good matching between measurement and simulation. According to Table 8.2 only 2,5 % deviation is obtained if the calculated energies are compared for trace 1. A higher deviation between measurement and simulation was calculated for trace 2 due to noise problems. Absolute deviations are very small.

Concerning the coupling factor only about 5 nJ or about 2000 times less energy was measured on trace 2.

TL	measurement	simulation	deviation
1	8,0 μJ	8,2 μJ	2,5 %
2	3,9 nJ	4,9 nJ	25 %

Table 8.2: Comparison of measured and simulated energies for IEC ESD generator

	Energy N2 - trace 1	Energy N4 - trace 2	Coupling factor (E_{N2}/E_{N4})
Simulation	8.2 μJ	4.9 nJ	1740
Measurement	8.0 μJ	3.9 nJ	2051

Table 8.3: Coupling factors for measured and simulated data

8.3.2.1.2 Measurement and Simulation Results for $R_{load} = 0,47 \Omega$

All transmission lines are terminated with $0,47 \Omega$ SMD devices except from node N1 where the IEC generator is discharged. The coupling current signal on conductor 2 is measured via a CT1 current sensor as shown in Figure 8.36.

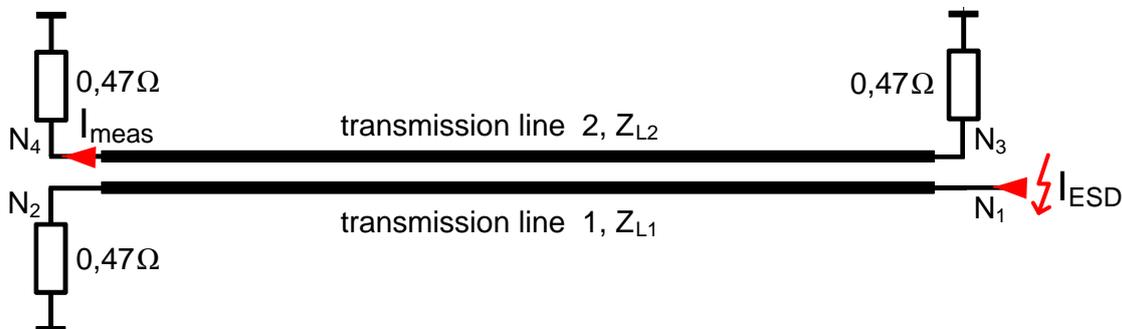


Figure 8.36: Measurement setup for cross-talk test with IEC generator and $R_{load} = 0,47 \Omega$

In comparison to the case $R_{load} = 1 \text{ k}\Omega$ the peak current in Figure 8.37 rises up to about 1,5 A. The simulated and measured current shapes show a good matching.

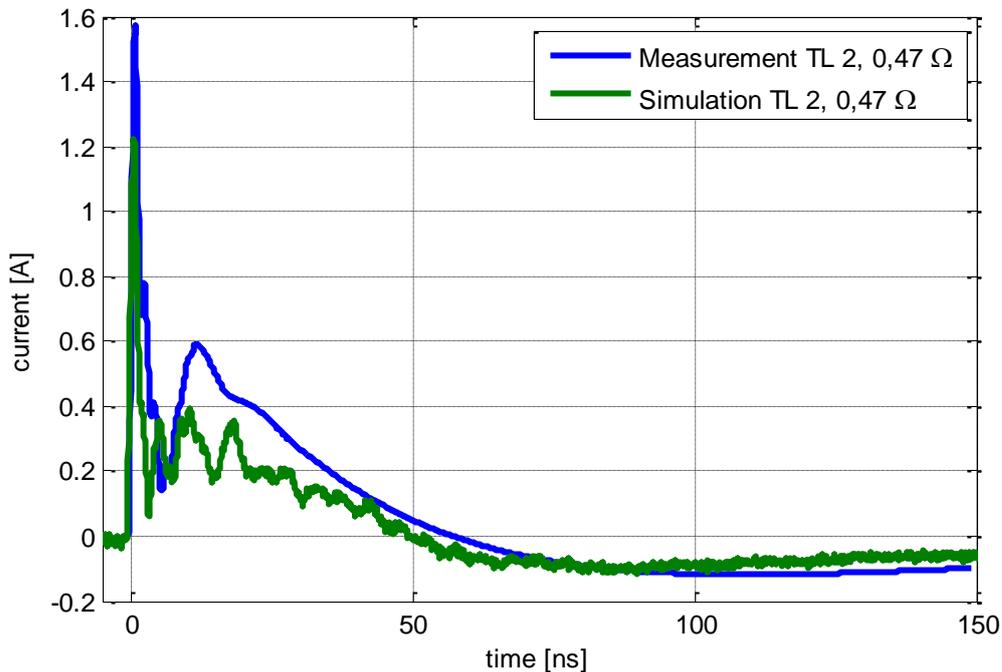


Figure 8.37: Measured and simulated current through transmission line 2 for 0,47 Ω termination

8.3.2.2 TLP

Similar to the investigation with the IEC generator in this section results are shown that were created with a TLP. The charging voltage of the TLP was set to 400 V. Figure 8.38 and Figure 8.39 show a schematic of the setup. The TLP is discharged via trace 1 so that the trace is terminated by 50 Ω impedance of the TLP and by R_{load} . Only the discharge current can be measured. On transmission line 2 voltage and current shapes were measured.



Figure 8.38: Measurement setup for cross-talk test with TLP on demonstrator PCB

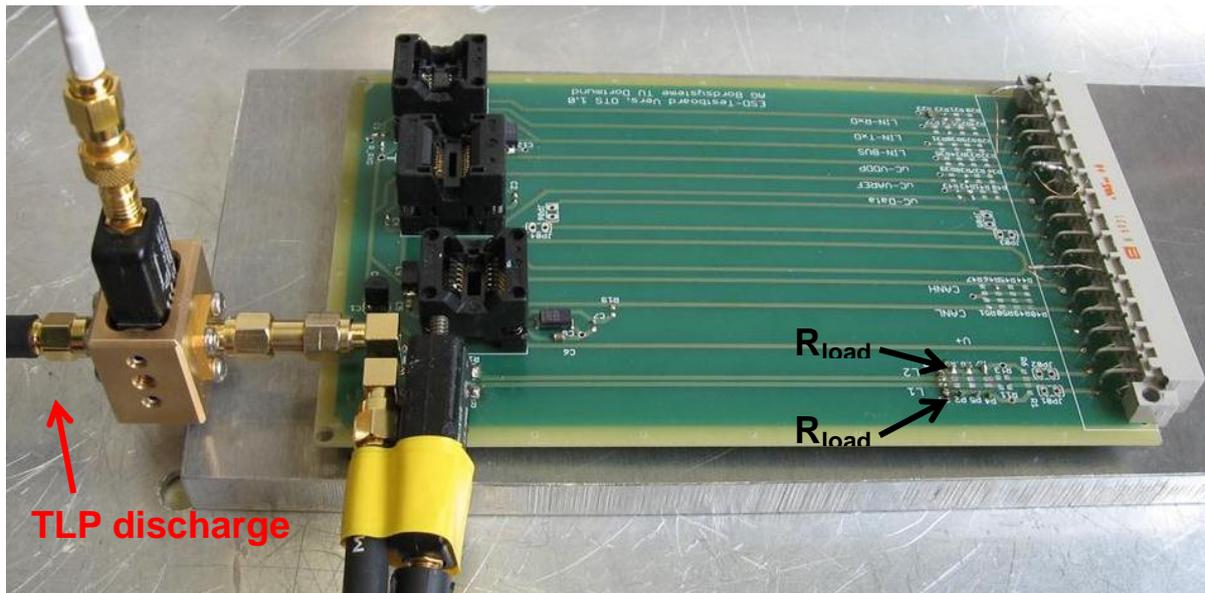


Figure 8.39: Measurement setup with CT1 current sensors for TLP discharge

8.3.2.2.1 Measurement and Simulation Results for $R_{load} = 51 \Omega$

In Figure 8.40 to Figure 8.42 measurement and simulation results are shown for $R_{load} = 51 \Omega$. All measured curves can be reproduced well with simulation. Current amplitude of about 4 A is reached with 50Ω termination and series instrument impedance. On transmission line 2 the maximum amplitude is about 400 mA. The coupling factor of the current is about 10.

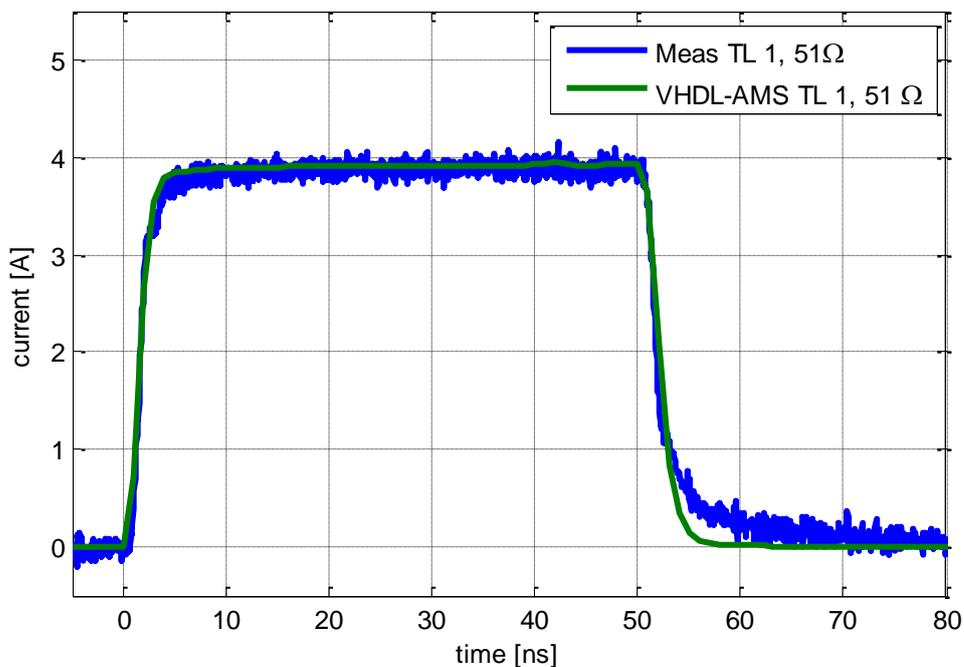


Figure 8.40: Measured and simulated current for 400 V TLP discharge on TL1

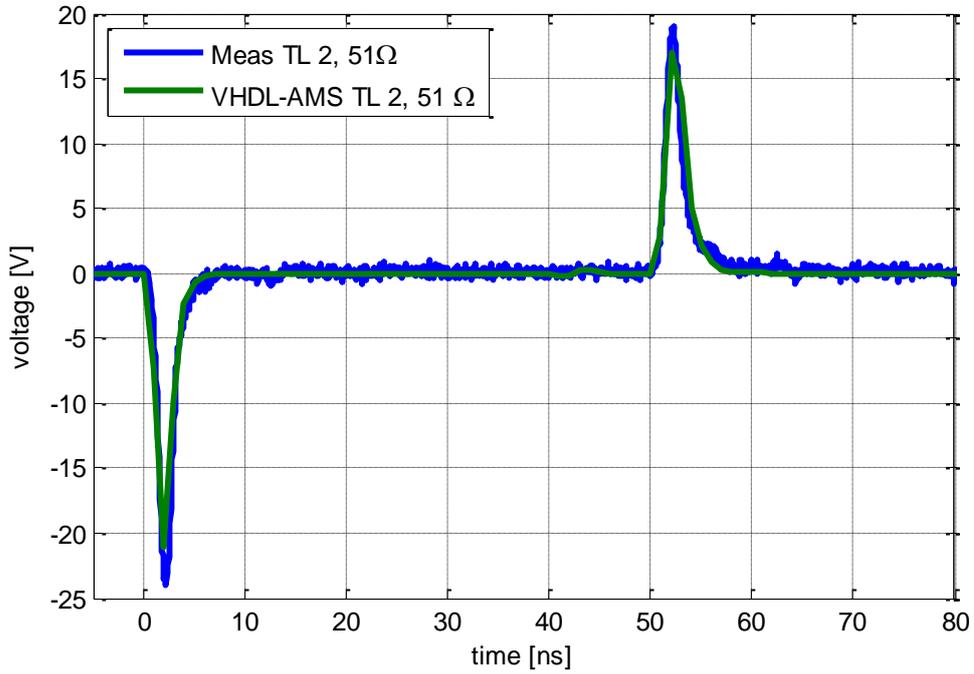


Figure 8.41: Measured and simulated voltage for 400 V TLP discharge on TL2

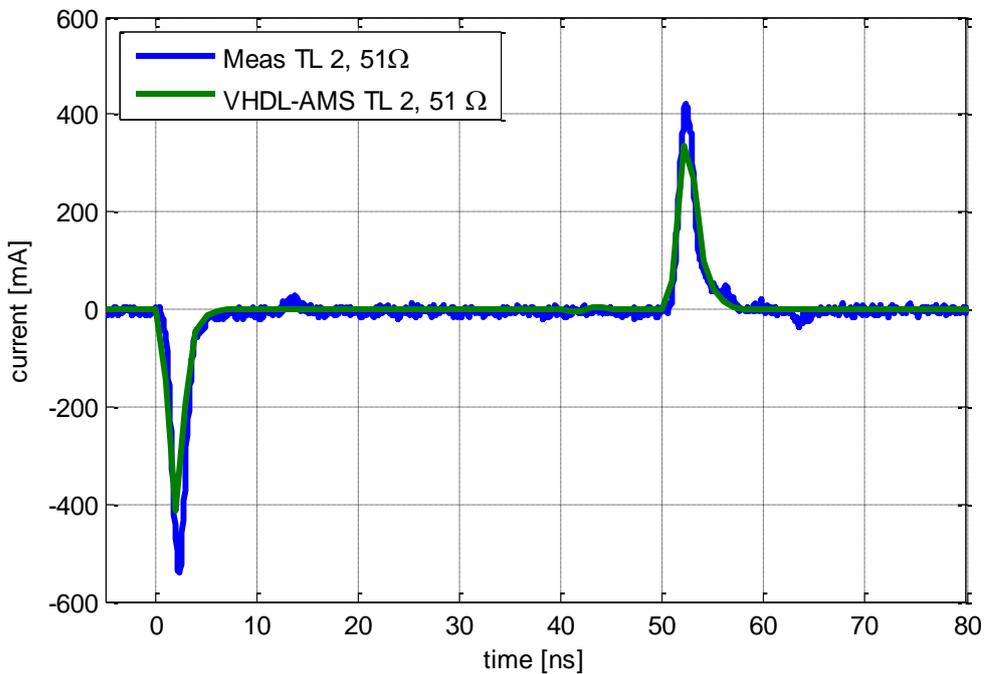


Figure 8.42: Measured and simulated current for 400 V TLP discharge on TL2

The deviation between simulated and measured energies on transmission line 2 is about 14 %, i.e. below the measurement error.

TL	measurement	simulation	deviation
2	25,7 nJ	22,2 nJ	-14 %

Table 8.4: Comparison of measured and simulated energies for TLP

8.3.2.2.2 Measurement and Simulation Results for $R_{load} = 0,47 \Omega$

In this section results are presented for $0,47 \Omega$ terminations. Current amplitudes of about 8 A are obtained on trace 1 for 400 V charging voltage because of low resistance. In Figure 8.44 and Figure 8.45 the measured and simulated currents are compared. Significant deviations of the current amplitudes on trace 2 were simulated. This might be caused by additional inductances in the measurement setup. The simulation is very sensitive for small variations of R_{load} . In Figure 8.46 R_{load} was replaced by 1Ω and 10 nH inductance.

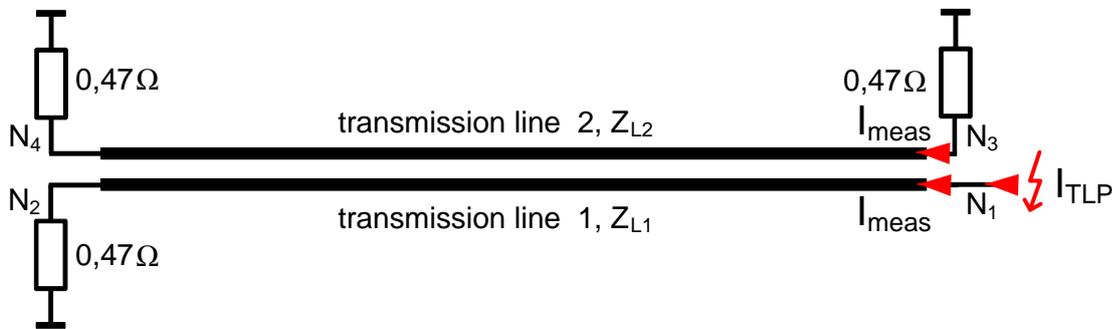


Figure 8.43: Measurement setup for cross-talk test with TLP and $R_{load} = 0,47 \Omega$

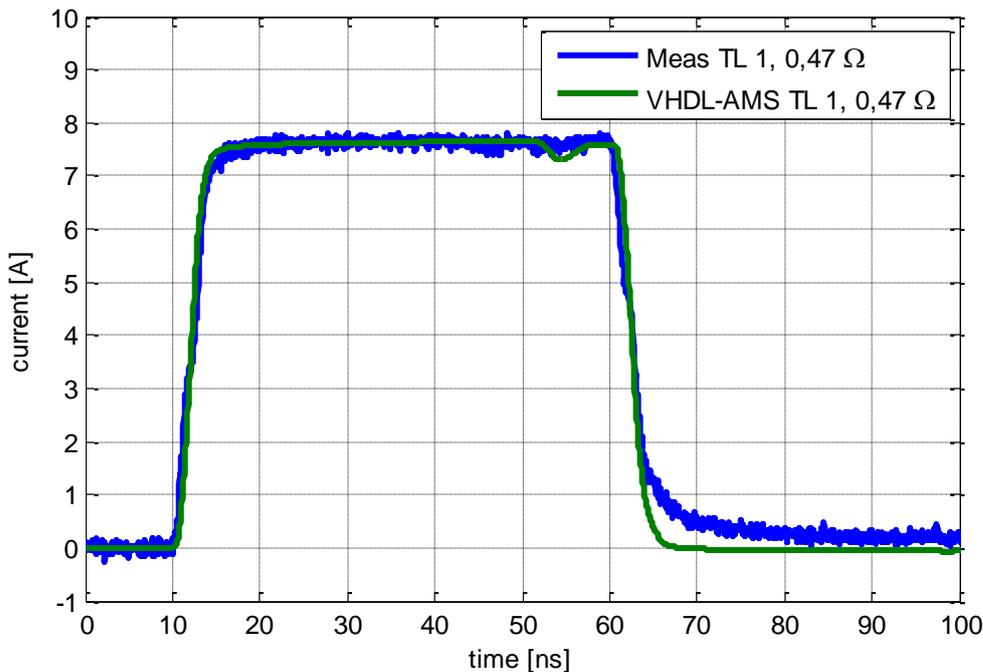


Figure 8.44: Comparison of simulated and measured current on TL1

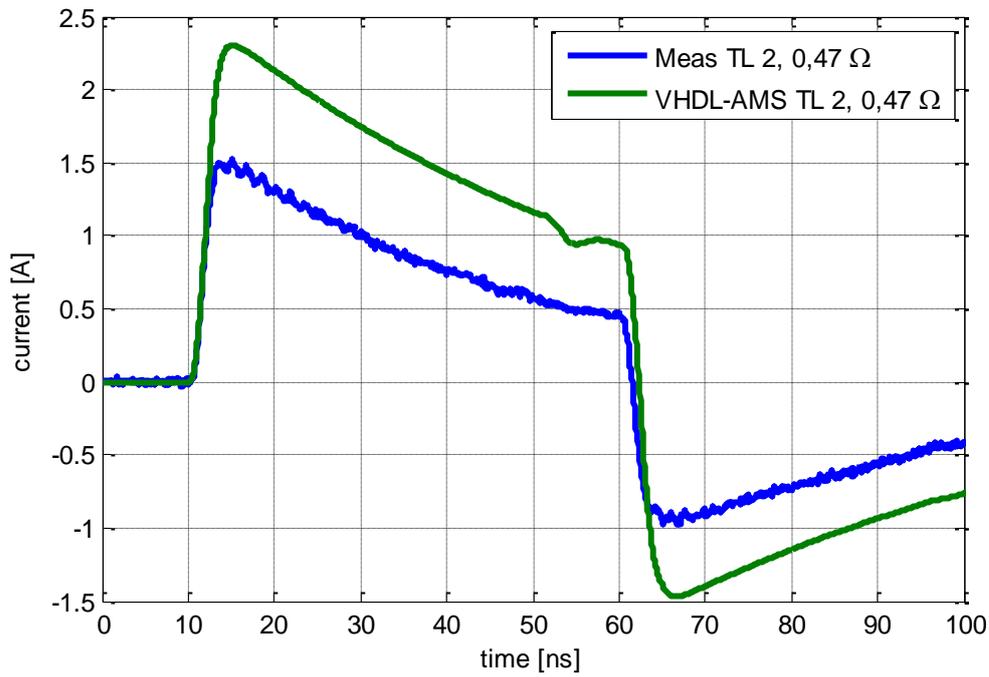


Figure 8.45: Comparison of simulated and measured current on TL2

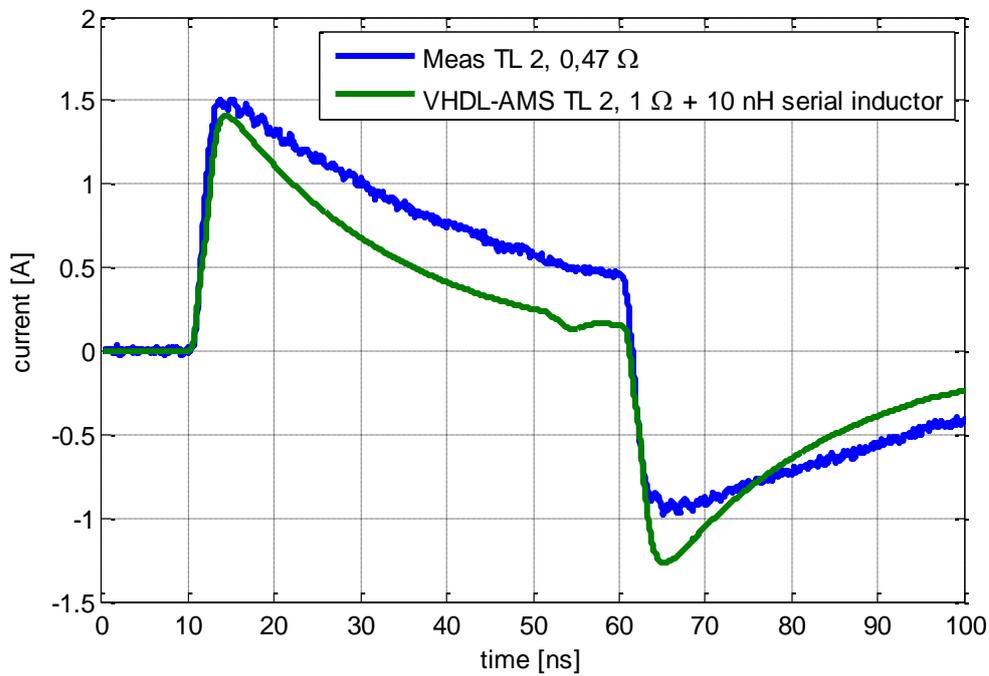


Figure 8.46: Simulated current with additional resistance and inductance

8.3.3 ESD Coupling between PCB Traces Terminated with ICs

A potential threat of ESD coupling between PCB traces is simulated. Current and voltage waveforms of IEC discharges with different charging voltage are analyzed by means of peak amplitude and energy at IC pins.

8.3.3.1 Setup

In the setup shown in Figure 8.47 a configuration is simulated which can be found in automotive electronic systems. An IEC ESD generator is discharged via a PCB trace connected to a global IC pin. A CANH input of the TJA1041T transceiver model was chosen which is connected via 10 cm transmission line to the point of discharge. Both endings of a second parallel victim transmission line are connected to microcontroller IC models representing local pins. Here a XC864 Data pin model was chosen.

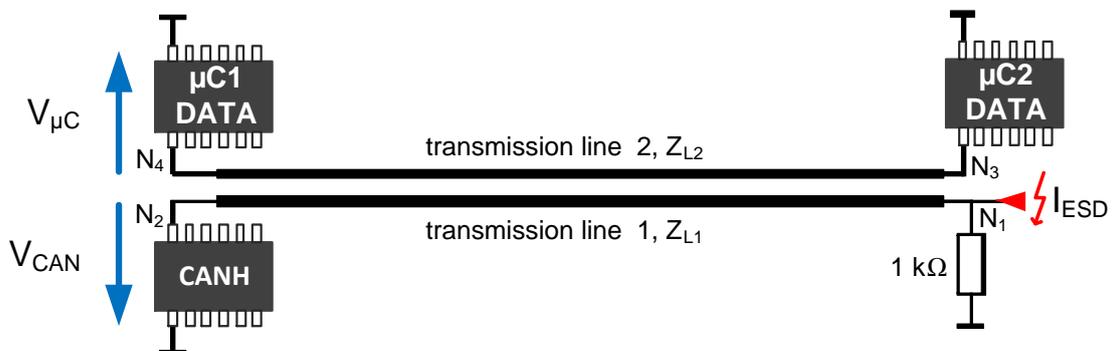


Figure 8.47: Simulation setup with microcontrollers as loads on the victim transmission line

The multi-conductor transmission line model is parameterized according to traces on a selected automotive ECU. Values for common and differential mode impedances are calculated using theoretical equations for stripline configurations which are implemented in a software tool [49]. In Table 8.5 physical and electrical characteristics of the automotive ECU are compared to those of the demonstrator PCB. Coupling between traces is increased by using long trace length of 10 cm.

	Automotive	Demonstrator
Width W	254 μm	1.1 mm
Gap S	254 μm	0.5 mm
Height H	0.5 mm	1.55 mm
Thickness T	35 μm	35 μm
Dielectric constant ϵ_r	4.2	4.55
Length l	100 mm	100 mm
Z_{even}	116.1	104.2
Z_{odd}	68.5	53.8

Table 8.5: Physical and electrical characteristics for automotive and demonstrator PCBs

8.3.3.2 Simulation Results

Simulated waveforms at the CANH pin are show in Figure 8.48 and Figure 8.49.

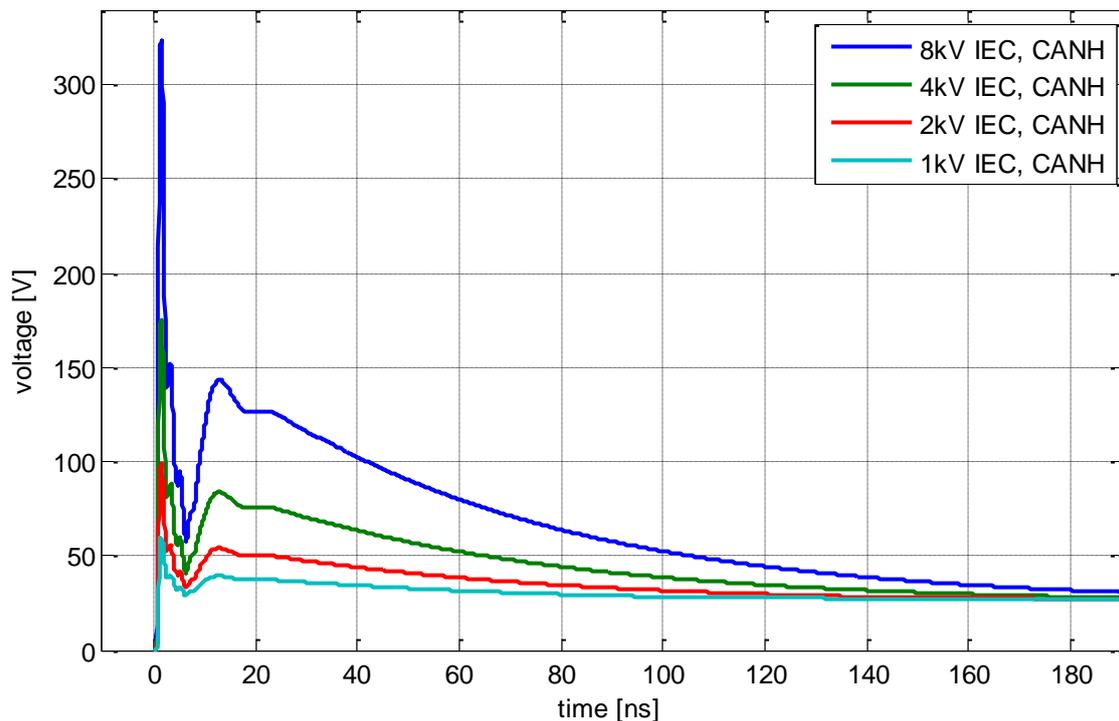


Figure 8.48: Simulated voltage at CANH pin connected to the ESD source line

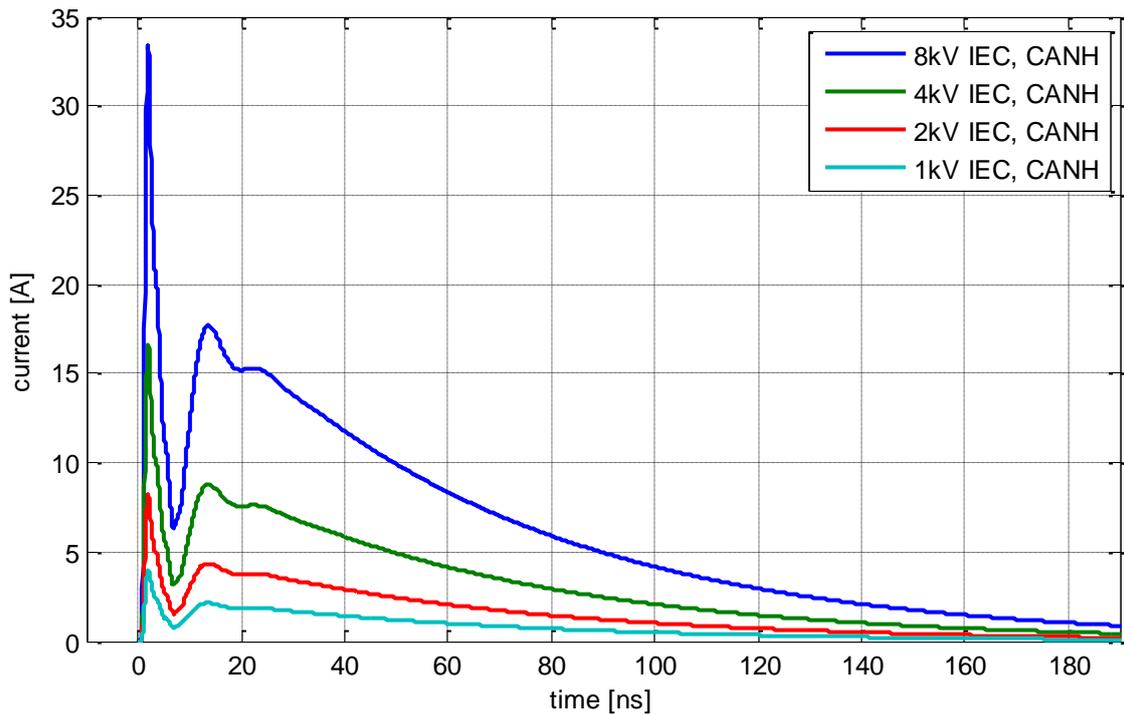


Figure 8.49: Simulated current at CANH pin connected to the ESD source line

Oscillating voltage and current shapes at μ C1 Data pin can be observed. The results are shown in Figure 8.50 and Figure 8.51 with maximal amplitudes of 90 V and about 8 A. The decay time for the 8 kV pulse is about 30 ns.

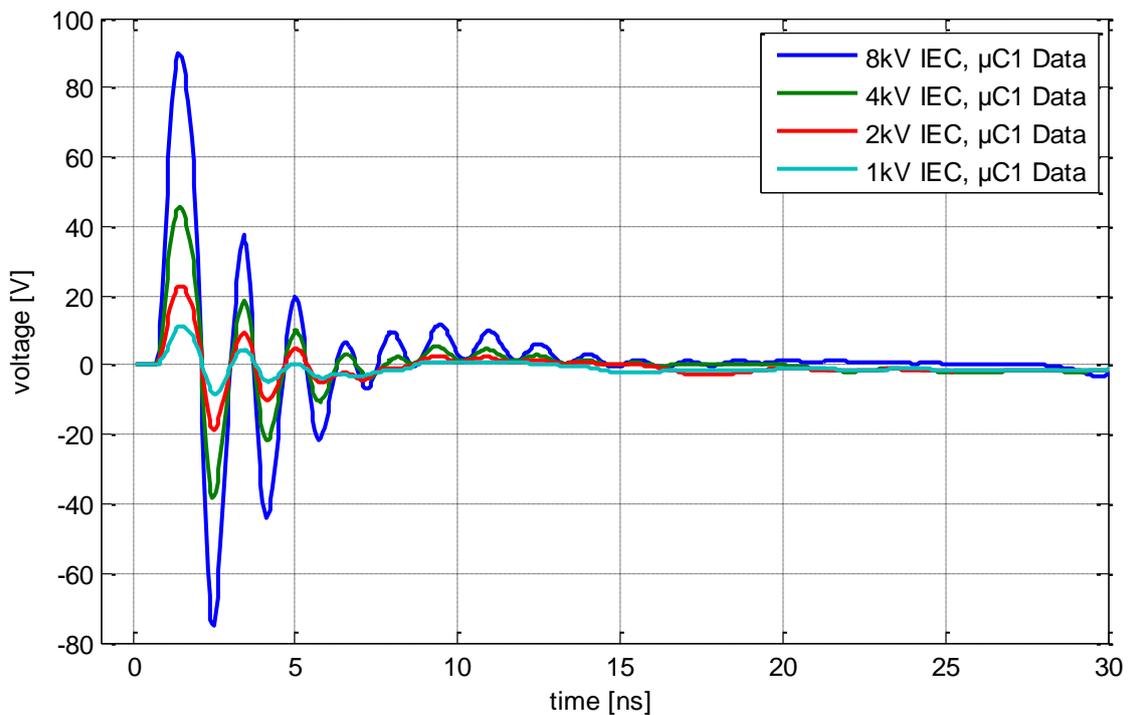


Figure 8.50: Simulated voltage at μ C1 Data pin connected to the ESD victim line

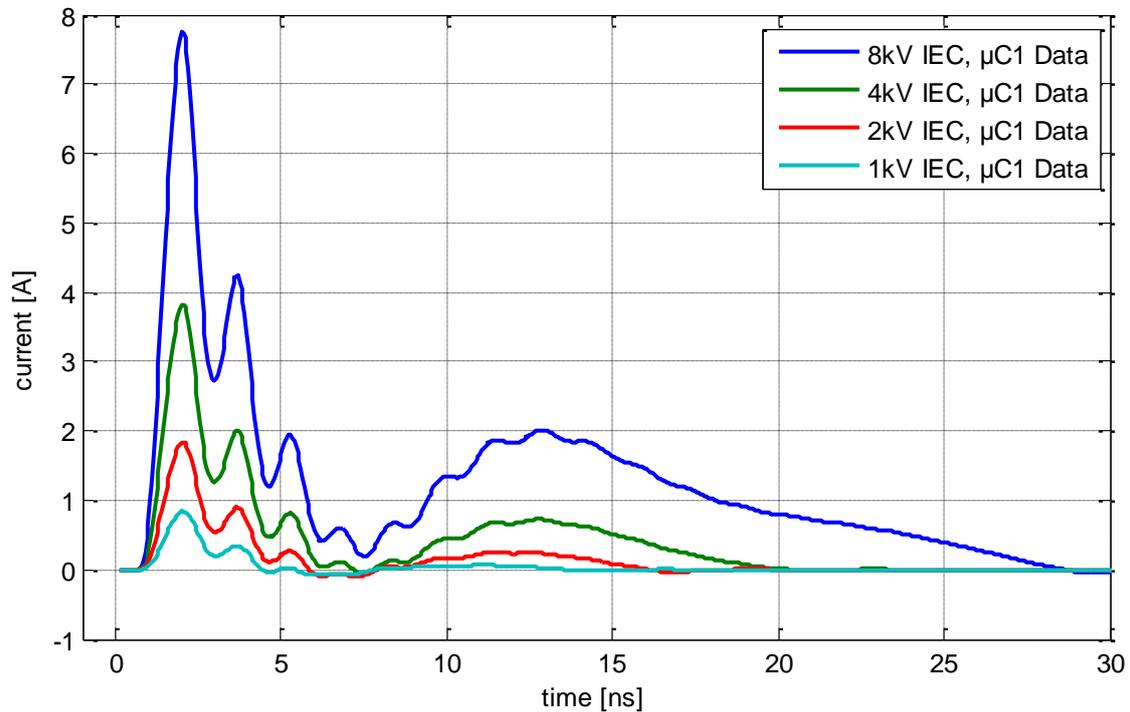


Figure 8.51: Simulated current at μ C1 Data pin connected to the ESD victim line

Simulated values are compared in Table 8.6 and Table 8.7. The maximal voltage and current at the source trace is 323 V and 33 A. A coupling factor can be calculated concerning maximal simulated amplitudes and energies at CANH and μ C1 Data pins. The factor E/E_{1kV} relates the energy to a 1 kV discharge. A factor 24.1 is obtained between the simulated energy for 8 kV IEC discharge at node N2 and 1 kV discharge compared to factor 64 with linear resistive loads. The simulated factor for μ C1 Data pin is 52. The maximum coupling factor for energy from the source line to the victim line is calculated to about 2000. Coupling energies on the victim trace increases relative to the source trace with higher ESD generator charging voltage levels. All simulated values of coupling energy are below the assumed critical level of 350 nJ. No thermal failure of μ C Data pins on the victim trace could be detected for simulated ESD charging voltage level of 8 kV. For a 8 kV discharge on the source line, 90 V and 7.8 A are simulated on the μ C1. For a device with voltage or current based failure mechanism, these measures may be critical.

Similar amplitudes and energy were simulated for a topology where the CANH pin is replaced by a 1 Ω short.

V _{charge} [kV]	V _{max} [V]	I _{max} [A]	E [μJ]	E/E _{1kV}
1	60	4	4.8	1
2	99	8	12.5	2.6
4	175	16	36.5	7.6
8	323	33	115.9	24.1

Table 8.6: Quantities at node N2 CANH

V _{charge} [kV]	V _{max} [V]	I _{max} [A]	E [nJ]	E/E _{1kV}	Energy Coupling Factor E _{CANH} /E _{μC1 Data}
1	10	0.8	2.5	1	1920
2	22	1.8	8.9	3.5	1404
4	45	3.8	31	12.4	1177
8	90	7.8	130	52	892

Table 8.7: Quantities at node N4 μC1 Data

In Figure 8.52 and Figure 8.53 simulated shapes at μC1 Data pin are compared for the automotive PCB and the demonstrator PCB. Improved coupling properties between traces were observed for trace parameters used for the demonstrator PCB. Simulated energy increases of about 33% compared to the topology with smaller trace width and distance to the ground plane. All simulated amplitudes are compared in Table 8.8.

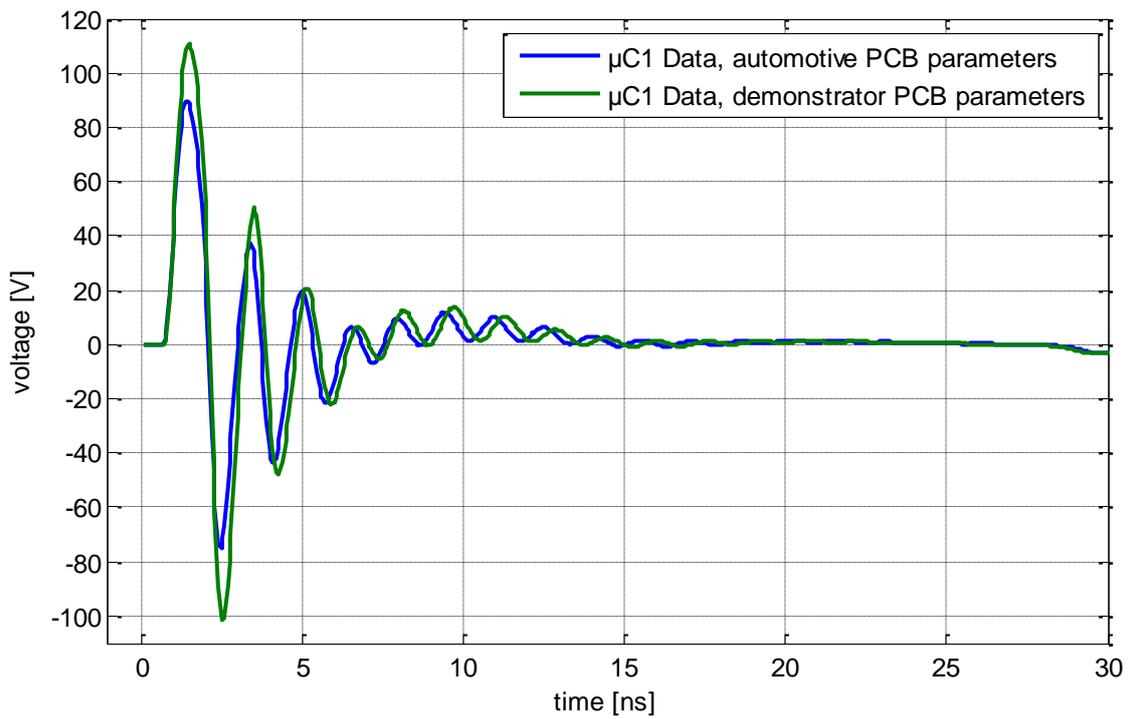


Figure 8.52: Voltage shapes at μC1 Data for different PCB parameters

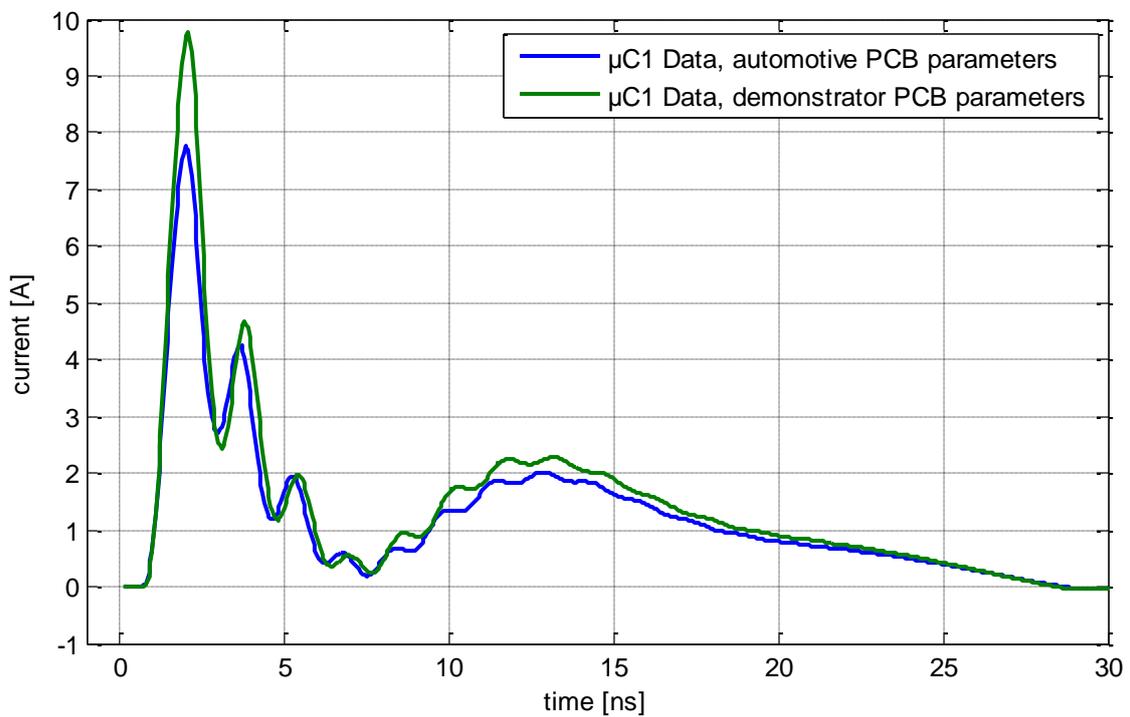


Figure 8.53: Current shapes at μC1 Data for different PCB parameters

PCB parameters	V _{charge} [kV]	V _{max} [V]	I _{max} [A]	E [nJ]
Automotive	8	92	7.7	130
Demonstrator	8	111	9.7	173

Table 8.8: Quantities at μ C1 Data for different PCB parameters

8.3.4 Impact of Protection Elements on Currents

In this section simulation of coupling signals with selected models of ESD protection elements is compared to measurement.

8.3.4.1 Setup

Current and voltage shapes on both transmission lines were measured in the cross-talk section of the demonstrator PCB. In the setup shown in Figure 8.54 the protection element (PE) is connected parallel to an 1 k Ω resistor at transmission line 2. The IEC ESD generator is discharged at node N1 via conductor 1. For observation, if the breakdown voltage of the protection devices is exceeded, voltage and current are measured with an oscilloscope at trace 2 at node N4 for 1 kV and 8 kV charging voltage.

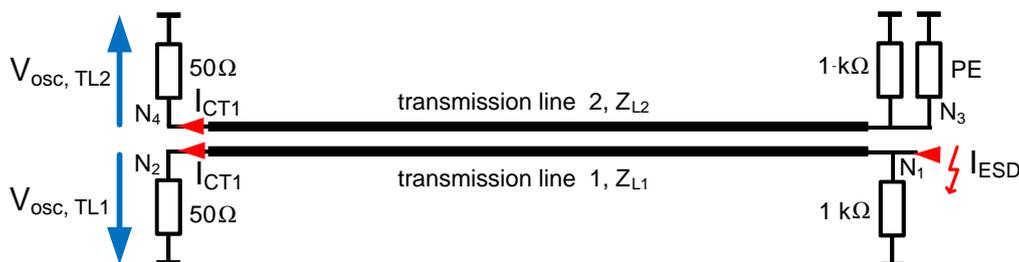


Figure 8.54: Setup for measurement of coupling signals with ESD protection elements

8.3.4.2 Measurement Results

A 10 nF capacitor, Protek TVS GBLCS05C diode and the EPCOS CT0603K14G varistor were selected as ESD protection elements for investigation.

8.3.4.2.1 10 nF Capacitor

In Figure 8.55 and Figure 8.56 the measured and simulated curves for 1 kV charging voltage are compared. The voltage amplitude exceeds 20 V. If the charging voltage of the IEC generator is set to 8 kV nearly 200 V and 4 A peaks can be measured. All curves show a good matching.

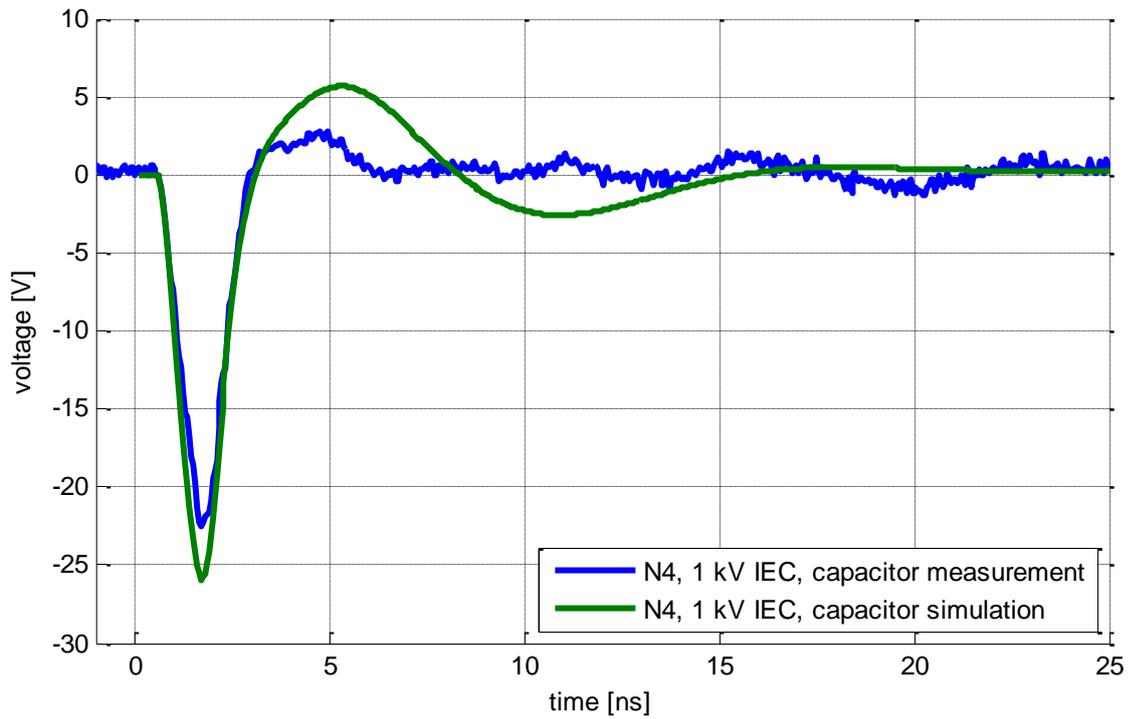


Figure 8.55: Voltage at node N4 with 10 nF capacitor on TL2 for 1 kV discharge on TL1

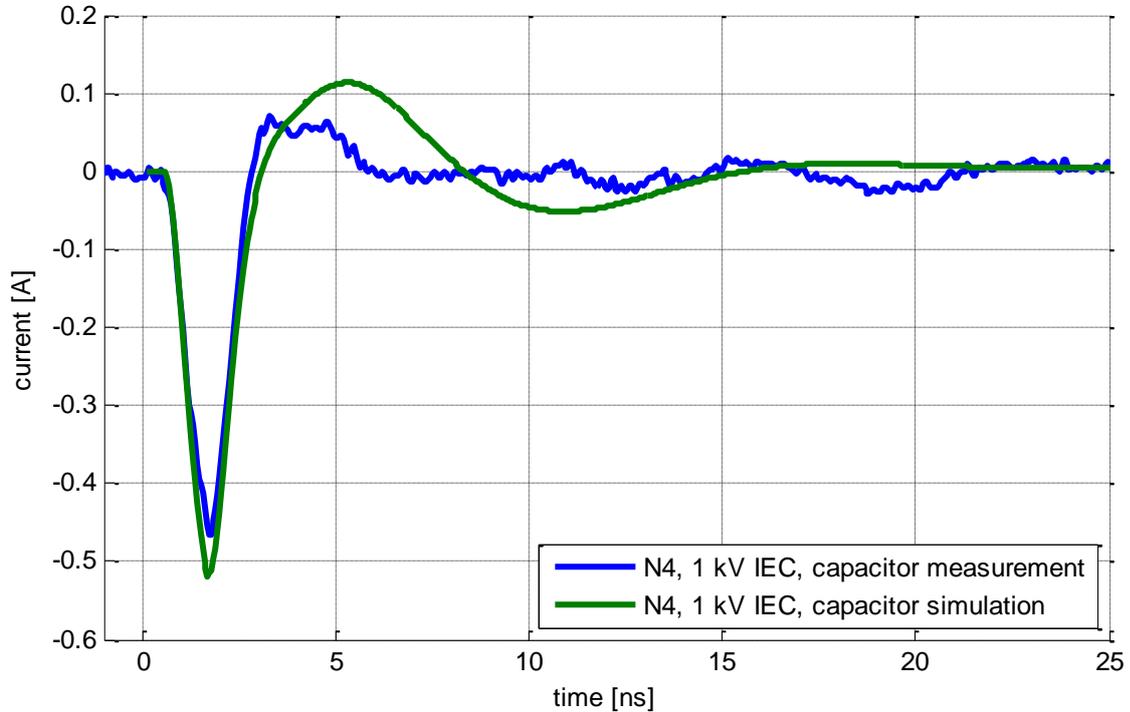


Figure 8.56: Current through node N4 with 10 nF capacitor on TL2 for 1 kV discharge on TL1

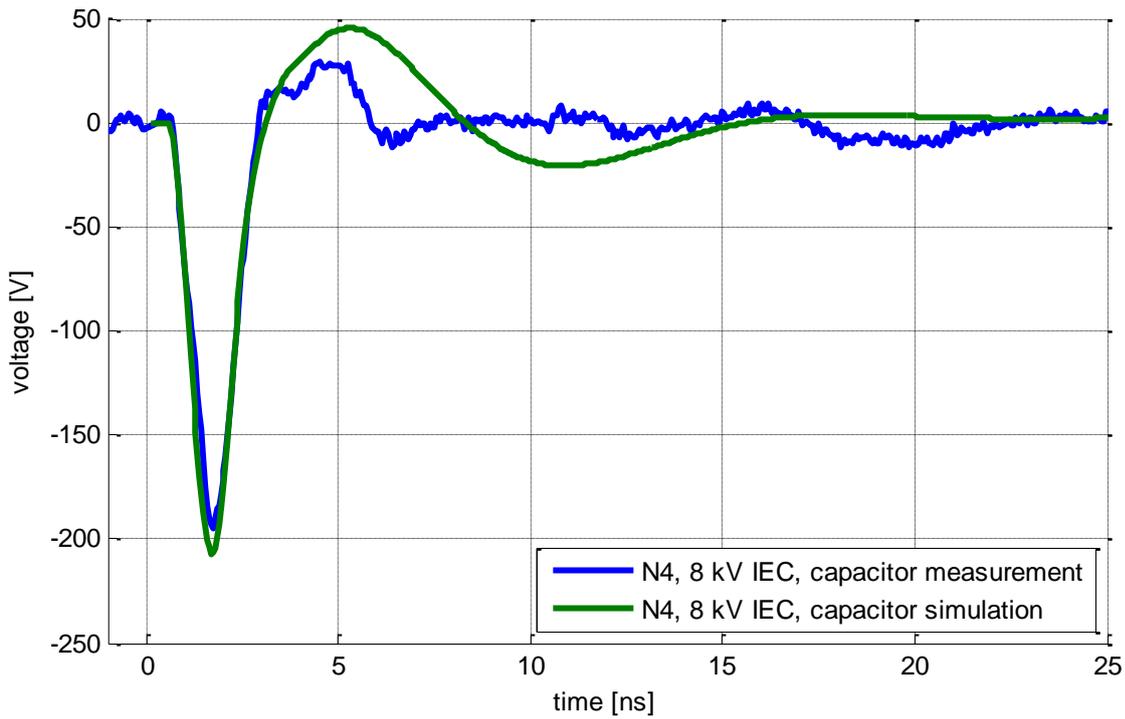


Figure 8.57: Voltage at node N4 with 10 nF capacitor on TL2 for 8 kV discharge on TL1

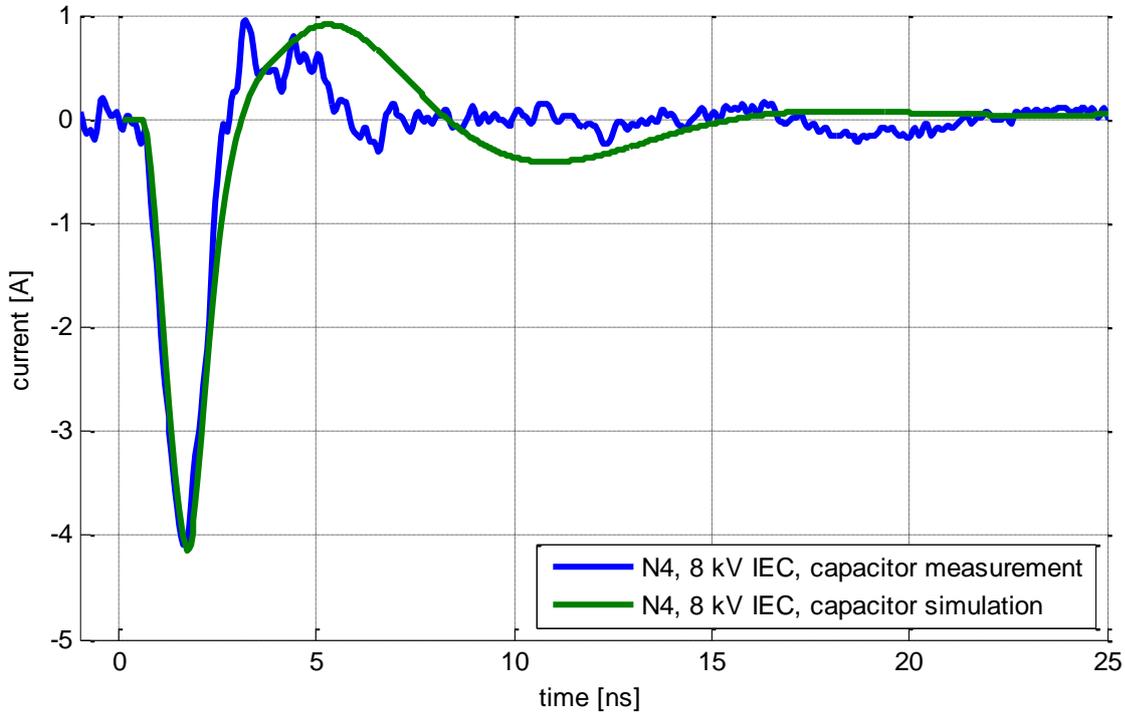


Figure 8.58: Current through node N4 with 10 nF capacitor on TL2 for 8 kV discharge on TL1

8.3.4.2.2 Diode Protek TVS GBLCS05C

Similar pulse shapes are obtained if a TVS diode is connected parallel to trace 2. Data for 1 kV and 8 kV charging voltage are compared in Figure 8.59 to Figure 8.62. Because of the IV characteristic and lower capacitance of the device the peak amplitudes are lower compared to the 10 nF capacitor. The rise time of the peak amplitudes is similar to the first peak of the IEC generator.

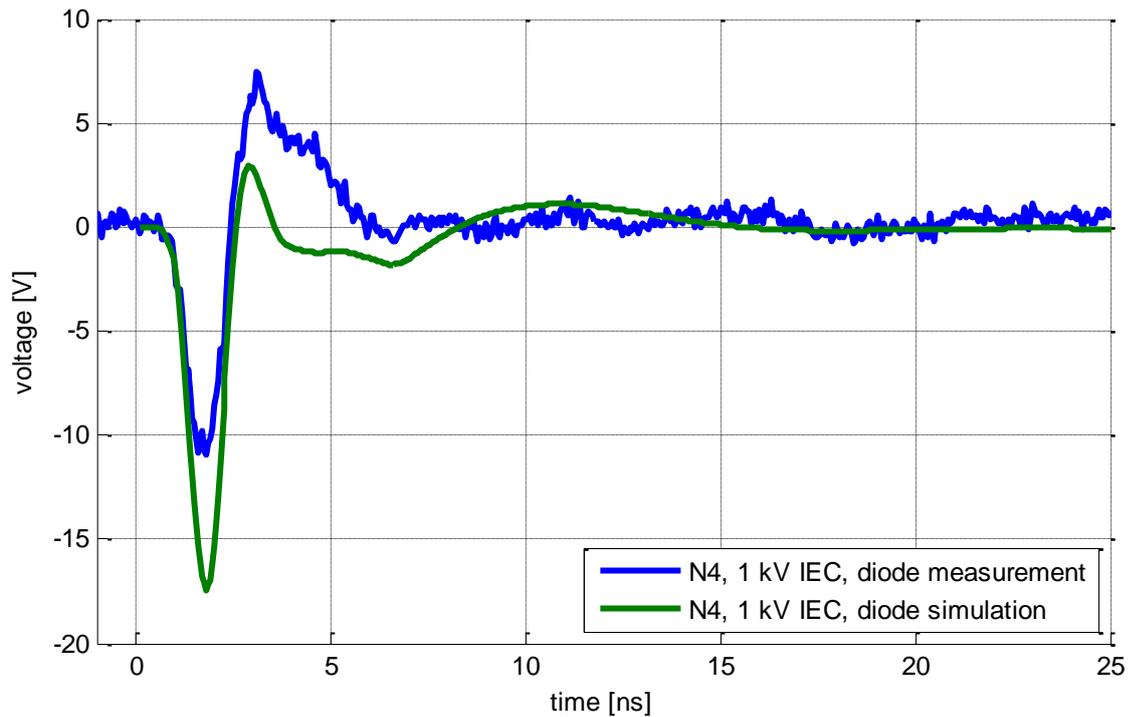


Figure 8.59: Voltage at node N4 with Protek TVS diode on TL2 for 1 kV discharge on TL1

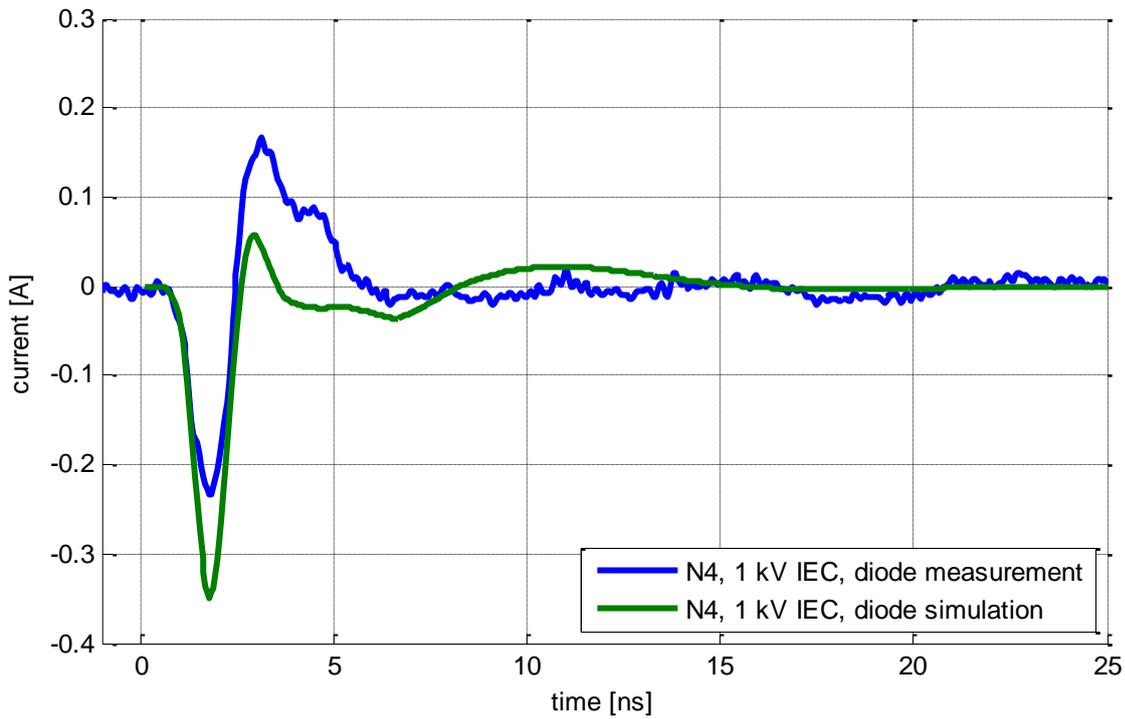


Figure 8.60: Current through node N4 with Protek TVS diode on TL2 for 1 kV discharge on TL1

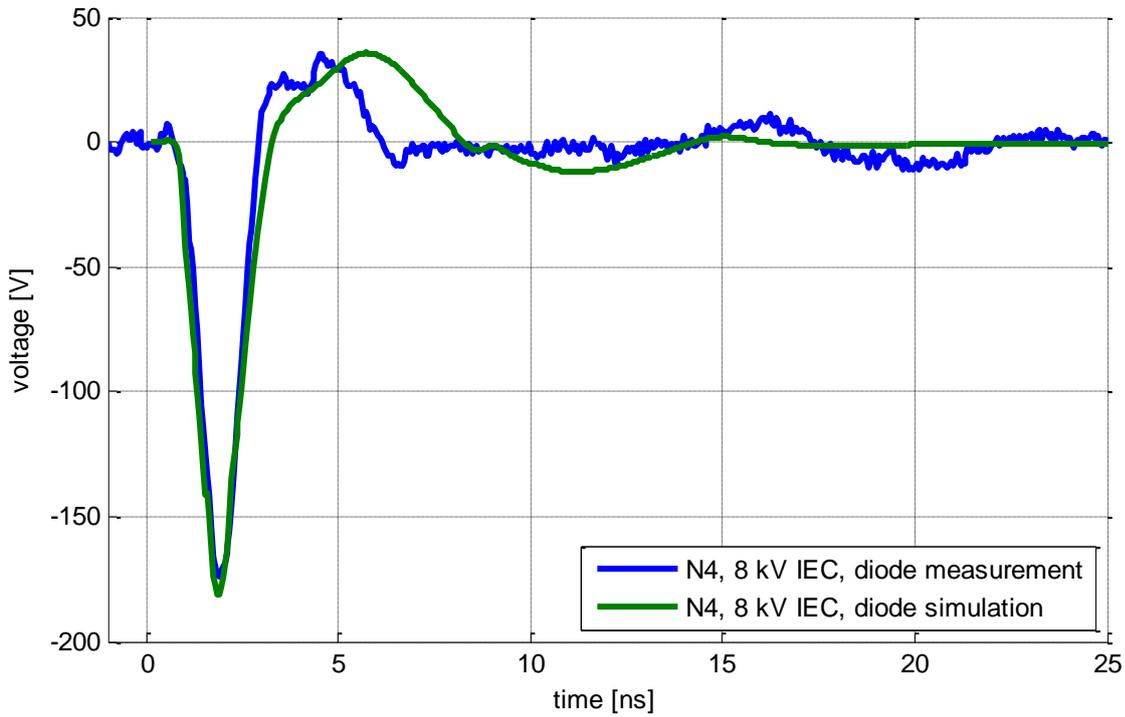


Figure 8.61: Voltage at node N4 with Protek TVS diode on TL2 for 8 kV discharge on TL1

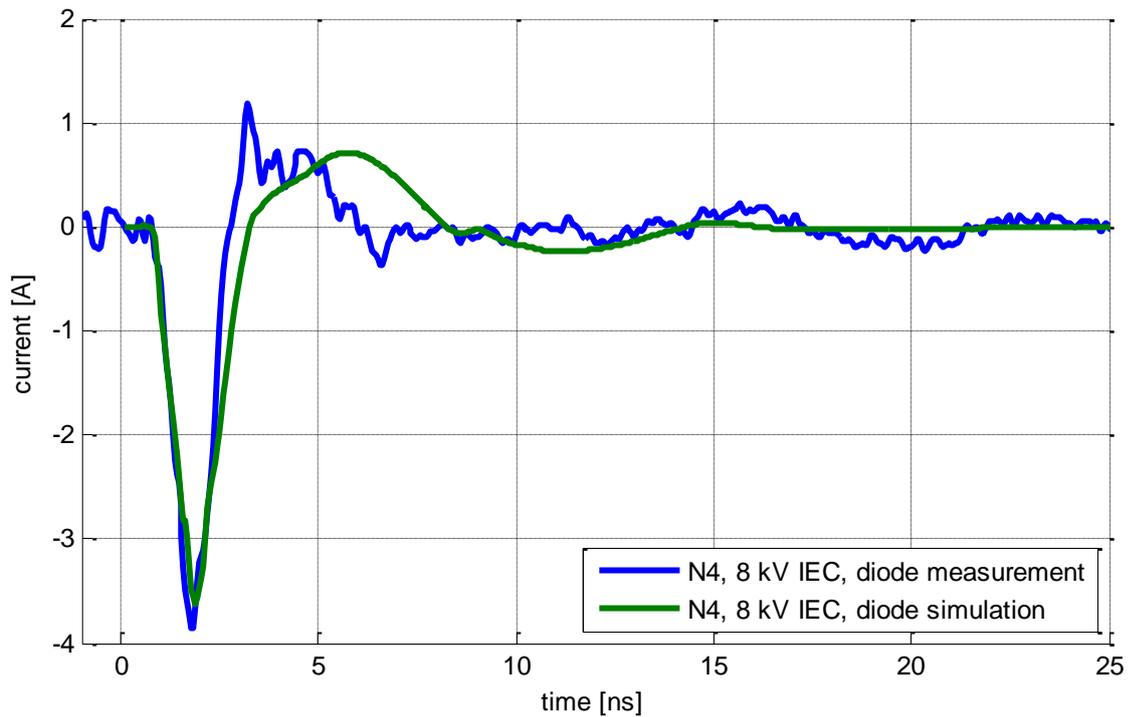


Figure 8.62: Current at node N4 with Protek TVS diode on TL2 for 8 kV discharge on TL1

8.3.4.2.3 Varistor EPCOS CT0603K14G

Good simulation results are obtained for the varistor. The peak amplitudes in Figure 8.63 to Figure 8.66 match well with measured data. Similar pulse shapes were observed with the diode.

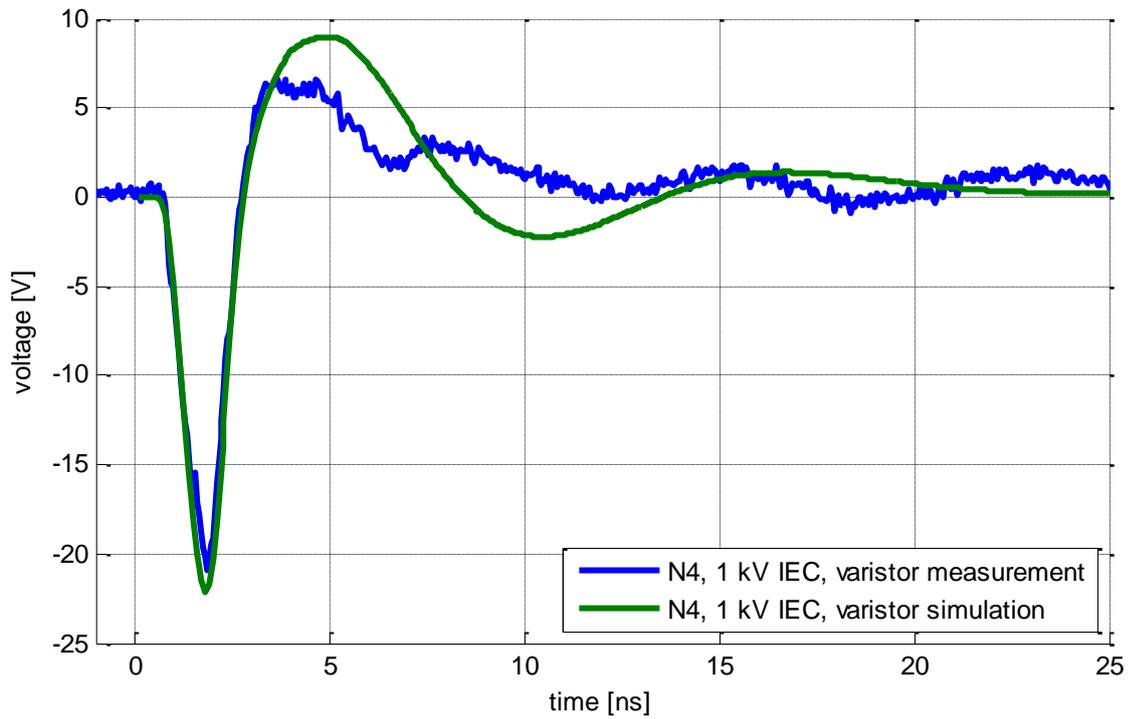


Figure 8.63: Voltage at node N4 with EPCOS varistor on TL2 for 1 kV discharge on TL1

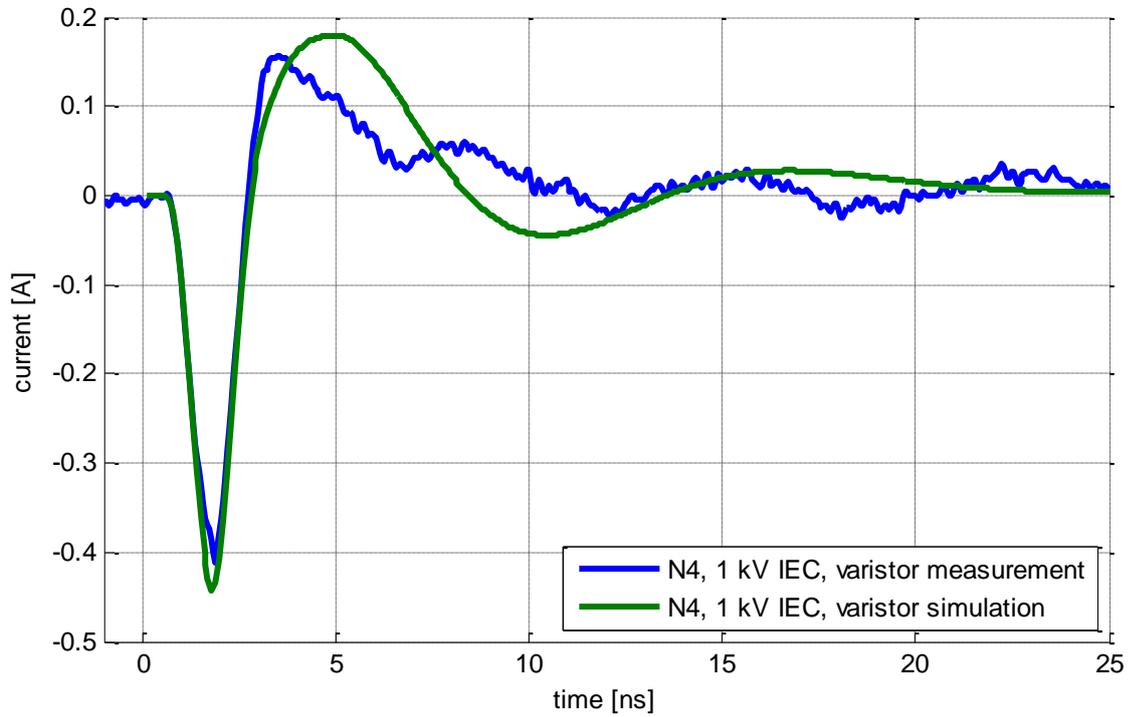


Figure 8.64: Current through node N4 with EPCOS varistor on TL2 for 1 kV discharge on TL1

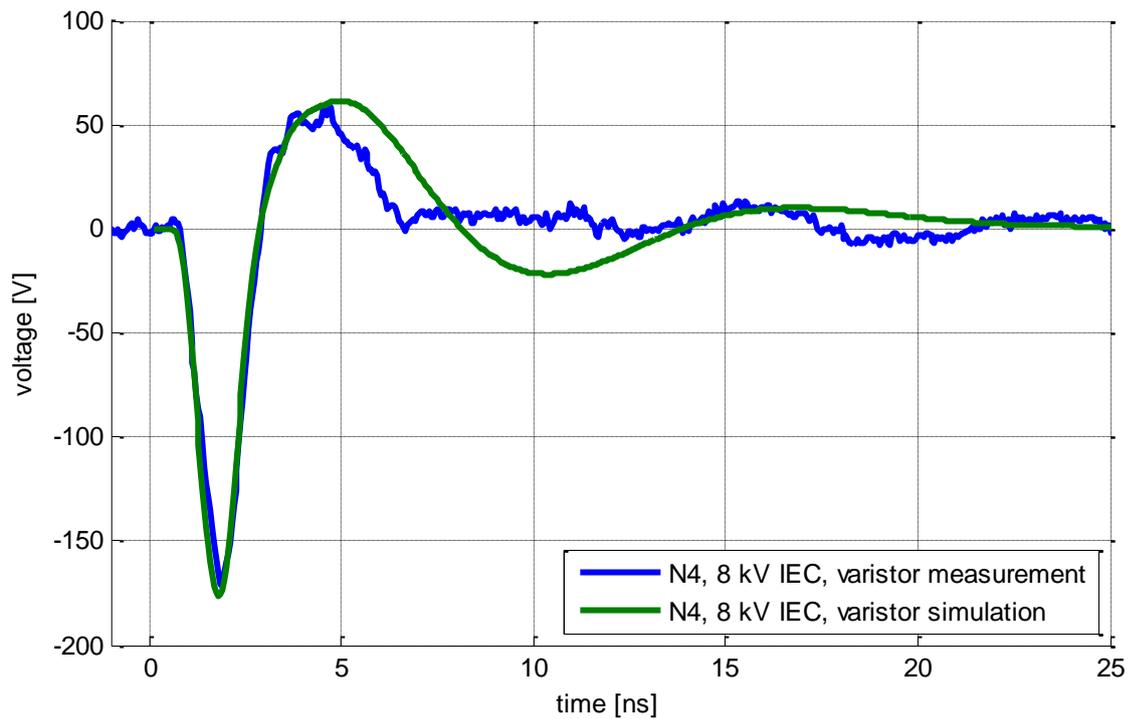


Figure 8.65: Voltage at node N4 with EPCOS varistor on TL2 for 8 kV discharge on TL1

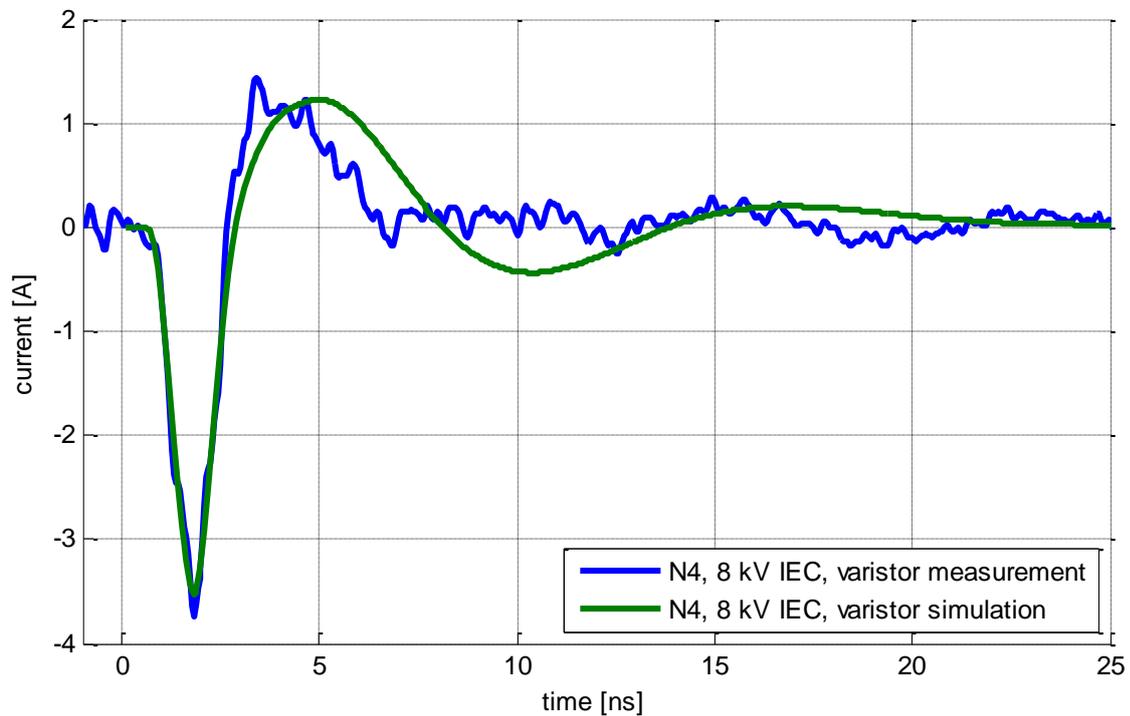


Figure 8.66: Current through node N4 with EPCOS varistor on TL2 for 8 kV discharge on TL1

8.3.5 ESD Current Coupling Case Study

Investigation about ESD current coupling is based on the trailer ECU shown in Figure 8.67. The PCB is equipped with 2 connectors. Connector 1 provides interface to the trailer socket which was identified as a potential source for ESD events. Internal vehicle pins such as LIN, CAN, supply pins and BLS pin are part of connector 2, with direct connection to vehicle cable harness.

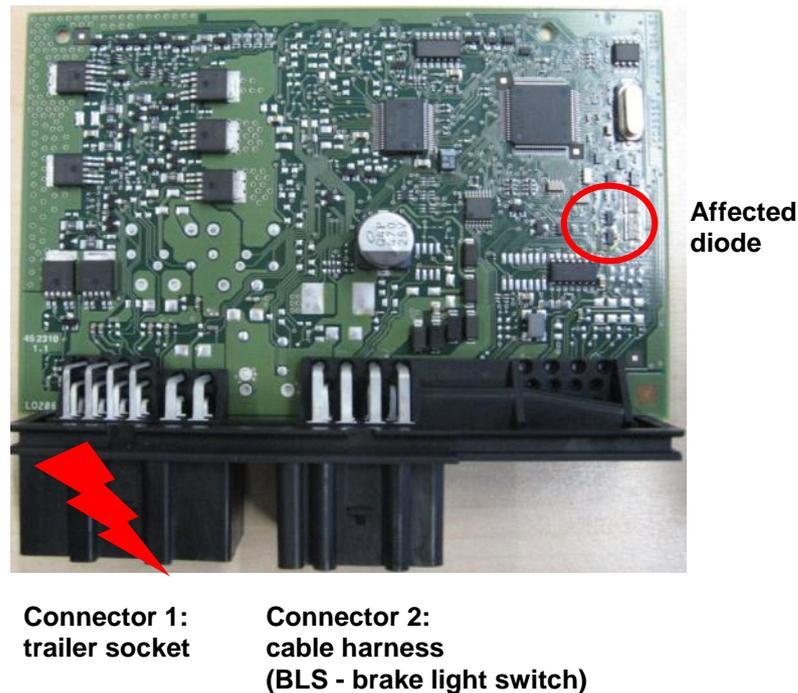


Figure 8.67: ECU PCB layout

8.3.5.1 Measurement Setup

In the circuit diagram shown in Figure 8.68 the BLS pin and KL15 pin are connected to connector 2 of the trailer ECU.

The capacitor CK1001 is not assembled on the PCB version with lower ESD robustness. In case of ESD current can be measured between D1000 and D1001 diodes using a CT1 sensor and an oscilloscope. Other current paths are negligible because of high serial resistances (R1005, R1006 and R1007). Voltage is not measured to prevent additional ground connection and current paths provided by the probe.

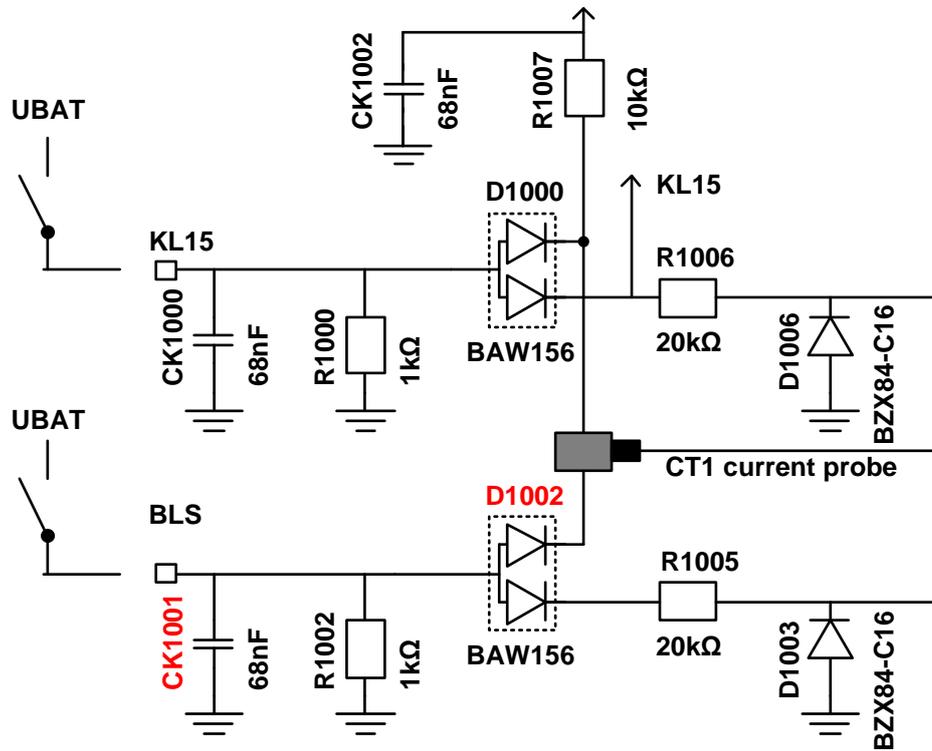


Figure 8.68: Circuit diagram of the ECU, capacitor CK1001 is not assembled on the PCB [52]

The PCB is removed from the ECU plastic housing during ESD testing. In the setup the PCB is isolated from the horizontal coupling plane by a Styrofoam block. ECU ground pins on connector 2 are connected by 100 mm wire to the HCP. UBAT connection is treated as ground for ESD signals and the KL15 pin is permanently connected to HCP by 100 mm wire. BLS is a two state signal pin. It may be optionally connected to HCP.

For measurement the PCB trace between D1000 and D1002 is interrupted and the current probe is installed using a small wire soldered between the trace ends. The ESD generator is discharged via connector 1 pins or via ECU ground plane. The setup is shown in Figure 8.69.

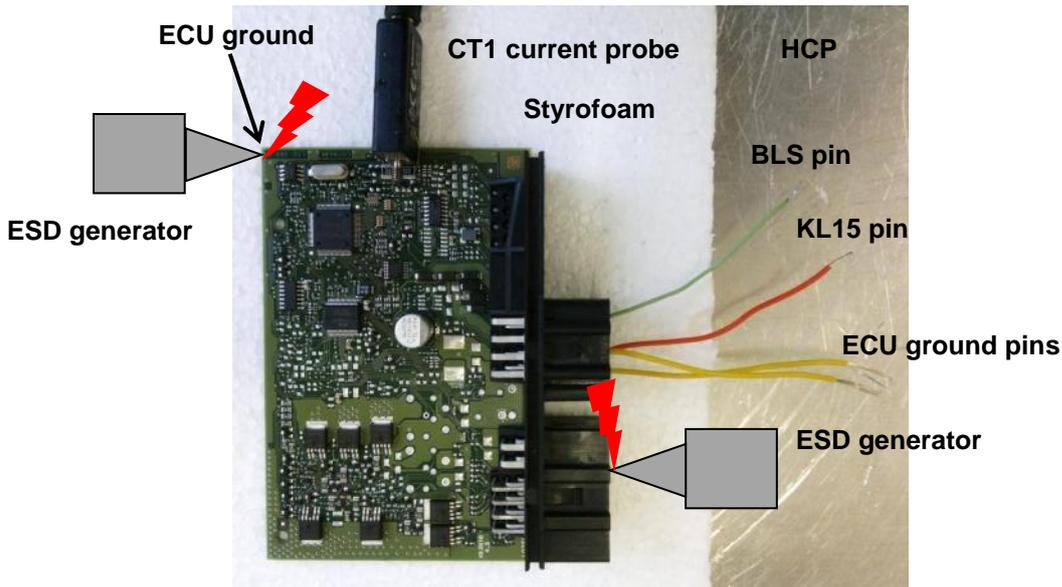


Figure 8.69: Measurement setup for system level tests of the ECU

8.3.5.2 ESD Sensitivity of Pins at Connector 1

The first measurement is done to localize the ESD coupling path for pins at connector 1. An ESD generator is discharged via pins of connector 1 and via the ECU ground plane. The IEC generator charging voltage was set to 5 kV and the current is measured at the diode. The BLS pin is left open during measurement. In Figure 8.70 average maximal / minimal amplitudes over three discharges are shown for each discharge pin of connector 1.

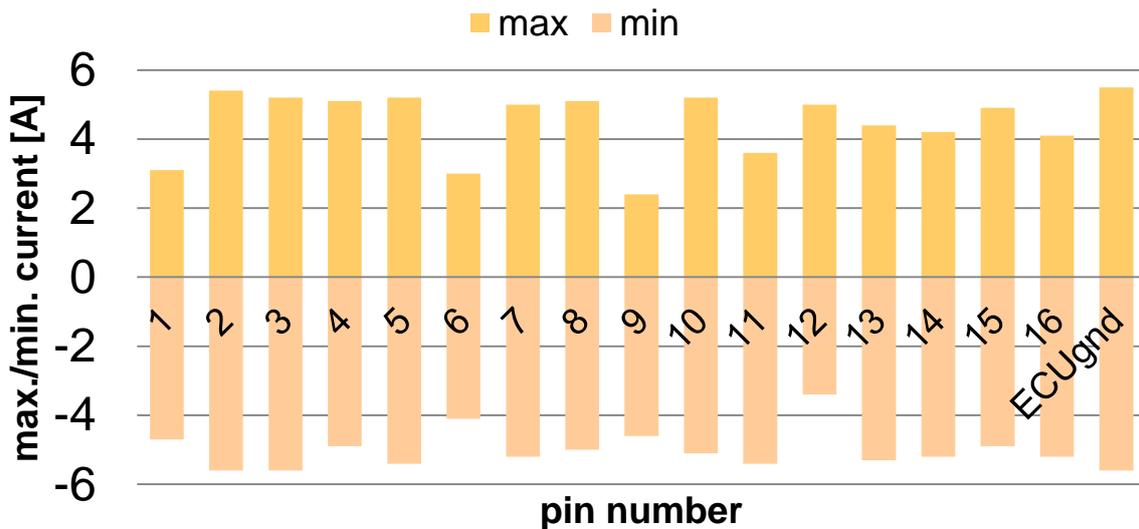


Figure 8.70: Maximal and minimal measured current amplitudes over pin number

Measured amplitudes are similar for discharges on connector 1 pins and ECU ground except for pins 1, 6 and 9. This indicates low impedance current path between diode

circuit and discharge pins. Pin 4 will be used for further study as a representative for connector 1 pins.

8.3.5.3 Testing Setups with Different Grounding Conditions

Four different setups were chosen to classify the stress for the diode in case of ESD:

1. Good connection of the ECU ground to the car body, brake light is switched off (ECU ground and KL15 are connected by 100 mm wire to HCP, BLS is left open)
2. Good connection of the ECU ground to the car body, brake light is switched on (ECU ground, KL15 and BLS are connected by 100 mm wire to HCP)
3. Impaired connection of the ECU ground to the car body, brake light is switched off (ECU ground is connected by 300 mm wire, KL15 is connected by 100 mm wire to HCP, BLS is left open)
4. Impaired connection of the ECU ground to the car body, brake light is switched on (ECU ground is connected by 300 mm wire, KL15 and BLS are connected by 100 mm wire to HCP)

Current is measured with each described setup for a 1 kV IEC discharge on pin 4 and on ECU ground. Figure 8.71 shows the measured results. Current amplitudes increase if BLS is shorted to the HCP. Inductive decoupling of the ECU ground and HCP by use of an extended grounding wire leads to higher current amplitudes. Setup 4 is the most critical one. Current shapes are similar for both discharge points.

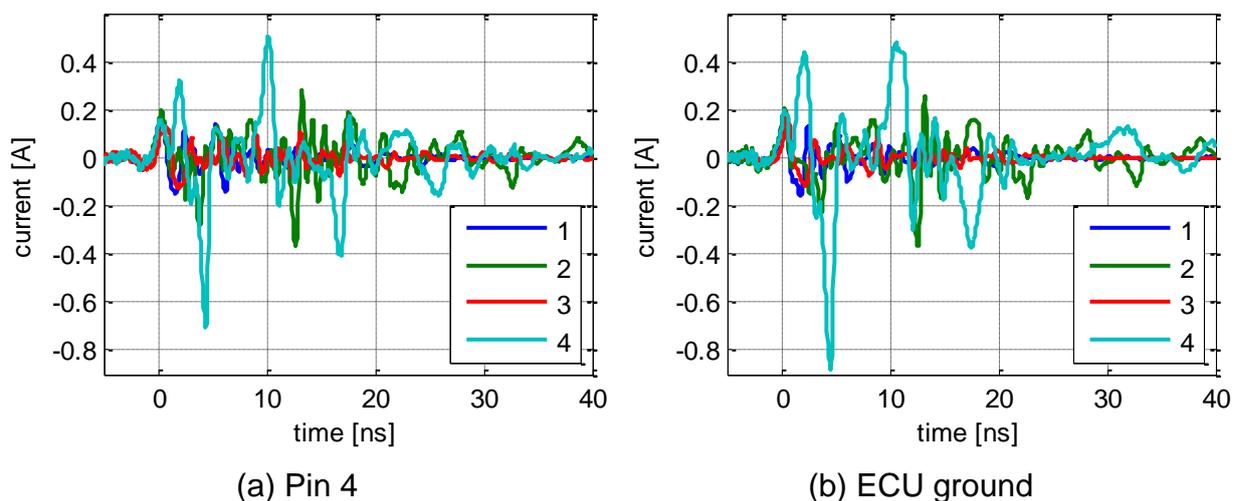


Figure 8.71: Comparison of measured currents for different setups. IEC discharge on pin 4 (a), IEC discharge on ECU ground (b)

In Table 8.9 measured amplitudes are summarized for all setups. Energy is calculated from the IV curve because only current data are available. The energies are lower than the critical value of 57 μ J measured with the TLP.

Further study will be done using setup 4 simulating an impaired ECU ground to car body connection and activated BLS. To improve reproducibility and avoid multiple current paths ECU ground plane is used as single discharge point for the next steps.

Setup	Pin 4			ECU ground		
	I_{max} [A]	I_{min} [A]	E [μ J]	I_{max} [A]	I_{min} [A]	E [μ J]
1	0.153	-0.148	0.016	0.191	-0.157	0.015
2	0.278	-0.364	0.06	0.253	-0.365	0.059
3	0.134	-0.125	0.014	0.171	-0.117	0.009
4	0.505	-0.704	0.138	0.476	-0.883	0.189

Table 8.9: Measured parameters with variation of setup for BAW156 diode and 1 kV IEC discharge

For the described configuration the maximal IEC robustness level of the diode is measured. Three discharges within 3 s are performed per voltage level. To reduce pre-damage starting charging voltage level was set to 5 kV. The charging voltage is increased in steps of 500 V until a significant rise of the leakage current is measured with the IV source meter. Figure 8.72 shows measured current shape for critical 30 kV charging voltage leading to permanent failure of the diode.

The calculated energy of the current shape from the IV curve is about 61 μ J which is 8 % less energy compared to 100 ns TLP measurement. Major part of the energy is absorbed by the diodes within 15 ns.

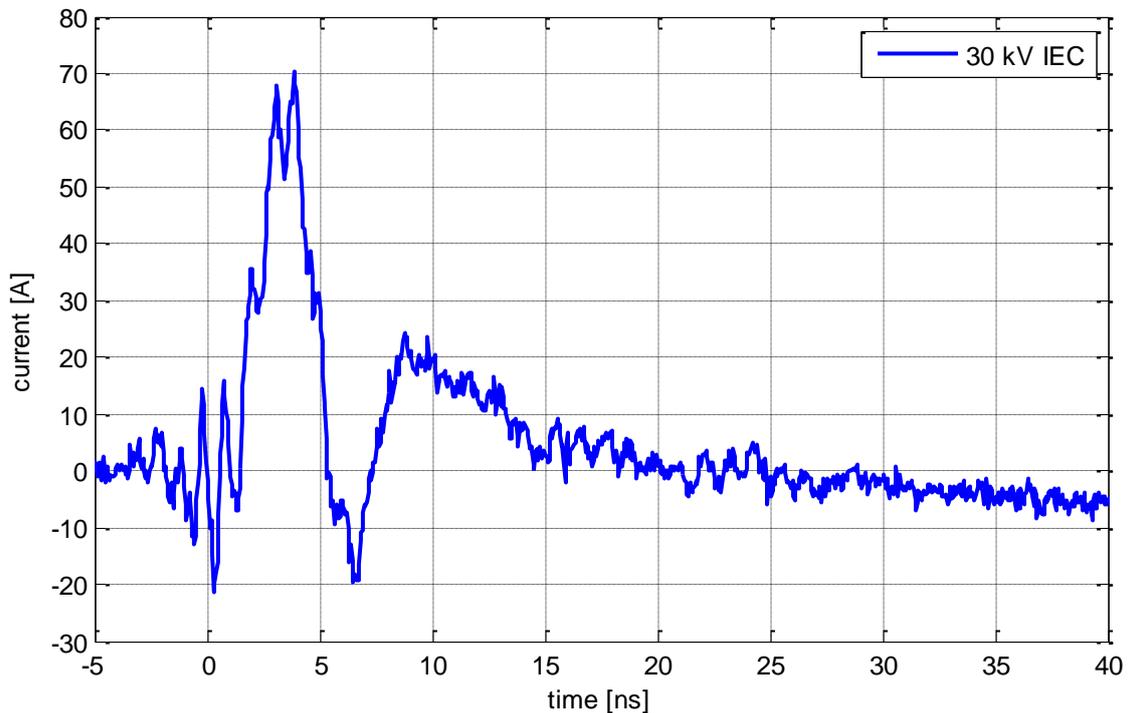


Figure 8.72: Current through the diode for 30 kV IEC discharge on ECU ground plane

ESD Generator	V_{charge} [V]	I_{max} [A]	I_{min} [A]	E_{crit} [μJ]	ΔE_{crit} [%]
IEC	30kV	70	-21	61	7.7

Table 8.10: Measured parameters of the current shape and deviation between estimated energy and 100 ns TLP energy

8.3.5.4 Investigation of Protection Strategies

Capacitors CK1000 and CK1001 were used as corrective measure in the second layout version. The effectiveness as ESD protection is investigated by measurement of the current shapes with and without capacitors. Charging voltage of the IEC generator is set to 1 kV and 5 kV. Higher voltage levels were not applied to prevent a possible pre-damage of diodes. Three setups are compared:

1. Only capacitor CK1000 is assembled on the PCB (version 1 of the trailer ECU)
2. Either Capacitor CK1000 nor CK1001 are assembled on the PCB
3. Capacitor CK1000 and CK1001 are assembled on the PCB (version 2 of the trailer ECU)

Current through the diode is shown in Figure 8.73 for the described setups. The current amplitude is lower if no ESD protection element is used. Results are similar to the case without any protection elements if both capacitors are assembled. Highest current amplitudes were measured if capacitor CK1000 is soldered on KL15.

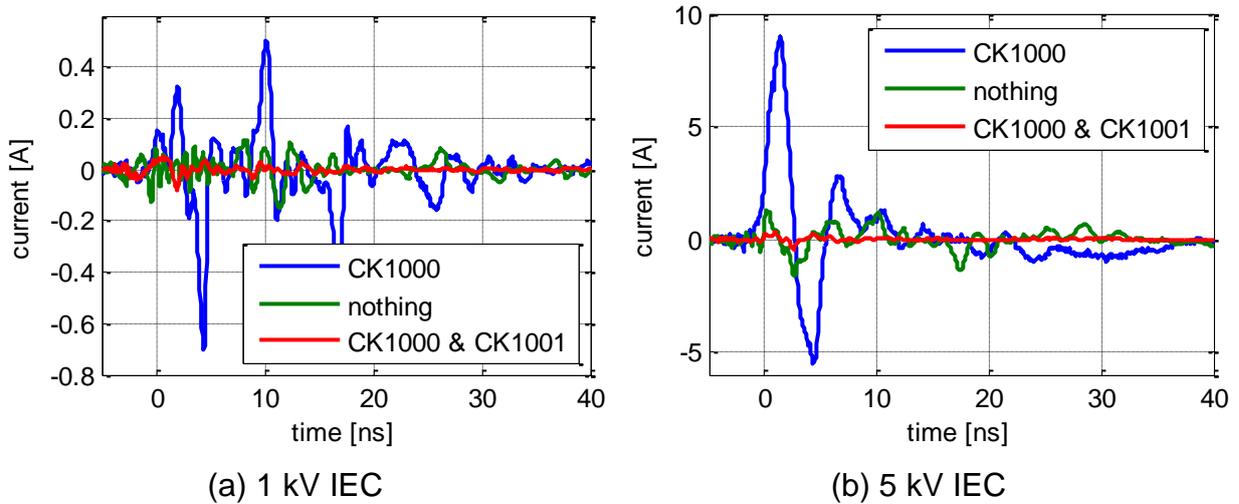


Figure 8.73: Comparison of measured currents for different protection strategies. 1 kV IEC discharge on ECU ground (a), 5 kV IEC discharge on ECU ground (b)

8.3.5.5 Analysis of the Current Path

Investigation results and the circuit diagram indicate capacitive current coupling as main failure mechanism. Following points concerning the ESD current path are considered:

1. ESD current is conducted from any pin on connector 1 through protection elements to ECU ground
2. Discharge of the ECU may be prevented due to floating connection to the car body or high impedance of the wire inductance for high frequencies
3. Capacitor CK1000 is a short for high frequency content of the ESD pulse
4. KL15 and BLS cable connectors can be modeled as inductance and prevent immediate discharge of the ECU
5. KL15 node is on the same potential as ECU ground
6. A potential difference is created between KL15 pin and BLS pin
7. ESD current flows through the diodes

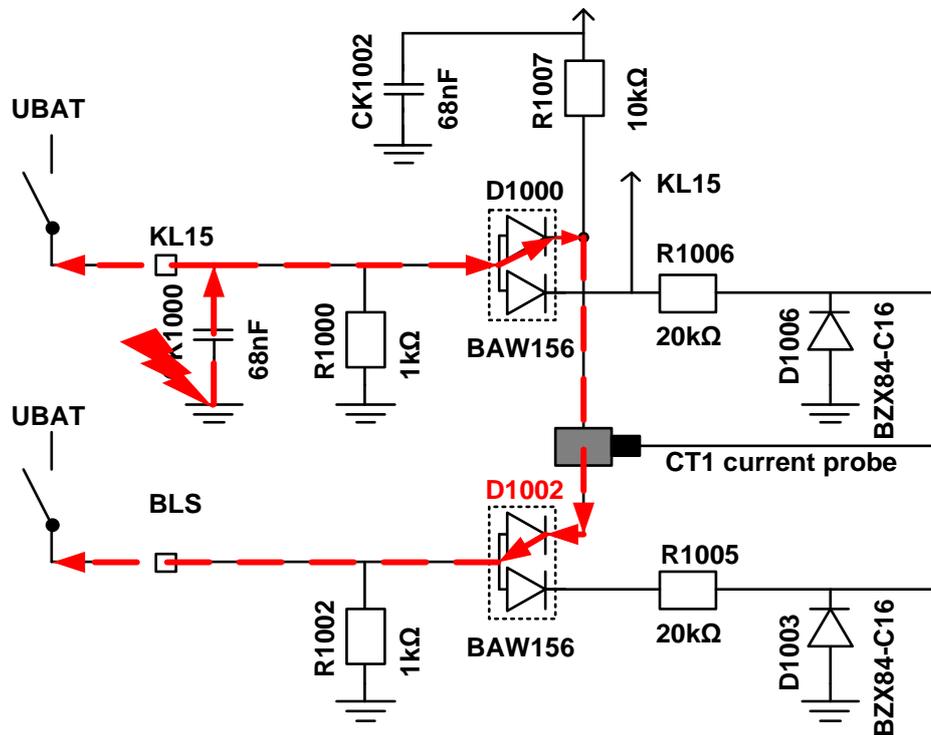


Figure 8.74: Circuit diagram of the ECU and possible current path

Current through the diodes increases with the length of the grounding wire from ECU ground to the car body. If the brake light is switched off, no current path through diodes might be established. If capacitor CK1001 is soldered on the ECU, the potential of KL15 pin is the same as of BLS pin. If both capacitors are assembled the circuit becomes symmetrical and no current will flow through diodes. Discharge is going through the cable harness. A small current still can be measured due to tolerances of devices (see Figure 8.73).

If capacitor CK1000 is not assembled, the main current path between diodes and ECU ground is removed. The capacitors can prevent ESD failure due to capacitive coupling from the ECU ground plane but do not provide any protection for ESD pulses coming from KL15 or BLS pin.

8.3.5.6 Simulation-Based Analysis

To validate measured results a simplified electrical circuit of the ECU diode branch is implemented (Figure 8.75). Branches with serial resistor R1005, R1006 and R1007 were not considered, due to its high current restriction. The BAW156 is modeled as a single diode according to the method presented in section 7.6. PCB traces from diodes to ECU connector are modeled by inductor and capacitor. Wiring from connector pins to HCP are simulated as inductor ($L' = 1 \mu\text{H/m}$). Coupling effects

between ECU ground and HCP are considered with a capacitor. A NoiseKen ESD generator model is used as ESD source in the simulation.

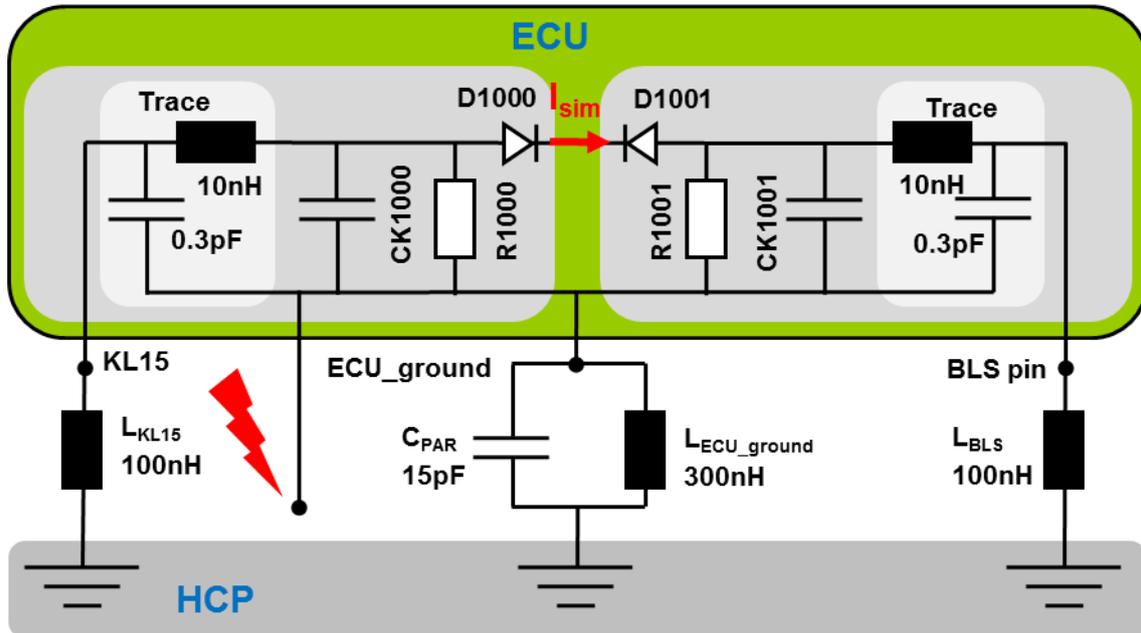


Figure 8.75: Simulation setup for trailer ECU

In Figure 8.76 simulation results are compared with measurement. A good matching of the first peak can be observed. Better results could be obtained by improved modeling of all parallel current paths. It can be shown by simulation that the failure current path is provided by the capacitor CK1000.

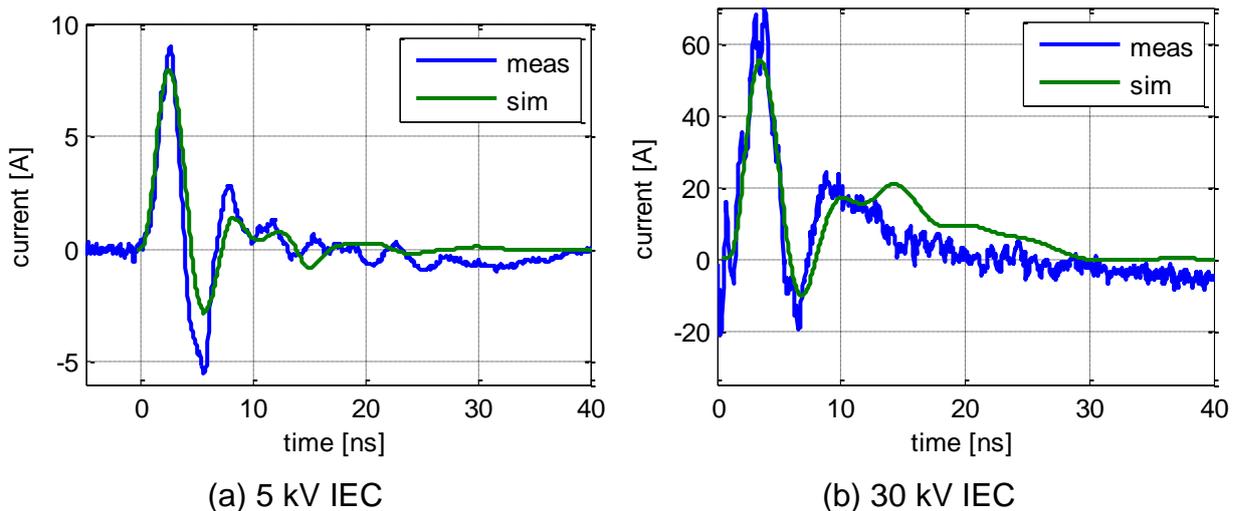


Figure 8.76: Simulated and measured diode current

In Table 8.11 simulated and measured values are compared. Absorbed energies of diodes D1000 and D1001 differ according to their opposite arrangement. Calculation of energy of D1000 with measured shapes is achieved using the measured IV curve.

Setup	Measurement	Simulation	Deviation	State
D1000, 5 kV	2.9	2.4	17 %	non defect
D1001, 5 kV	3.5	3.1	11 %	non defect
D1000, 30 kV	30	12	60 %	non defect
D1001, 30 kV	62	63	1.5 %	defect

Table 8.11: Comparison of energies for diodes D1000 and D1001 for different charging voltage

Diode failure is simulated for 30 kV IEC discharge. This value matches with measurement results. It can be seen that the simplified circuit represents well the relevant part of the ECU.

The IEC ESD discharge assumes human as a source. Parameters of a trailer discharge may be different considering current shape and energy. Three additional ESD sources are considered in simulation:

- Basic IEC generator according to the IEC 61000-4-2, detailed description is presented in Section 7.3.2
- Serial RC network. Trailer hard discharge with low serial resistance, capacity can be higher depending on trailer dimensions.
- A cable discharge, when connecting a trailer to a towing vehicle. In simulation a 1 m transmission line is used. As characteristic line impedance of a wire within a cable harness 200 Ω were chosen.

Charging voltage is increased in steps of 500 V until a damage of a diode D1000 or D1001 is observed. Figure 8.77 shows the critical current shapes for defined ESD stresses.

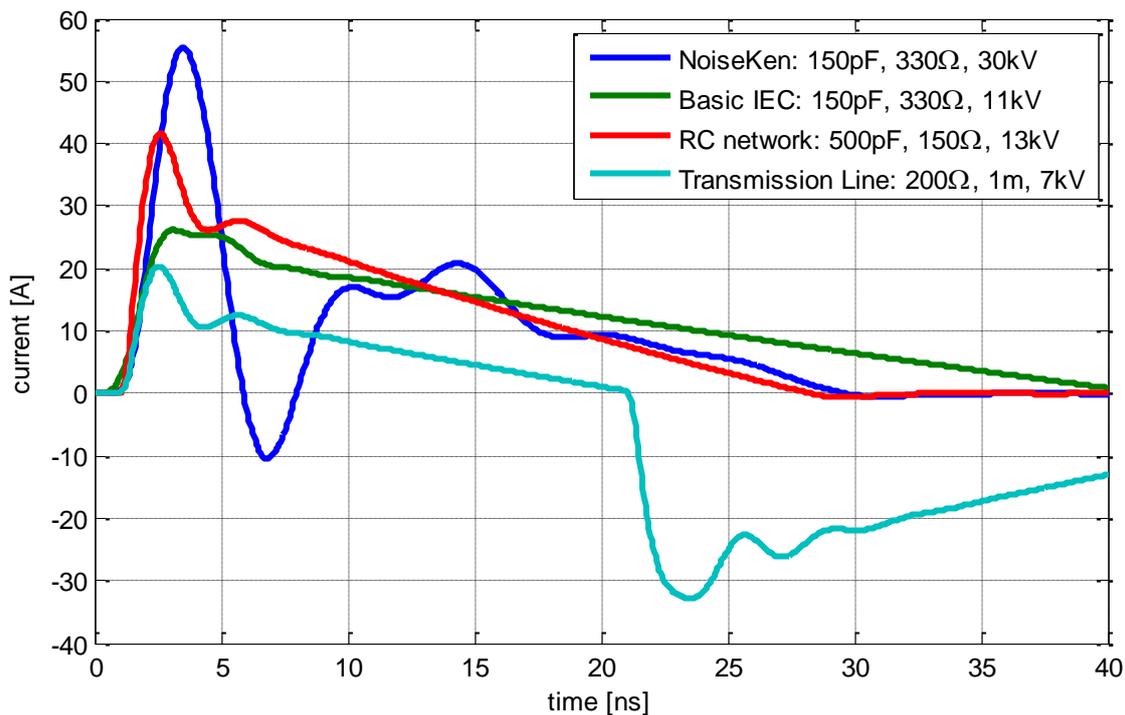


Figure 8.77: Diode currents for different ESD stress levels

Maximum voltage level is reached by discharge of the NoiseKen ESD generator. For basic RLC generator discharge failure is detected at 11 kV charging voltage level, which is about 37 % of the critical NoiseKen level although both ESD generator models fulfill the IEC 6100-4-2 standard. Reflections of a cable discharge lead to a failure of D1000. In Table 8.12 all relevant parameters are compared.

ESD generator	V _{charge} [kV]	I _{max} [A]	E _{D1002} [μJ]	E _{D1000} [μJ]
NoiseKen: 150 pF, 330 Ω	30	56	63	12
Basic IEC: 150 pF, 330 Ω	11	26	59	7
RC network: 500 pF, 150 Ω	13	42	61	9
Transmission Line: 200 Ω, 1 m	7	20	45	60

Table 8.12: Comparison of failure levels for different ESD sources

8.3.5.7 Conclusion

Destruction of the trailer ECU by an ESD event was reproduced in the lab. The affected diode was characterized, the failure was modeled in thermal domain. A possible failure path was described. The modeled circuit robustness to three additional ESD sources was investigated.

Capacitive current coupling from the ground plane to the diode branch was observed. Failure mechanism can be referred to an impaired grounding connection of the ECU.

The study has shown that good ground connection can help to prevent ESD damages. ESD failure was observed in case of inductive decoupling of the ECU ground from the vehicle body. Today's ESD standards prescribe a good grounding for the tests. Often metallic body components are exchanged by plastic parts. This might prevent short grounding connections in some cases. To consider the impact of grounding on ESD tests artificial vehicle network boxes, known from EMC testing could be adopted for ESD system level test as well.

Investigation of the diode failure under different stress conditions has shown that destruction using non-standardized ESD waveforms is possible at lower charging voltage levels. For a trailer discharge it is assumed that the capacitance increases and the discharge resistance decreases compared to an IEC generator. This combination causes short rise times and high current peaks.

8.4 ESD Field Coupling into PCB Structures

The coupling of ESD into PCB structures has been investigated on two examples. One being the discharge into a USB connector, the other the discharge into or close by an enclosure. The enclosure contains a simple PCB.

8.4.1 Field Coupling into USB Connector

ESD to USB Connectors often hit the shell which is usually not well connected to a partial chassis. These simulations analyze basic coupling effects and parametric influence of different grounding configurations on voltages coupled to traces and to flex cable like board to board connections. Investigated, but not fully shown in this brief summary have been:

- Effects of the USB-shell to enclosure connection, as this are the primary placed to divert the current away from the electronics. However, this is only possible if a metallic chassis is present.
- Changes in the connector PCB connection to reduce the mutual coupling between the ESD current path and the PINs of the USB cable
- Chassis connections between the PCB and the chassis
- Types of flex cable connections used, for example, single layer, dual layer, and signal topology such as G D- G D+ G vs. G D- D+.

This brief summary of these simulations quantifies the effect of the shell connection and the location of the taps which connect the USB connector to the PCB.

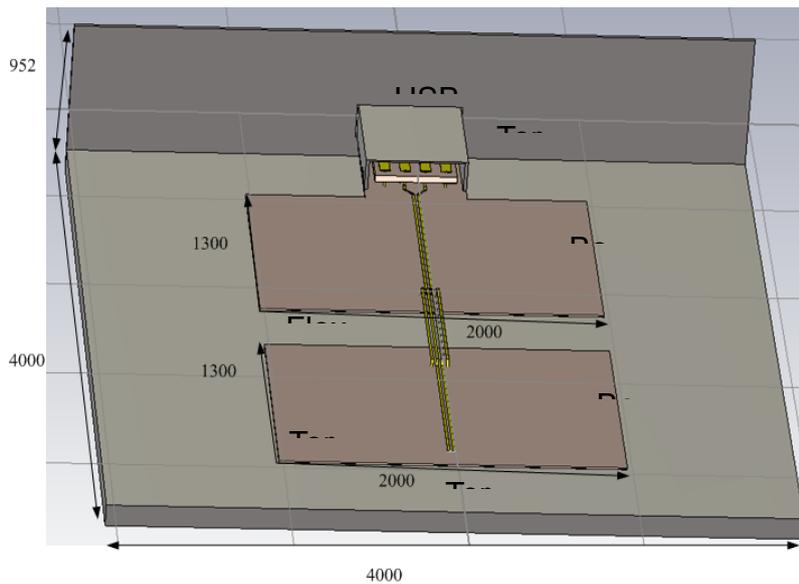


Figure 8.78: Geometry of the two boards USB port system

The USB port system is shown in Figure 8.78. The USB connector connects to the PCB ground by two side taps. The location of the side taps has been set upon commercially available USB connectors. Several posts are used to connect the PCB ground to chassis, or the PCB is connected directly underneath the connector. A flex cables connect two boards. Objective is to determine the main coupling mechanism and to quantify the effect of different grounding topologies. Such a configuration could be part of an entertainment system inside an automobile.

The excitation is performed using an ideal current source placed between the chassis and the USB connector shell. The current waveform is taken from a NoiseKen 2000 ESD generator at 1 kV charge setting.

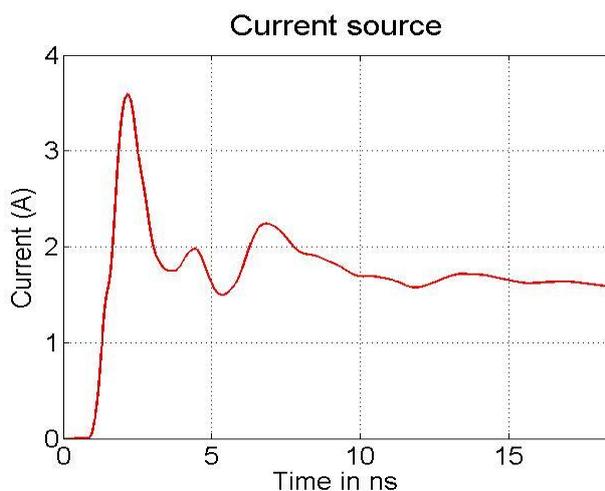


Figure 8.79: Current source waveform

The current is injected at the top center of the USB shell. A typical current flow path is from the shell via the taps to the PCB and then to ground.

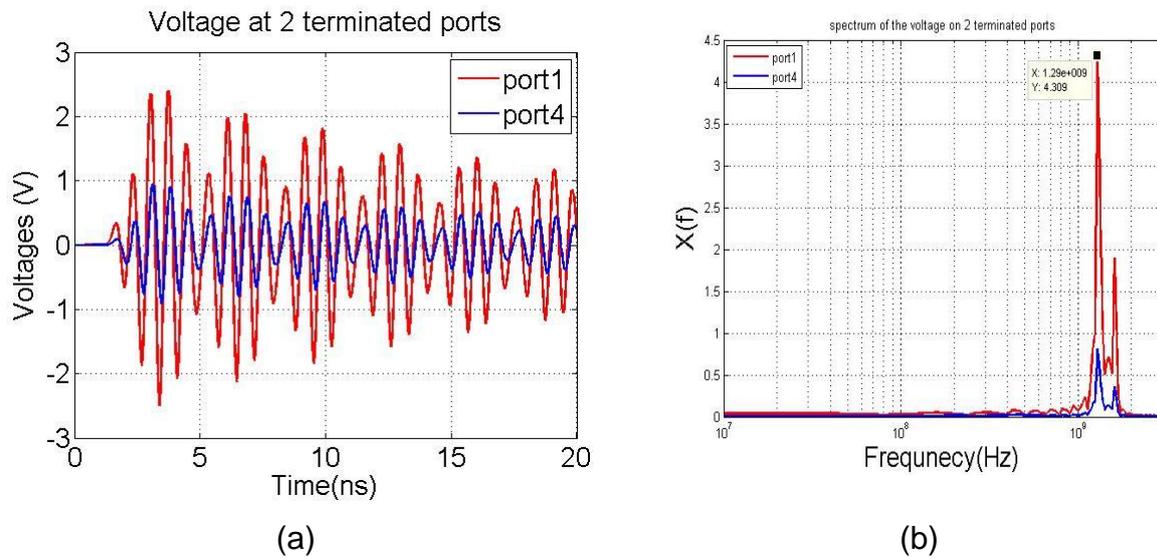


Figure 8.80: Coupling voltage at port 1 and port 4 (a), their spectrum (b)

The coupled voltage on port 1 (at the USB connector, terminated with 50 ohm) and port 4 (at the IC end of the trace, also terminated with 50 Ohm) and spectrum are shown in Figure 8.80. The peak to peak value of the voltage on port1 is 4.8 V, and the voltage on port 4 is 1.6 V. The ring frequency is 1.29 GHz. The voltage difference between the two ends of the board is a result of the S41 of the board.

The dominating coupling between the ESD current and the USB traces takes place at the tap of the connector. The flux of the ESD current flowing in the tap will couple to the PINs of the USB connector. The simulation results show that the coupling is governed by:

- The current's derivative. If the current is diverted to the chassis by directly connecting the USB connector the induced voltages will be less
- If such a connection is not possible, for example, the chassis is made from plastic, then the distance between the tap and the USB connector PINs can be used to reduce coupling by increasing this distance, or by adding extra ground PINs as shield around the contact PINs of the USB connector (this would require a special connector footprint).

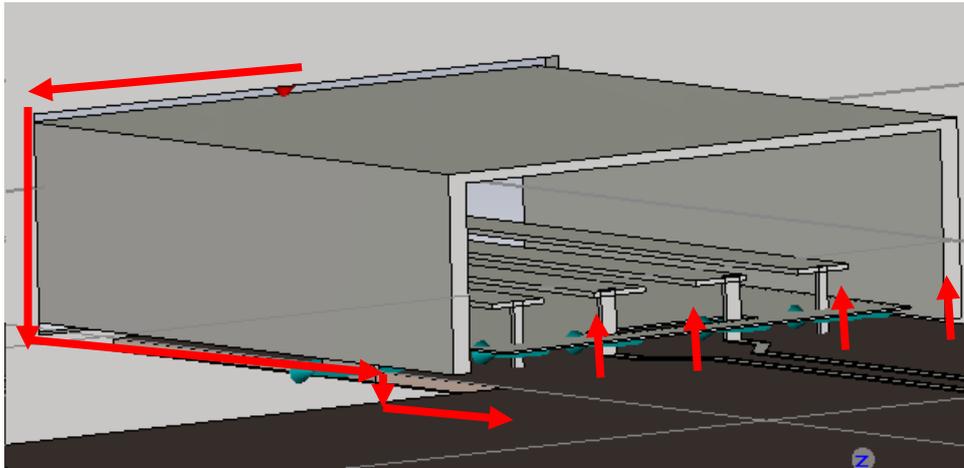


Figure 8.81: ESD current path via the tap that connects the USB shell to the PCB ground

8.4.1.1 Side Connection

The side connection of USB shell to the chassis is shown in Figure 8.82.

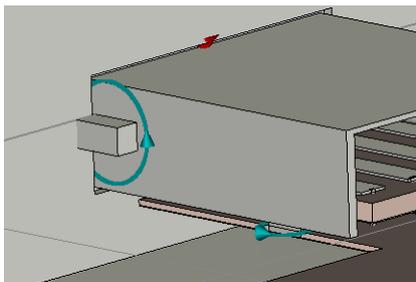


Figure 8.82. Illustration of the side connection that diverts the ESD current to the chassis

If such a connection can be implemented the current from the ESD source will mainly pass via the side connection as it provides the lowest impedance path. Small portion of current will flow via the taps. Using this model the induced noise voltage will be reduced from 4.8V (no side connection of the USB) to 0.18V at 1kV ESD charge voltage. If 4kV are used, which is the minimal value for most for IEC 61000-4-2 testing, the voltage would still be around 0.8V. This will certainly lead to disturbances on the USB traffic. Depending on the correct implementation of the USB protocol such a brief interruption may not be noticed by the user, or it may cause the USB device to be disconnected. Details will depend on the software implementation, on the USB device and on other routing and filtering in the board.

The simulation result is compared to the normal case (no side tap), as shown in Figure 8.82. The current of each critical locations are simulated to indicate the current path. The current comparison result is shown in Table 8.13. 90% of the source current flows via the USB shell connection to the chassis, a small portion current still flows via the taps which have strong coupling to USB pin.

- Tap1, Tap2: Connection of the USB connector to the PCB

- Post_near1, Post_near2: Two posts that connect the first PCB to the chassis close to the USB connector
- Post_fa1, Post_far2: Two posts that connect the first PCB to the chassis at the other end of the PCB
-

Location\ Current (A)\ geometry	source	Connection of USB shell to chassis	Tap1	Tap2	Post_ near1	Post_ near2	Post_ far1	Post_ far2
With side connection	3.6	3.2	0.32	0.16	0.16	0.24	0.035	0.023
Without side connection	3.6	No data	2.5	2.5	2.05	2.05	0.18	0.18

Table 8.13: Current at different locations with and without connection of the USB shell to the chassis

	Port 1 voltage [V]/ ring frequency [GHz]	Port 4 voltage [V]/ ring frequency [GHz]
With Connection of the USB shell to chassis	0.18/1.29	0.1/1.29
Normal	4.8V/1.29	1.6/1.29

Table 8.14: Coupled voltages on the trace comparing the connected to the not connected case

The coupling voltage on port 1 and port 4 and their spectrum are shown from Figure 8.83. Port 1 is at the USB connector and port 4 is at the other end of the trace (IC end). The peak to peak value and the ringing frequency of the coupled signal on the two ports are shown in Table 8.13: Current at different locations with and without connection of the USB shell to the chassis

The coupled voltage on port 1 is reduced by a factor of 25 by the USB shell chassis connection. For port 4 the ratio is 16. This indicates the importance of diverting the current away from the taps in the USB connector for this USB connector geometry. A next simulation set investigates the effect of moving the taps away from the PINs to reduce coupling.

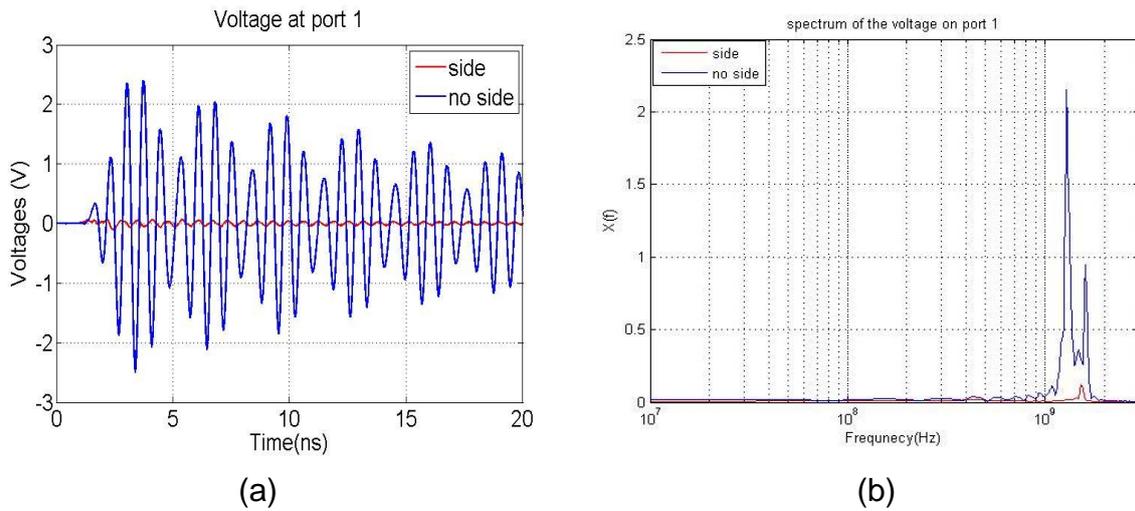


Figure 8.83. Coupled voltage on port1 (a) and its spectrum (b)

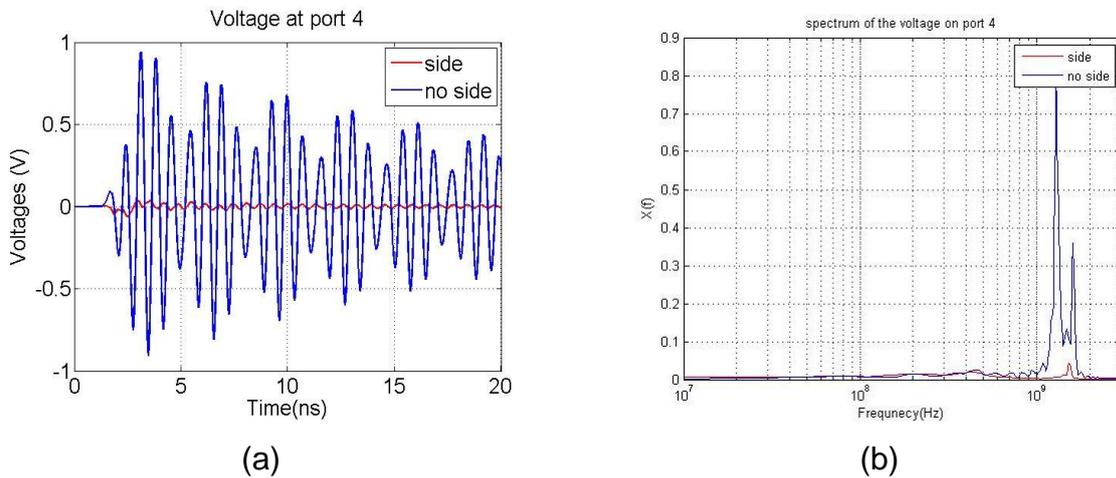


Figure 8.84. Coupled voltage on port4 and its spectrum

8.4.1.2 Increase of the Distance between the Tap and the USB Pins

As explained before, the distance between taps and the USB pins determines the mutual inductance. By increasing the distance, the current generated magnetic flux density decreases, the inductive coupling reduces. As shown in Figure 8.85 the tap is moved to a new location, 300 mil away from its original location (indicated by Tap 1).

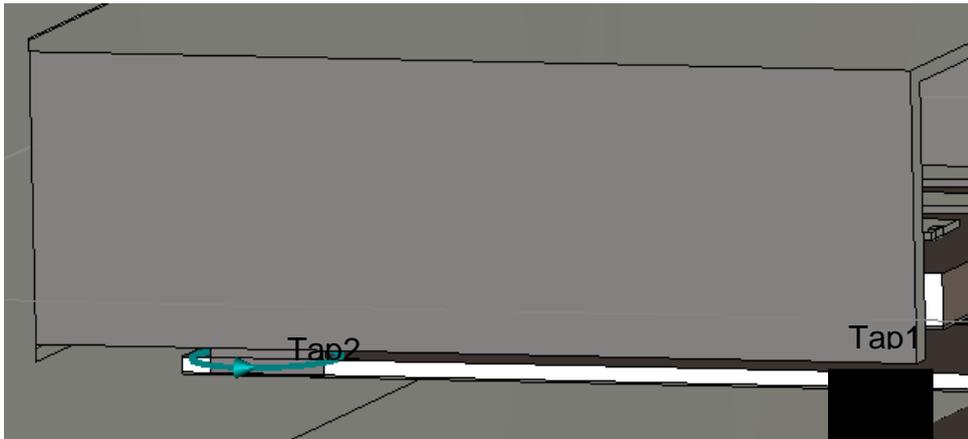


Figure 8.85. Increased distance between the tap and the USB pins (Tap 1 indicates the old position, Tap 2 indicates the new position).

The simulated currents and voltages are shown in Table 8.15 and the coupled voltage is shown in Table 8.16. The current at the USB data pin is reduced by a factor of 8 relative to the original case (no USB side shell connection to the chassis).

Location\ Current(A)\ geometry	source	Tap1	Tap2	Post_ near1	Post_ near2	Post_ far1	Post_ far2	USB pin data
Far tap	3.6	2.4	2.4	2.05	2.05	0.18	0.18	0.017
Normal position tap	3.6	2.5	2.5	2.05	2.05	0.18	0.18	0.13

Table 8.15: Current at different coupling locations of far tap and normal tap

Location\ Voltage (V)\geometry	Port 1 voltage [V]/ ring frequency [GHz]	Port 4 voltage [V]/ ring frequency [GHz]
Far tap	0.6/1.29	0.42/1.29
Normal position tap	4.8V/1.29	1.6/1.29

Table 8.16: Coupled voltage on the trace comparing two tap positions.

The voltage waveforms for the two cases are shown in Figure 8.86.

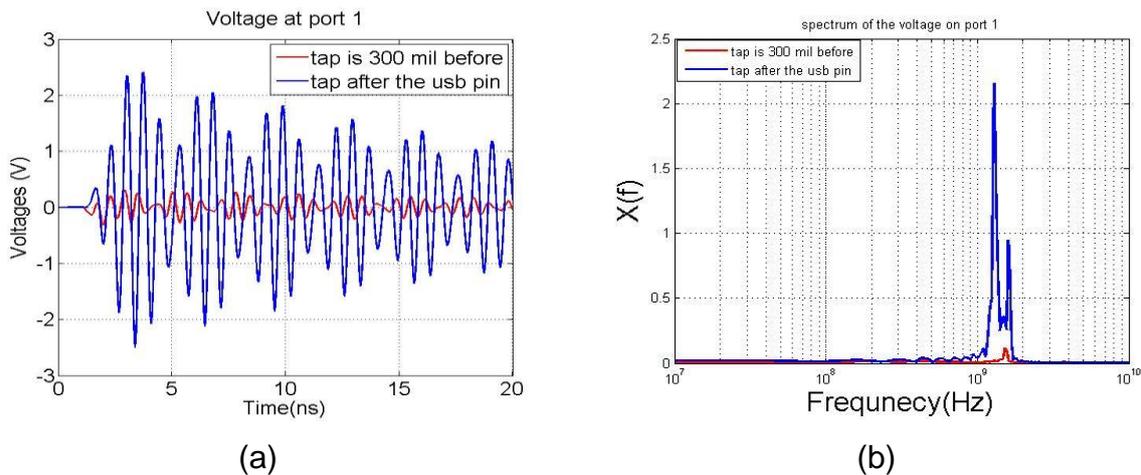


Figure 8.86. Coupled voltage on port1 (a) and spectrum (b)

8.4.2 Field Coupling into PCB Structure Closed by an Enclosure

The objective of the simulation is to analyze and quantify the coupling to a PCB in an enclosure from a discharge of an ESD generator. Two topologies are investigated: direct discharge to the enclosure and indirect discharges close to the enclosure into a large ground plane. The data are analyzed by the voltage induced at port 2, which terminates a trace on the PCB. The test environment consists of:

- An ESD generator
- A PCB inside an enclosure (dual layer)

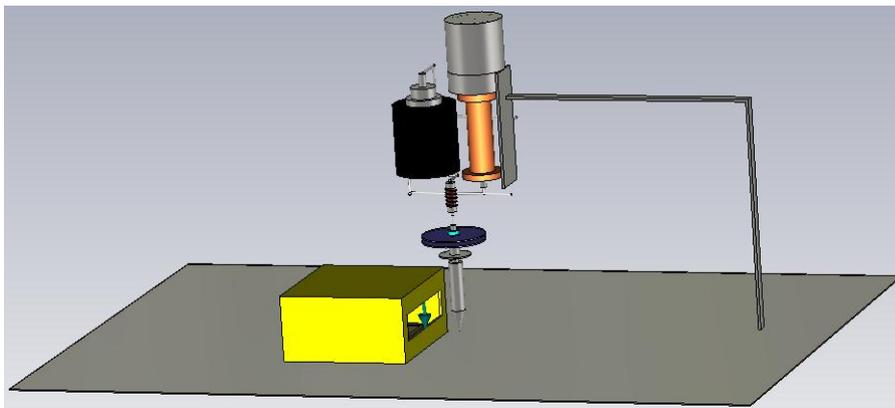


Figure 8.87. Simulation model

The ESD simulator models the Noise Ken ESD generator. The outside dimensions of the enclosure are 100mm×100mm×60mm. It is placed on the ground plane. The enclosure wall thickness is 3mm which is not relevant if a metallic enclosure is simulated, but is relevant if a semi-conducting plastic enclosure is investigated. There is a PCB in the enclosure. The PCB is a very simple PCB having two ports and a 50 Ohm trace. The PCB model assumes 1.6 mm FR-4 and 3mm wide traces. The structure is shown in Figure 8.87. The PCB is placed inside the enclosure as shown

in Figure 8.88. The edge of the ground of the PCB is contacted to the wall of the enclosure. The enclosure is metallic and has a slot to allow for coupling. The voltage across the slot is also being monitored during the simulation.

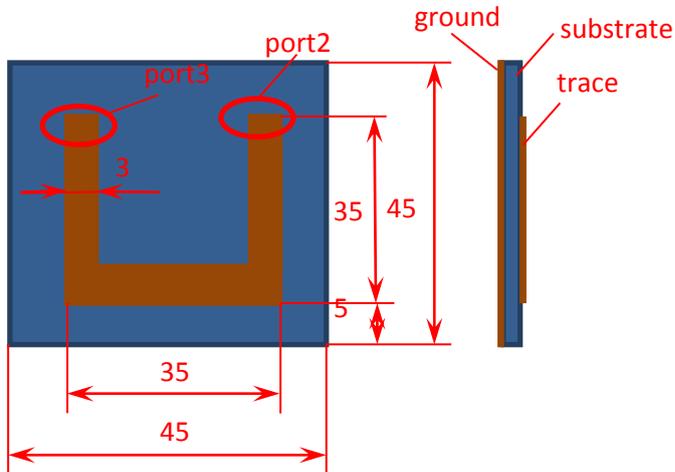


Figure 8.88. Structure and size of the PCB

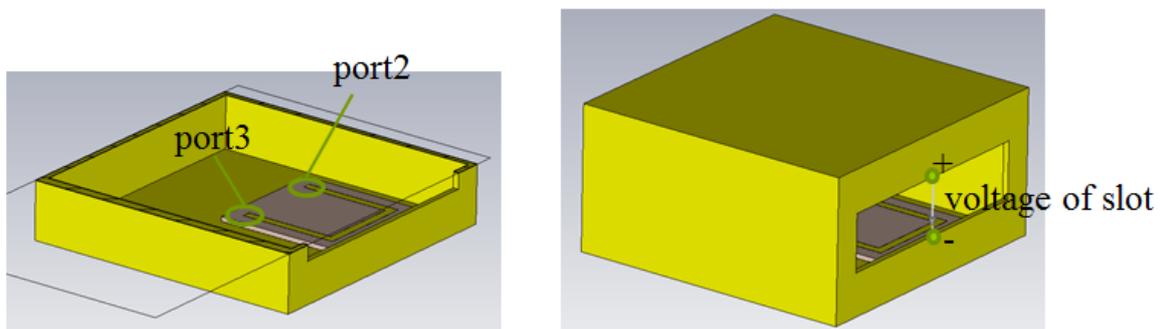


Figure 8.89. The structure of the PCB and the enclosure

In the simulation, the following factors are considered as parameters.

- The discharge location
- The size of slot
- The characteristics of materials filling the enclosure (effect on the Q-factor)
- The size of enclosure
- The material of the enclosure

In all the simulation the dimension of the enclosure are 100mm×100mm×60mm, and the size of slot is 80mm×20mm, and the PCB is 3mm beneath the bottom edge of slot, except if specified differently.

8.4.2.1 Effect of Discharge Location on Coupling

The coupling of ESD noise inside the enclosure is dominated by the resonance frequency of the enclosure as no cables enter the enclosure. The Q-factor of the

enclosure has been reduced by filling it with a virtual material having the following properties: ($\epsilon_r=1$, $\sigma=0.003$ S/m). There are four discharge locations Figure 8.90

Location 1: The discharge location is on the ground plane, which is an indirect discharge.

Location 2: The discharge location is at an upper corner of enclosure near slot, which is a direct discharge

Location 3: The discharge location is at the middle of the edge of the enclosure above slot, which is a direct discharge.

Location 4: The discharge location is at the middle of an upper edge of enclosure far away the slot, which is a direct discharge

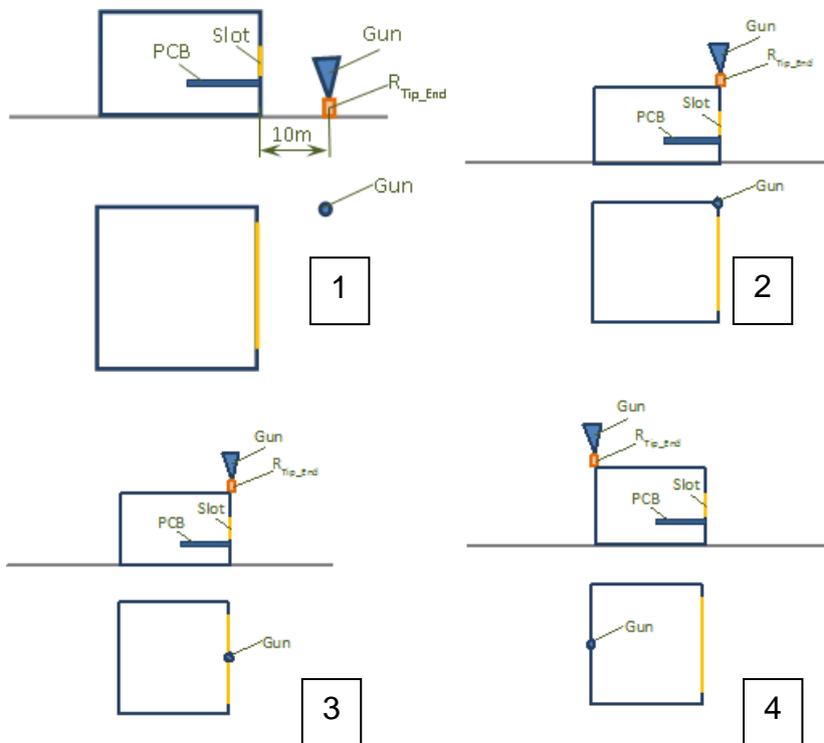


Figure 8.90: Discharge locations

The simulation results are as follows:

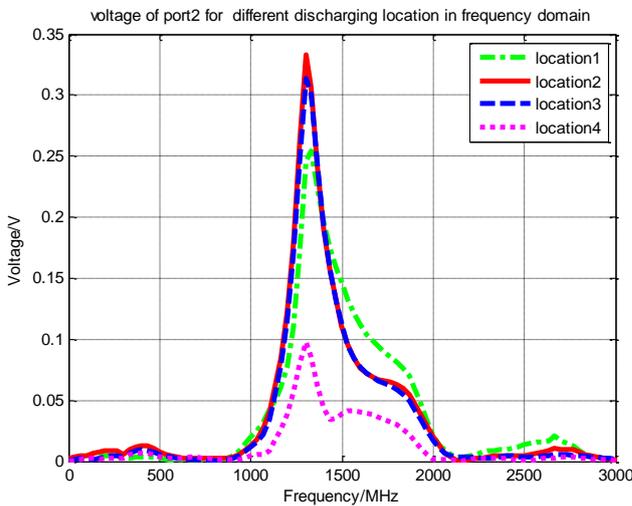
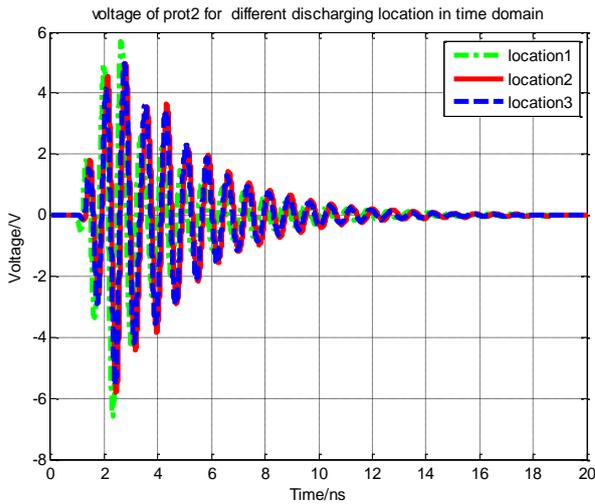


Figure 8.91: Voltage of port2 for different discharge location in time domain and in frequency domain

The induced voltages are dominated by the enclosure resonance. All locations, except the far away location lead to approximately the same voltage. From the Figure 8.91, the Table 8.17 is obtained.

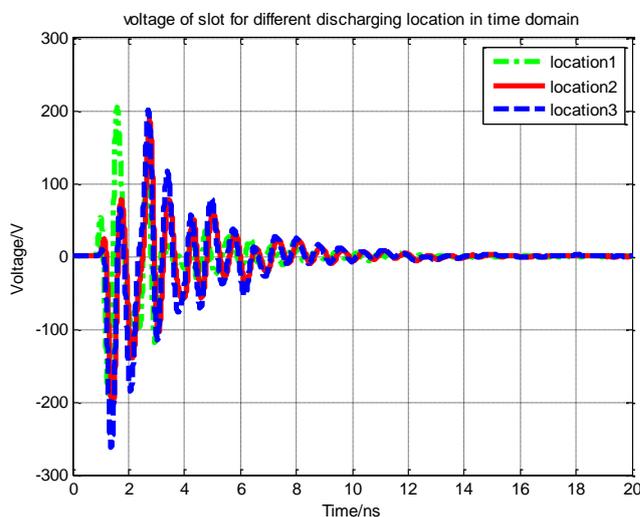
Discharging location	V _{pp} /V	Resonant Frequency/GHz	Magnitude at Resonant Frequency/V
Location 1	12.30	1.334	0.2543
Location 2	10.80	1.300	0.3328
Location 3	10.53	1.300	0.3133
Location4	3.802	1.300	0.09767

Table 8.17: Voltage of port2 for different discharge location

Note: V_{pp} is the peak-to-peak voltage obtained from the time domain data shown in - Figure 8.91.

Based on Figure 8.91 and Table 8.17 there is little effect of the discharge location on the resonant frequency. This is also not to be expected as the ringing is determined by the enclosure resonance frequency. The voltages change little between the locations selected, except for the far away location (4). Here the voltage is obviously reduced.

The main conclusion is the importance of resonances inside the system. At these resonant frequencies the coupling to the spectrum of the ESD current and fields is strongly enhanced. Such effects have also been observed during ESD testing of a larger set of products: Each product and each test point had its own sensitive frequency ranges which let to large variations of test results if different ESD generators had been used. The reason was that each model ESD generator has different spectral composition and if a specific ESD generator has strong spectral components in a region at which a test point is sensitive the system will be upset at lower ESD generator settings than compared to the case in which the specific ESD generator has low spectral content. Further information on the underlying reasons for test result variations of contact mode ESD testing for system upsets can be found in 329[96].



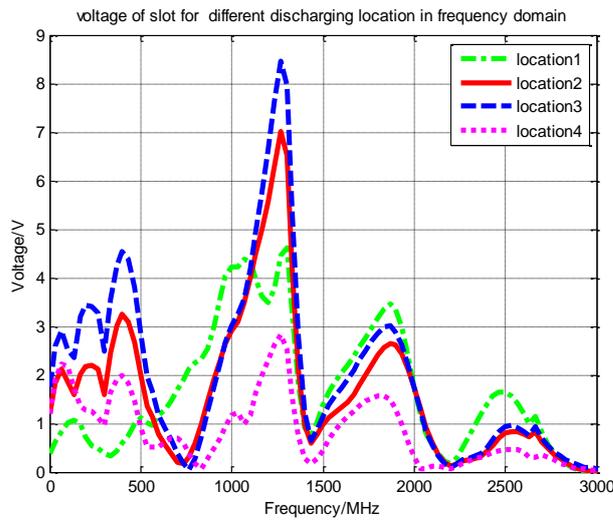


Figure 8.92: Voltage across slot for different discharge location in time domain and in frequency domain

Discharging location	V _{pp} /V	Resonant Frequency /GHz	Magnitude Resonant Frequency/V	at
Location 1	392.5	1.300	4.626	
Location 2	326.4	1.267	7.009	
Location 3	385.6	1.267	8.456	
Location 4	130.0	1.267	2.831	

Table 8.18: Voltage across the slot for different discharge location

The voltage across of the slot reaches many hundred volts. The spectral content contains energy at the enclosure resonance but also at other frequencies.

The empty cavity resonances of the enclosure do not match the measured ringing frequencies. This is due to introducing the PCB into the enclosure which sets up different resonance frequencies, as shown in Table 8.19.

PCB	1 st /GHz	2 nd /GHz	3 rd /GHz
Without PCB	2.198	3.463	3.482
With PCB	0	0.855	1.415

Table 8.19: Resonant frequency of enclosure

Note: The enclosure is closed, without slot. The position of PCB in the enclosure is just as Figure 8.89.

The following conclusion can be draw based on the first set of simulations:

- 1) The spectrum of the induced voltage is dominated by the resonance frequency of the loaded enclosure.
- 2) The slot size, the enclosure size and the PCB location and size determine the resonance frequency
- 3) Voltages of many hundred volts are induced on the slot.

8.4.2.2 Effect of Slot Height & PCB Location Coupling

This is to find the effect of slot height & PCB location on the coupling. When the slot height is altered, the distance between PCB and the bottom of slot varies.

The enclosure is stuffed with the loss material ($\epsilon_r=1, \sigma=0.003\text{S/m}$). The discharge location is location2.

There are three cases:

- Case1: Slot height = 20mm, $D_{\text{PCB}_S} = 3\text{mm}$
- Case2: Slot height = 10mm, $D_{\text{PCB}_S} = 8\text{mm}$
Changing the slot height and not changing the position of PCB.
- Case3: Slot height = 10mm, $D_{\text{PCB}_S} = 3\text{mm}$
Changing the slot height and moving up the PCB to keep the D_{PCB_S} invariable

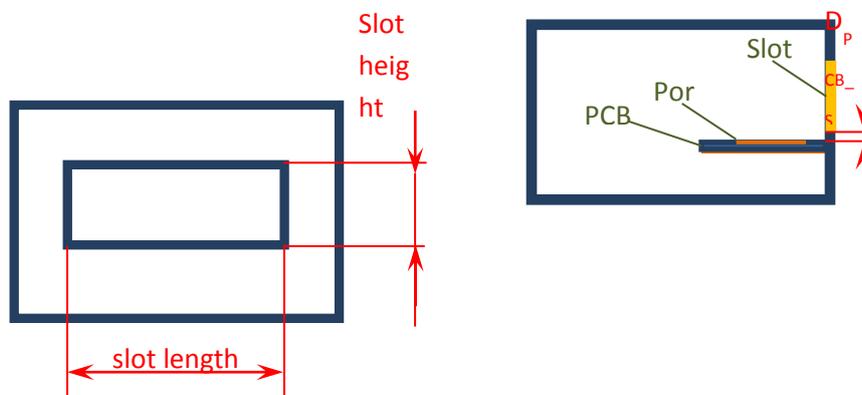


Figure 8.93. Slot height & PCB location

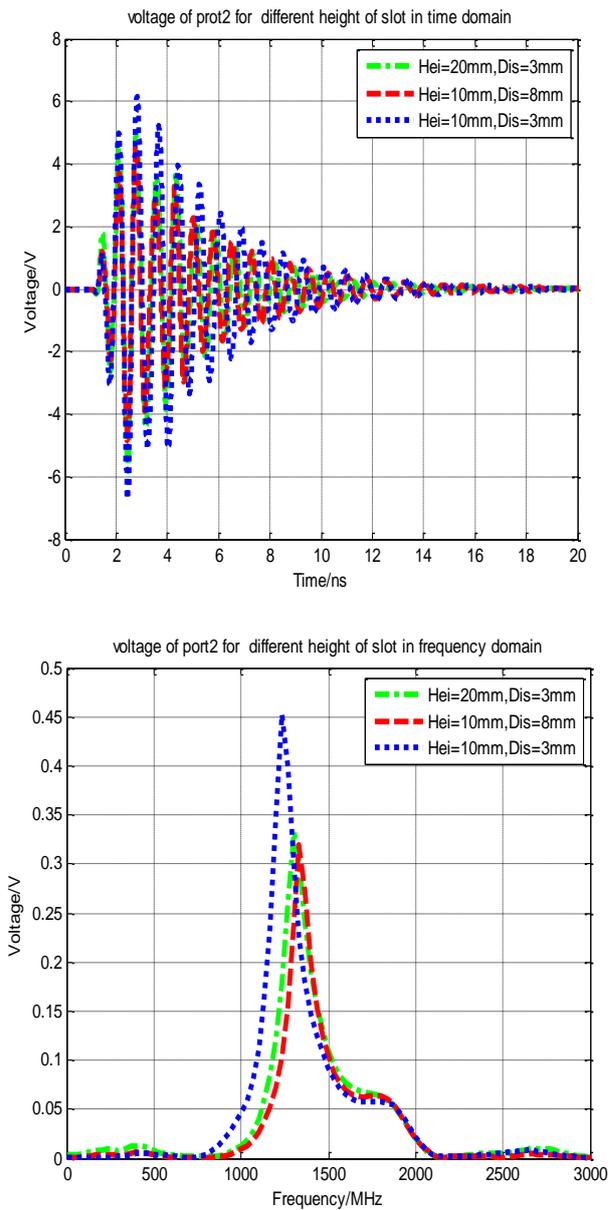


Figure 8.94: Voltage of port2 for different slot height & PCB location in time domain and in frequency domain

Slot length/mm	Slot width/mm	D_{PCB_S} /mm	V_{pp}/V	Resonant Frequency/ GHz	Magnitude at Resonant Frequency/V
80	20	3	10.796	1.300	0.3328
80	10	8	9.425	1.334	0.3196
80	10	3	12.836	1.233	0.4531

Table 8.20: Voltage of port2 for different slot height & PCB location

Note: V_{pp} is the peak-to-peak voltage in time domain in Figure 8.94. Resonant frequency is the frequency where the magnitude is maximum in frequency domain in Figure 8.94.

The PCB location has more effect on V_{pp} , resonant frequency and magnitude at resonant frequency than the slot height. Hence, the proper layout of PCB can reduce the coupling of PCB the interference from the discharging of ESD. The situation that the signal frequency is close to the resonant frequency should be avoided.

8.4.2.3 Effect of Slot Length

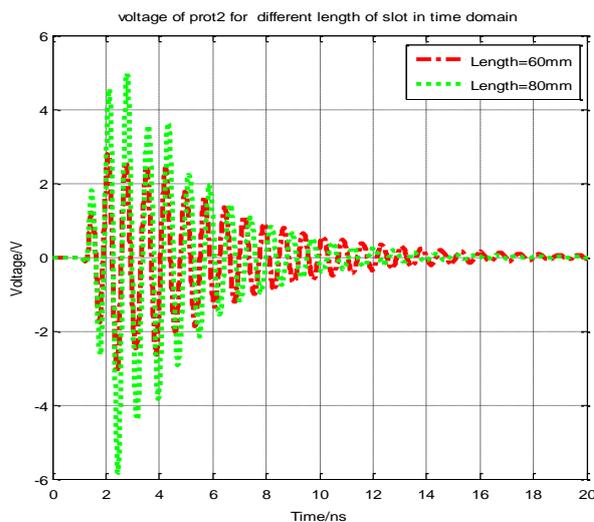
This is to find the effect of slot length on the coupling.

The enclosure is stuffed with the loss material ($\epsilon_r=1, \sigma=0.003S/m$). The discharge location is location2.

There are two cases as shown in Figure 8.93.

- Case1: length=80mm
- Case2: length=60mm

The condition and simulation results are listed in following.



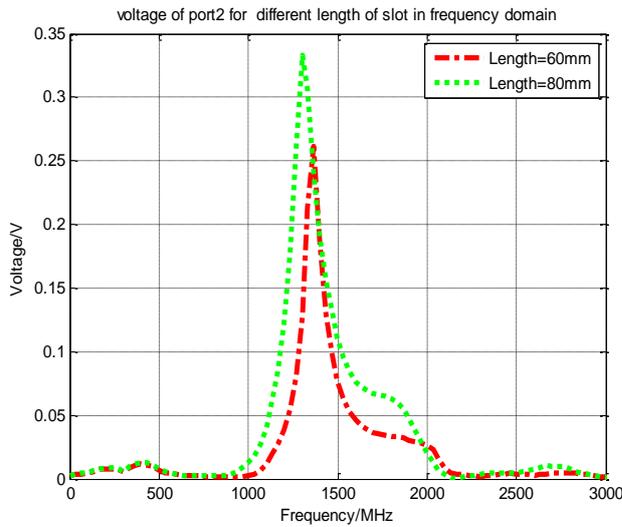


Figure 8.95: Voltage of port2 for different slot length in time domain and in frequency domain

Slot length /mm	Slot width /mm	V _{pp} /V	Resonant Frequency/GHz	Magnitude at Resonant Frequency/V
80	20	10.796	1.300	0.3328
60	20	5.899	1.367	0.2615

Table 8.21: Voltage of port2 for different slot length

Note: V_{pp} is the peak-to-peak voltage in time domain in Figure 8.95. Resonant frequency is the frequency where the magnitude is maximum in frequency domain in Figure 8.95.

Though there isn't much change of resonant frequency and magnitude at resonant frequency when slot length increases, V_{pp} increases obviously.

8.4.2.4 Effect of Enclosure Loading Material

The enclosure has been filled with a lossy material to reduce its Q-factor, as real enclosures normally do not have Q-factors above 50. This part of the investigations simulates different filling materials. The discharge location is location. The size of slot is 80mm×20mm.

Three different materials are compared.

- Case1: $\epsilon_r=1, \sigma=0S/m$
- Case2: $\epsilon_r=1, \sigma=0.003S/m$
- Case3: $\epsilon_r=2, \sigma=0S/m$

The condition and simulation results are listed below.

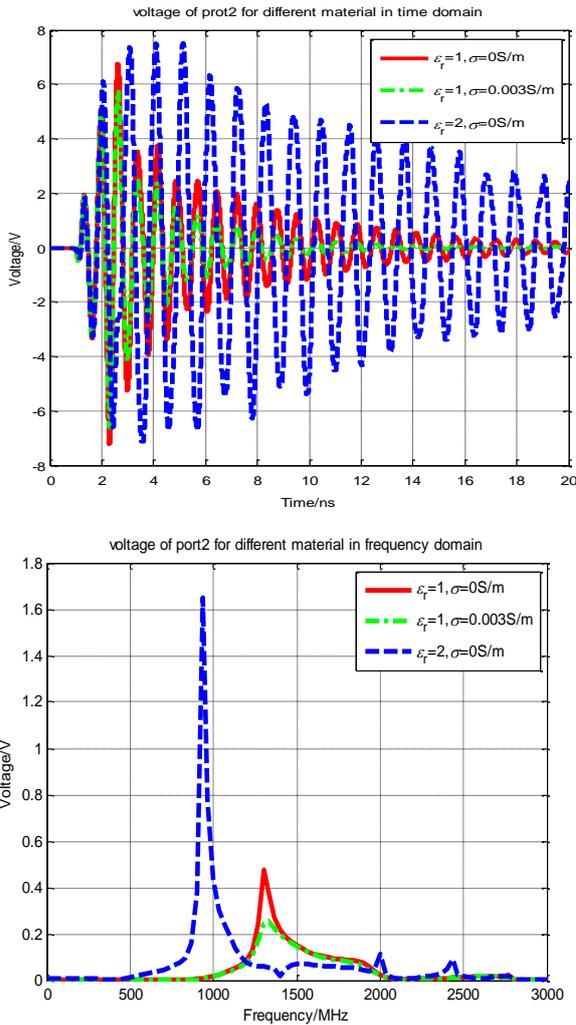


Figure 8.96 Voltage of port2 for different stuffed material in time domain and in frequency domain

Material stuffed	Vpp/V	Resonant Frequency/G Hz	Magnitude Resonant Frequency/V	at
$\epsilon_r=1, \sigma=0\text{ S/m}$	14.01	1.300	0.4751	
$\epsilon_r=1, \sigma=0.003\text{ S/m}$	12.30	1.334	0.2543	
$\epsilon_r=2, \sigma=0\text{ S/m}$	15.31	0.9335	1.649	

Table 8.22: Voltage of port2 for different stuffed material

The resonant frequency and magnitude at the resonant frequencies changes obviously with permittivity. The change in the resonance frequency ($\epsilon_r = 2$) again verifies that the enclosure resonances are dominating the coupling.

8.4.2.5 Effect of Different Enclosure Material

The effect of different enclosure material is simulated in this section. The discharge location is location1. The enclosure is empty, no filling material is used

There are four cases for enclosure material

- Case1: copper
- Case2: PEC
- Case3: conductive plastic ($\sigma=300S/m$)
- Case4: without enclosure

The condition and simulation results are listed in following.

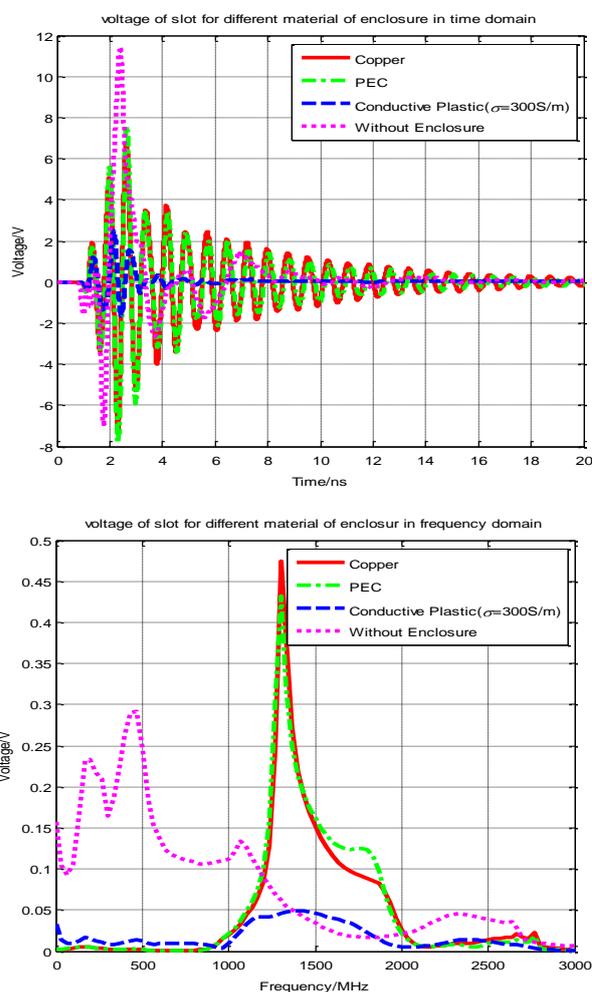


Figure 8.97 Voltage of port2 for different enclosure materials in time domain and in frequency domain

Enclosure material	V _{pp} /V	Resonant Frequency/GHz	Magnitude at Resonant Frequency/V
copper	12.30	1.30	0.4751
PEC	15.365	1.300	0.4323
conductive plastic	4.114	1.434	0.0488
without enclosure	18.359	0.4668	0.2913

Table 8.23: Voltage at port2 for different enclosure material

Removing the enclosure increases the induced voltage but not dramatically. The reason is that the Q-factor of the enclosure enhances the fields inside while shielding against fields at other frequencies. Consequently more low frequency components are seen if there is no enclosure and the spectrum of the induced voltage is more broadband. The difference between PEC and copper is small. In actual enclosures other content would de-Q the enclosure. If conductive plastic is used strong losses are introduced. The induced voltage has its lowest value as the Q-factor is strongly reduced, but the plastic enclosure still provides some shielding. Without enclosure the strongest signals are observed having energy concentrated around lower frequencies.

This set of simulations combined with other simulations that vary the dimensions of the enclosure can be summarized in the table below:

Factor	Effect on resonant Frequency			Effect on Coupling Amplitude		
	Obvious	some	little/ no	obvious	some	little/ no
With or without PCB	√			-	-	-
ϵ_r	√				√	
σ		√			√	
Discharging location			√	√		
Slot length		√		√		
Slot height			√	√		
PCB height location		√			√	
Enclosure length		√		√		
Enclosure width			√			√
Enclosure height		√		√		
Enclosure material	√			√		

Table 8.24 Coupling factor table

For system design we learn that resonances are a strong contributor to the ESD coupling, as the coupled voltage is dominated by resonances in the coupling path, and not by the spectral content of the ESD simulator's currents or fields.

8.5 ESD Field Coupling into Remote Key Antenna

Remote keyless entry (RKE) is a system designed to remotely permit or deny access to premises or automobiles. Its basic functionality is to enable user to remotely lock / unlock the doors from 10m to 20m distances. RKE typically consists of a Microcontroller, Transmitter and a printed circuit antenna. Its frequency of operation is 315MHz in USA & Japan and 433.92MHz in Europe. RKE printed circuit board (PCB) typically consists of a Microcontroller, Transmitter IC and a loop antenna. As RKE key fobs are handheld devices, the loop antenna is susceptible to ESD. Therefore, analyzing the impact of ESD on RKE system is critical to prevent the system from malfunctioning. Malfunctioning could be self-recovering, not being noticed by the user, to complete, permanent failure, or loss of stored information or to latch up which will drain the battery quickly. All but self-recovering errors must be considered serious.

The following sections detail the modeling and simulation of ESD on RKE PCB and also some protection schemes.

Objective is to analyze the Electromagnetic interference on the remote keyless entry PCB via simulation. The source of electromagnetic interference is either an ESD close to the key, or a direct ESD to the antenna. The simulation is performed using full wave simulation based on CST Microwave studio.

For the ESD directly to the antenna we assume that the plastic enclosure can be penetrated by an ESD usually at the interface of two plastic parts.

8.5.1 Modeling Approach and Steps Involved

The source is modeled by an ESD generator and the victim is modeled as a PCB, considering the relevant components of an RKE system like Transmitter IC's output stage, impedance matching network and the loop antenna.

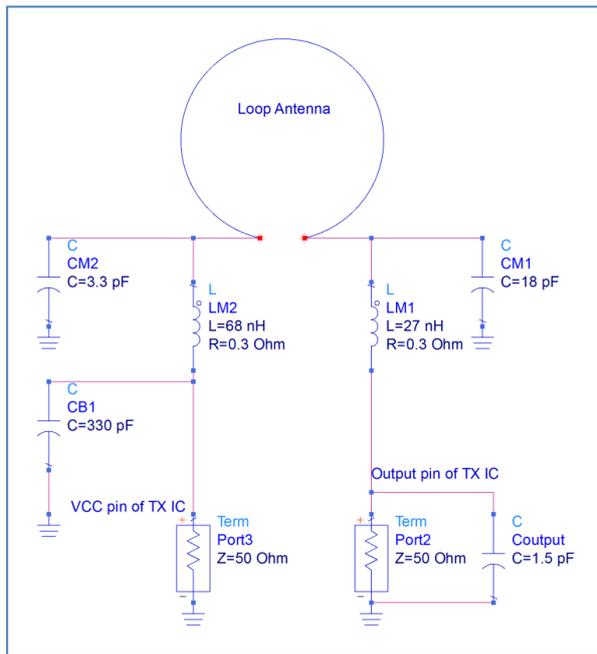
Following are the sub-tasks involved in modeling and simulation of RKE system

- Creation and verification of RKE PCB model that includes the modeling of the Printed circuit antenna, Transmitter IC output stage and the impedance matching network
- Integration of the ESD generator model into the above PCB model
- Simulation of direct discharge and field coupling scenarios to compute the voltage developed on the Transmitter IC output pins.

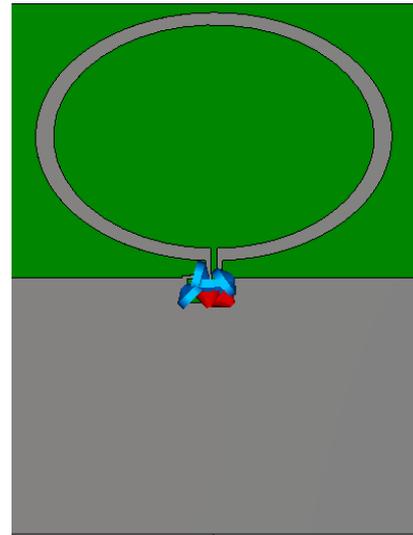
8.5.1.1 Modeling RKE PCB

Critical path for analyzing the impact of ESD on RKE is the path connecting the transmitter IC to the loop antenna. Thus, a simplified schematic that is shown in Figure 8.98(a) is used as the basis for creating a 3D model of the RKE PCB in CST. Figure 8.98 (b) shows 3D model.

PCB size is 37mm X 47mm made of lossy FR-4 ($\epsilon_r = 4.3$). All metal is selected to be PEC. All passive components are modeled as lumped elements. The ICs are not modeled directly, just the ESD input protection is modeled either as resistor or as diode.



(a)



(b)

Figure 8.98: Simplified schematic of an RKE PCB (a), 3D model of RKE PCB Simplified schematic and 3D model of RKE PCB (b)

8.5.1.2 Simulation Scenarios

There are two basic types of ESD scenarios, ‘*Direct discharge*’ and ‘*Field coupling from a nearby ESD*’. These are sub-divided further as shown in Figure 8.99.

In all the simulations, port 1 is the excitation port formed by the ESD generator’s discrete port. Ports 2 and 3 represent the two pins of the TX IC (shown in Figure 8.98 (a)) connecting the impedance matching network of the loop antenna.

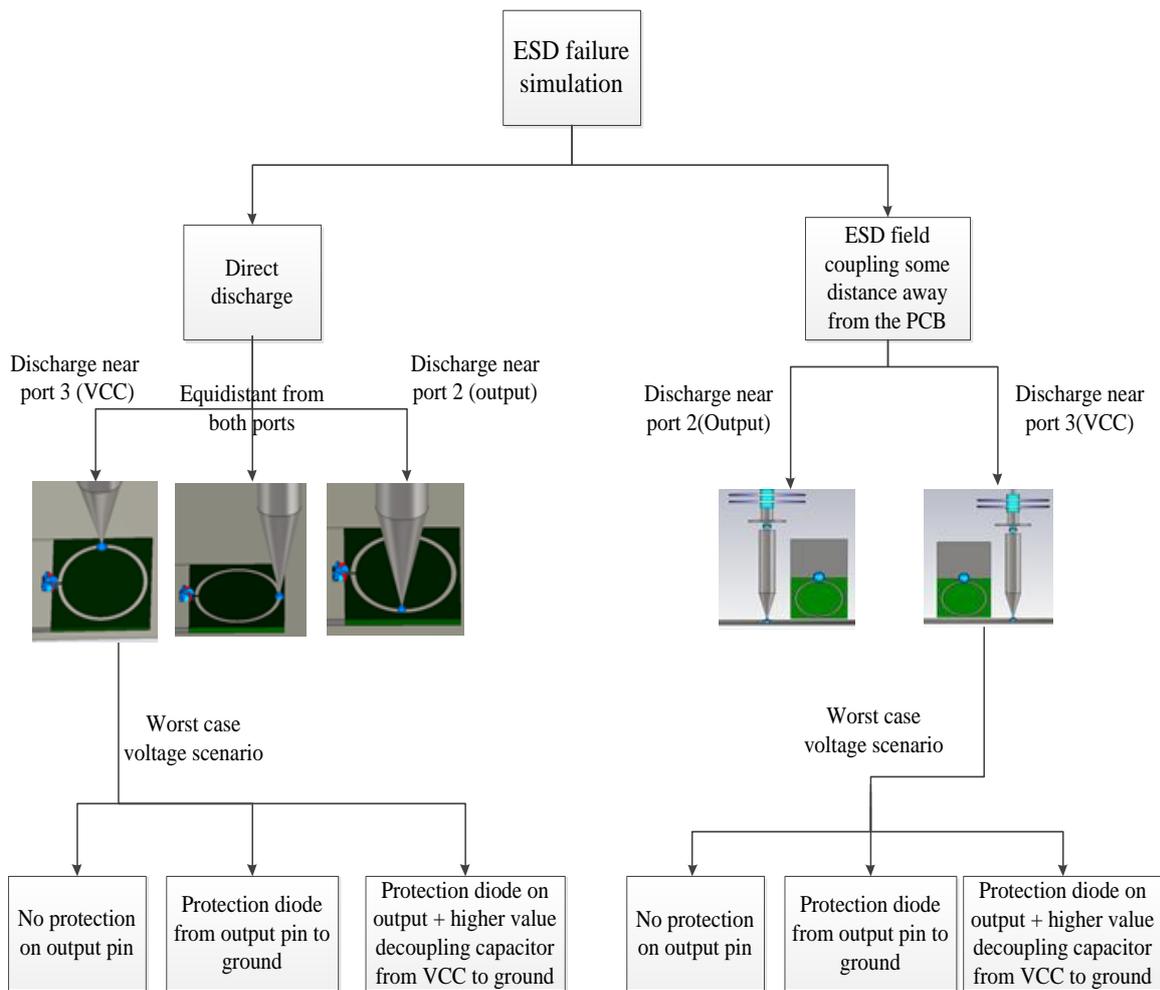


Figure 8.99: Simplified schematic and 3D model of RKE PCB

8.5.2 Simulation of Direct Discharge

Below are the simulation settings for this case. Figure 8.100 depicts this scenario.

- The remote key PCB is placed such that the tip of ESD generator is in contact with the loop antenna
- Port 1 is the discrete port of the ESD generator and also the excitation port
- Excitation source is a 10kV step and the duration is 20ns shown in Figure 8.101(a)
- Time domain solver is used and the frequency range is 30kHz to 3GHz
- Boundary conditions: open on all sides and $E_T = 0$ below the ground plane

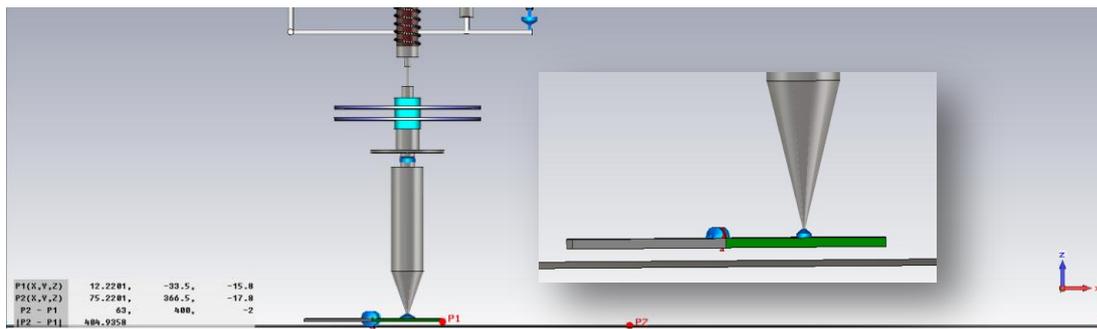


Figure 8.100: Direct discharge to the PCB loop antenna

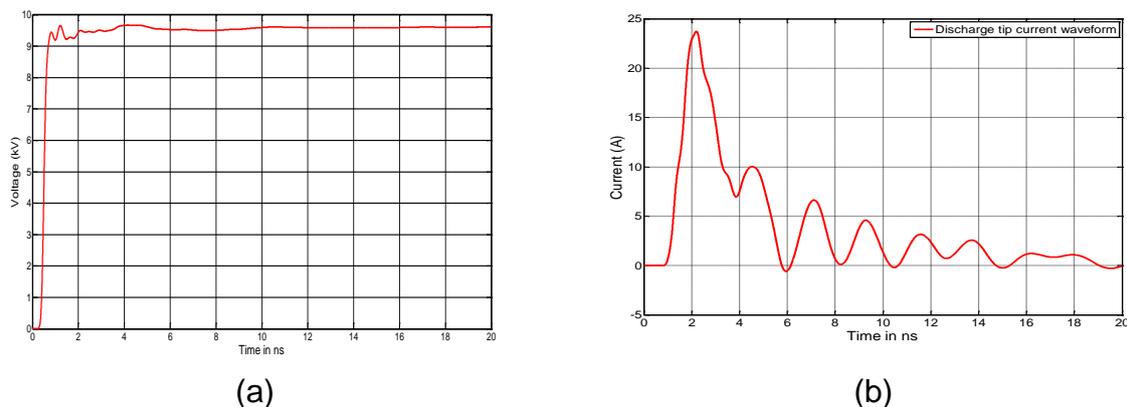


Figure 8.101: ESD generator excitation voltage (a) and discharge tip current (b) waveforms

8.5.2.1 Comparison of Voltages on TX IC with and without ESD Protection

A test voltage of 10kV was selected throughout this study. The rise time of the generator is set to 0.85ns, thus, a contact mode ESD has been simulated. If for example a 25kV air discharge would take place the peak current into a large ground plane would be larger, however, the rise time would be slower. As most of the coupling processes in this key are current derivative driven we would not expect drastical differences between a 10kV 0.85ns ESD and a 25kV 3n ESD. Due to the difficulty of modeling the air discharge we opted to use 10kV as it provides a good insight into the dominating dependencies.

Upon direct ESD to the antenna, voltages on output and VCC pins of TX IC rise close to 400V and -50V respectively. Hence, output and VCC pins of the IC need protection.

One way to achieve output pin protection is by connecting an ESD protection diode from output pin to ground. In simulation this was modeled as a 1Ω resistor to ground.

Figure 8.102 shows the related results. The blue curve is a hypothetical result: If the input would just be a small capacitance and 50 ohm a voltage of -400 V would be induced by a 10kV direct discharge to the loop. In reality, the internal ESD protection would forward bias and provide different impedance. This impedance is modeled as 1 Ohm in this simulation. Later simulation uses a diode model. Even with 1 Ohm the

voltage reaches 15V (green – subplot), thus 15A which is likely to destroy or latch up most ICs. For the VCC pin, the decoupling capacitance that is already present has been increased in its value to verify the reduction of the voltage at VCC. Figure 8.103 shows this result.

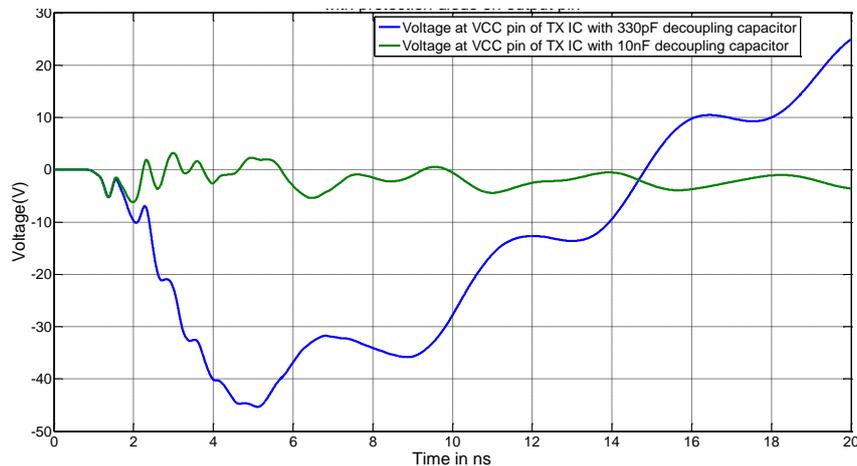


Figure 8.102: Comparison of output pin voltage with and without 1Ω resistor to ground

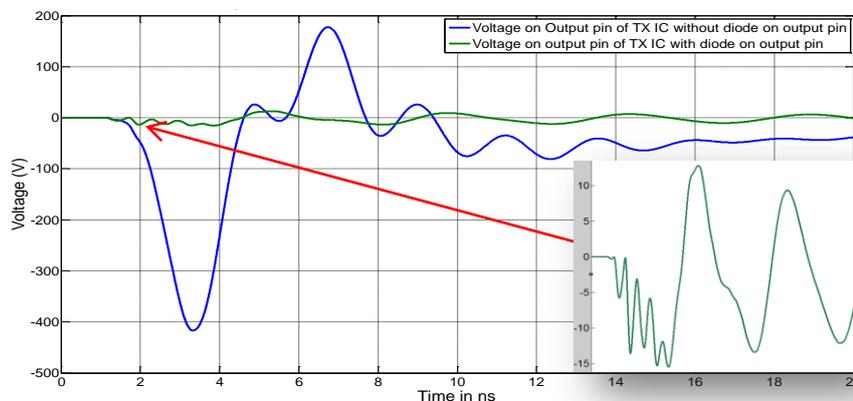


Figure 8.103: Comparison of voltage on VCC pin of TX IC with 330pF and 10nF decoupling caps

Figure 8.102 clearly shows that a 1Ω to ground (equivalent of an ESD protection diode above break down voltage) helps in reducing the voltage on the output pin of the TX IC to -15V but this might still be sufficient to upset the IC and further analysis needs to be done to predict if this would cause soft errors or hard errors or both. Based on this analysis the decision of further levels of protection can be taken.

Similarly, Figure 8.103 indicates that increasing the decoupling capacitor value helps in limiting the voltage rise on the VCC pin of TX IC due to direct discharge. However, the noise voltage at the VCC is still very large: +/- a few volt which will certainly upset

the key, and depending on the key circuitry might lead to loss of memory, latch up or other unwanted behavior. A 10kV direct discharge to the antenna has a high probability to disturb or even damage the IC. Detailed simulations would need to take the specific IC used into account and would need a soft error model for this IC which relates noise voltage to latch up, loss of memory or self- recovering errors.

8.5.3 Simulation of Field Coupling

For field coupling a discharge to a metallic plate close to the key is assumed.

- RKE PCB is placed such that the tip of the ESD generator is 1.5 cm away
- ESD generator tip touches ground plane of the generator and RKE PCB is 2mm above this ground plane
- Excitation signal on the port1 (ESD generator) is shown in Figure 8.105 (a)
- Time domain solver is used and the frequency range is 30kHz to 3GHz
- Boundary conditions: open on all sides and $E_T = 0$ below the ground plane

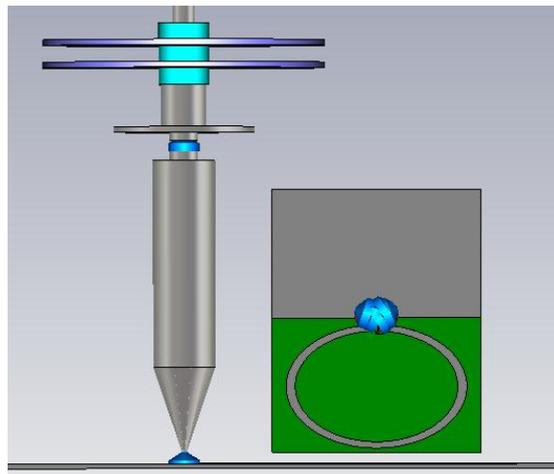


Figure 8.104: Simulation setup for field coupling on RKE PCB from ESD 1.5cm away

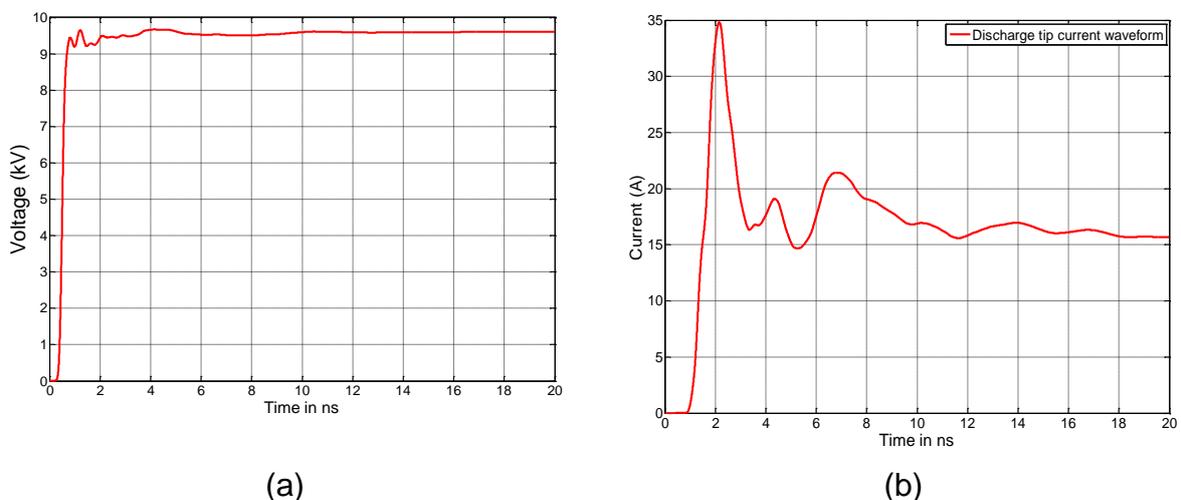


Figure 8.105: ESD generator excitation voltage (a) and discharge tip current (b) waveforms

8.5.3.1 Comparison of Voltages on the TX IC with and without ESD Protection

Due to field coupling from an ESD to ground 1.5 cm away from the RKE PCB, voltages on output and VCC pins of TX IC reach close to 45V and -8V respectively (if no protection is present). Hence output pin needs protection and VCC may or may not need a protection in this case. One of the ways in which output pin protection can be achieved is by connecting an ESD protection diode from output pin to ground. In simulation this was modeled as a 1Ω resistor to ground. Figure 8.106 shows the related results.

For the VCC pin, the decoupling capacitance that is already present has been increased to check if that helps in reducing the voltage rise on VCC. Figure 8.107 shows this result.

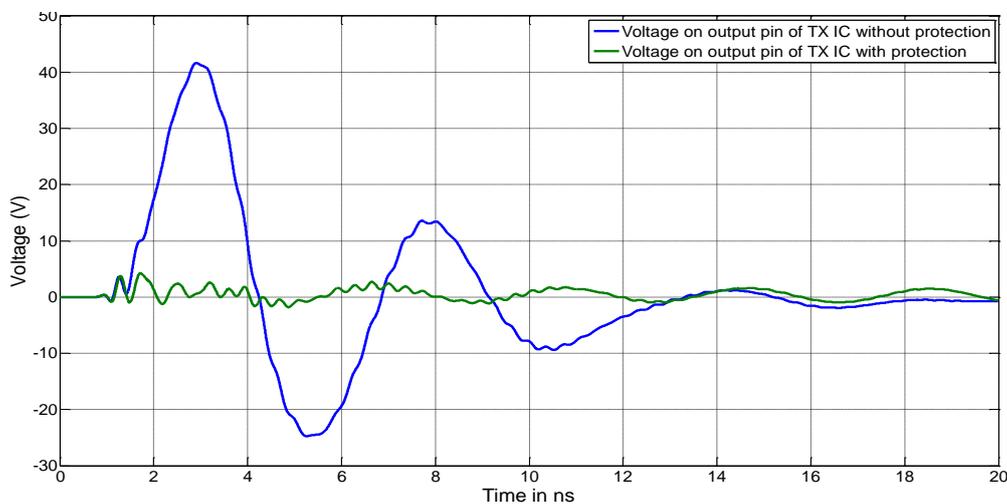


Figure 8.106: Comparison of voltage on the output pin of the TX IC with and without 1Ω to ground

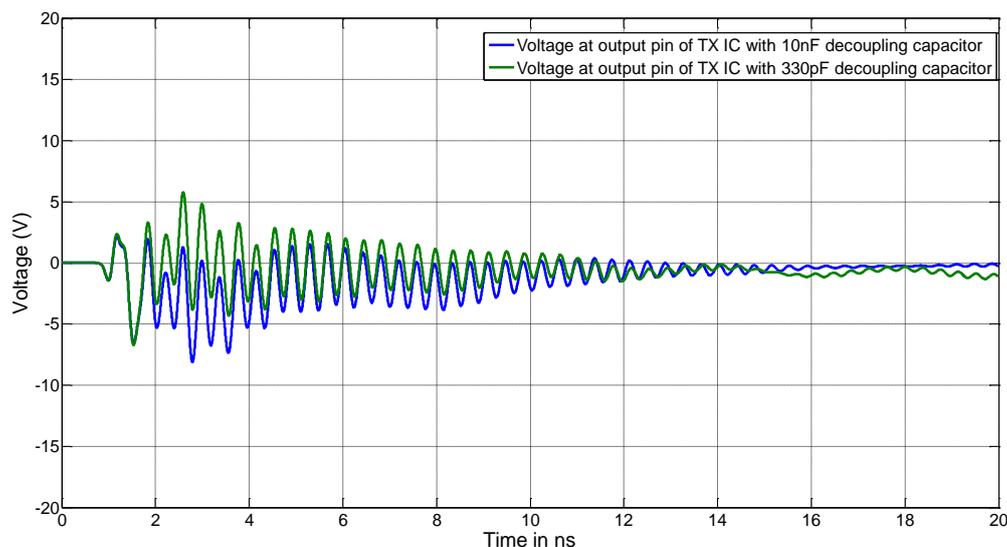


Figure 8.107: Simulation setup for field coupling on the RKE PCB from ESD 1.5cm away

Figure 8.106 shows that a $1\ \Omega$ to ground (equivalent of an ESD protection diode above break down voltage) helps in reducing the voltage on the output pin of the TX IC to less than 6 V. As per Figure 8.107 it can be inferred that increasing the decoupling capacitance value helped in limiting the voltage rise on VCC pin due to field coupling is limited to within ± 6 V. But a fluctuation on VDD pin level might cause soft/hard errors. Further investigation is required to estimate the nature of the errors.

8.5.3.2 SPICE Simulation of Additional External Protection

As discussed in section 1.4.1, internal IC protection ($1\ \Omega$ to ground) was not sufficient enough to limit the voltage on the output pin to desired level. So, an additional external ESD protection can be used between the loop antenna input and the matching inductance coming from output pin. This has been analyzed using SPICE simulation. Two different ESD protection diode models are used. In the previous simulations we used 1 Ohm as slope resistance equivalence for the input protection of the IC (internal). The value of 1 Ohm is kind of low. We increased it to 5 Ohm, but added an external ESD protection having 1 Ohm slope resistance. Both protections are decoupled by the tuning inductance of 27 nH. As shown below, this allows to protect the input against the field coupled ESD very well. Figure 8.108 shows SPICE simulation circuit that simulates the ESD current at a distance of 1.5 cm with additional ESD protection.

The coupling at 1.5 cm has been simulated by adding an appropriate mutual inductance ($M=3.3\ \text{nH}$) between the ESD current source and the loop antenna. Here we assume a pure magnetic coupling between the loop antenna and the ESD discharge current path.

rise time). These values can be used to test if direct coupling to the IC (not to the PCB or the antenna, but to the lead frame and die of the IC directly) is likely to cause an upset. As reference data measured on VLSI ICs is used. The data indicates that there is a significant chance of direct coupling to the IC with upset as consequence. This indicates that the ICs used in remote key entry system need to be investigated for their soft error or latch up response with respect to transient fields.

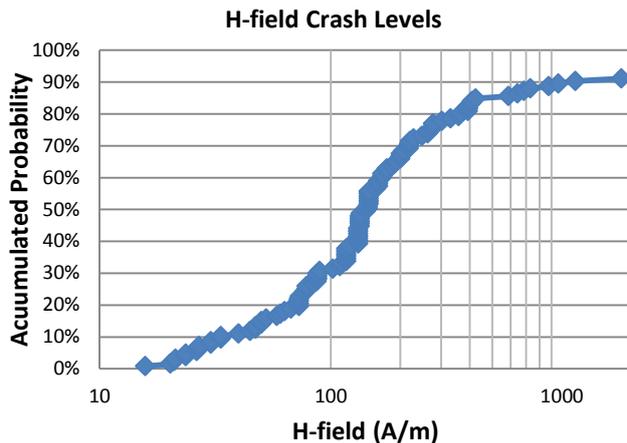


Figure 8.110: H-field crash levels

Upset probability of VLSI ICs for direct ESD coupling to the IC and its lead frame as a function of magnetic field derived from testing using 500 ps rise time single transient field pulses.

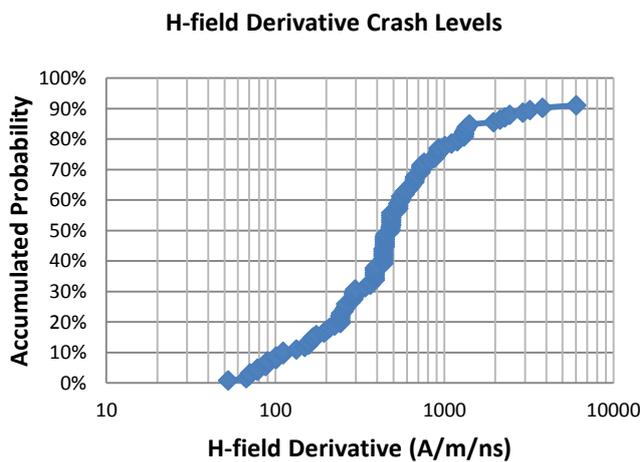


Figure 8.111: H-field derivative crash levels

Upset probability of VLSI ICs for direct ESD coupling to the IC and its lead frame as a function of magnetic field time derivative derived from testing using 500 ps rise time single transient field pulses.

8.5.4 Conclusion

- A remote key PCB 3D model has been created and verified
- An ESD generator model has been integrated with the RKE PCB model and full wave simulations were performed to estimate the voltages developed on the output and VCC pin (port 2 and port3)
- Direct ESD to the antenna is pretty severe in terms of causing high voltages on the TX IC pins. Including an assumed 1 Ohm like IC internal ESD protection the peak voltage on output pin is still as much as -15V and this might cause the IC to malfunction or be damaged. Further levels of protection are needed in this case.
- Also, during direct ESD to the antenna the VDD voltage fluctuates around $\pm 6V$. This is likely to lead to upset of the ICs
- Field coupling to the antenna is relatively less severe but is still enough to upset the IC. An additional level of protection at the input point of the antenna proved to be useful in this case.
- Coupling can occur to the antenna, to loops or surface traces on the PCB and to the lead frame and the die of the IC directly. The field strengths of a 10kV nearby ESD are strong enough to upset ICs by direct coupling to the IC. In this case no PCB based methods will prevent the upset, it is suggested to determine the soft-failure response of the ICs used to transient field coupling for example by susceptibility near field scanning.

8.6 Charging Effects due to Electrostatic Induction

8.6.1 Triboelectric Effect and Electrostatic Induction

Positive and negative charge on a device are separated by the approach of a second charged object because of electrostatic induction. Triboelectric charging of both, conducting and dielectric objects can very likely take place in automotive environment. Production, servicing and usage of a vehicle are affected. Automotive parts may be charged due to:

- friction as a result of vibration during transport,
- friction as a result of vibration when driving,
- cleaning and polishing,
- packaging,
- unpacking and removing of protection foils
- etc.

If dielectric objects like window, housing, decor elements etc. are charged, an electrical field is generated. The field decays very slowly and adjacent conducting parts like PCBs or integrated window antennas may be charged due to electrostatic induction. A subsequent discharge through sensitive electronics is possible.

8.6.2 Case Study - Polishing of Window

In a modern vehicle antennas are integrated often in rear or side windows. When polishing the window on the outside it may become electrostatic charged and induces voltage in antenna structures, placed inside the window. A subsequent ESD pulse in connected amplifier may cause a failure. Figure 8.112 shows the test window.



Figure 8.112: Side window with integrated antenna structures

The electric voltage after manual polishing is measured with a field mill under environmental conditions of 20°C and a relative humidity of 35 %. The voltage is acquired between the antenna structure and HCP. Triboelectric effect is enhanced using of styrofoam as a polishing material. Values about 1 kV could be observed.

Capacities of antenna structures are measured with RLC bridge. Capacitor is located between the antenna structure and the charged surface on the window outside. To be able to measure the structure the window outside is covered with aluminum foil. Table 8.25 shows the results. A maximal value of 45 pF could be measured.

Structure	Capacity [pF]
Antenna 1	18
Antenna 2	45

Table 8.25: Measured capacity of the window antenna

The maximum energy to be stored by a 45 pF capacitor for 1 kV is 22.5 μJ. A μC XC864 Data pin characterized in section 7.6 has a critical energy of 12.3 μJ for 100 ns TLP pulse. A failure of the IC is very likely. A potential threat is evaluated in simulation.

Two critical scenarios are possible:

- Charged antenna is plugged to the connecting cable (Figure 8.113 a)
- An IEC discharge occur on already connected antenna (Figure 8.113 b)

Antenna structure is modeled as a capacitor. Parasitics are modeled by equivalent serial 1 Ω resistor and 5 nH inductor. XC864 Data pin is used as a representative for antenna amplifier input. Connection is given by a lossless 5 m coaxial cable with 50 Ω characteristic impedance.

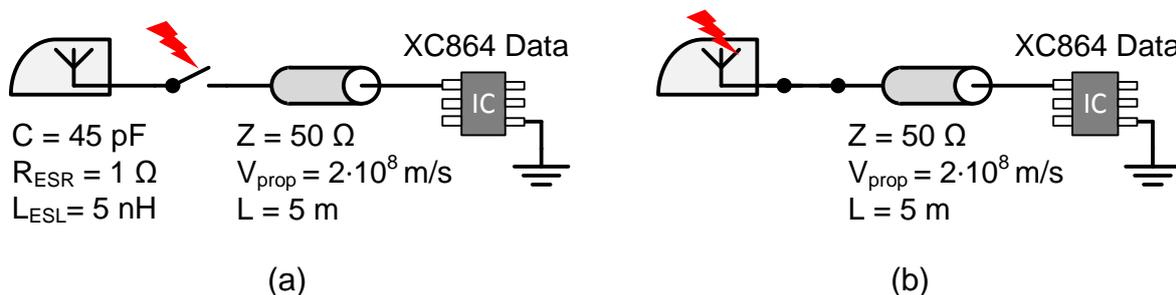


Figure 8.113: Simulation setup for antenna discharge (a), IEC discharge in antenna

Simulated voltage and current at XC864 Data pin are compared in Figure 8.114 and Figure 8.115. The reflections on the transmission line cause repeated voltage and current peaks. Cable length of 5 m results in relatively long time delay between two consecutive peaks. Only for the first few hundreds of nanoseconds the IC is adiabatic, later the heat dissipation increases. Therefore it is assumed only the energy absorbed in first 200 ns is relevant. Simulated voltage peak of the antenna discharge is 880 V, of the IEC discharge only 67 V. This high difference results because of the low serial resistance of the antenna structure. Current peak of the IEC discharge is followed by a characteristic plateau, where the most of the energy is transported to the IC.

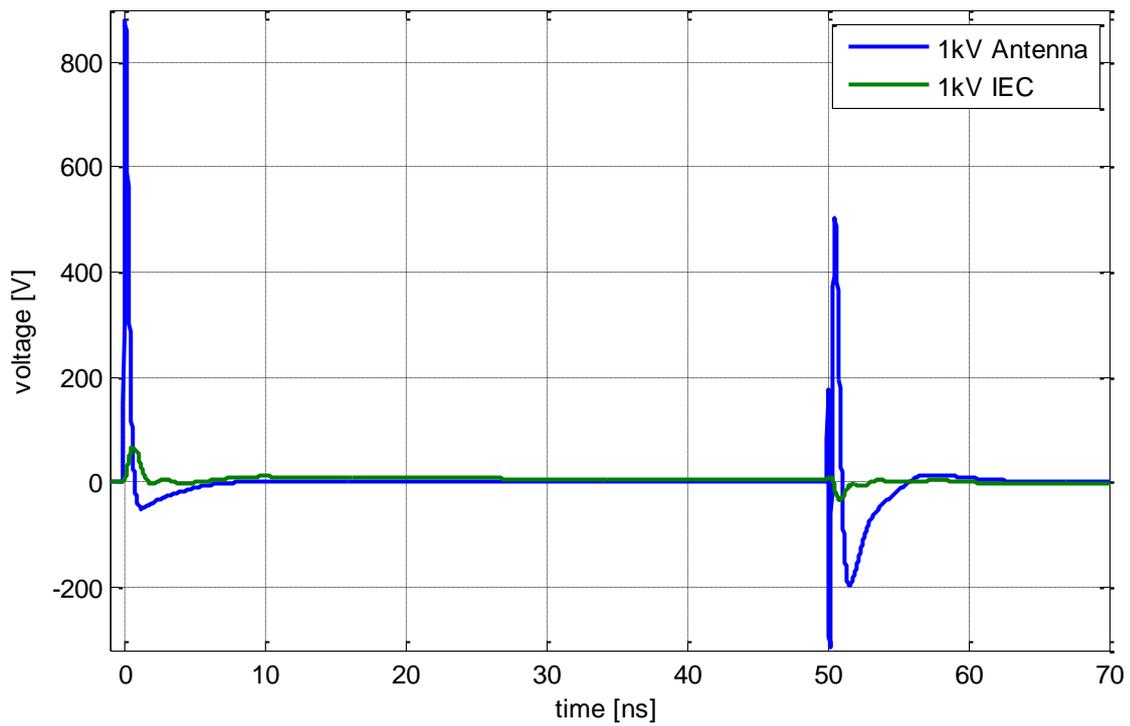


Figure 8.114: Comparison of simulated voltage at μC XC864

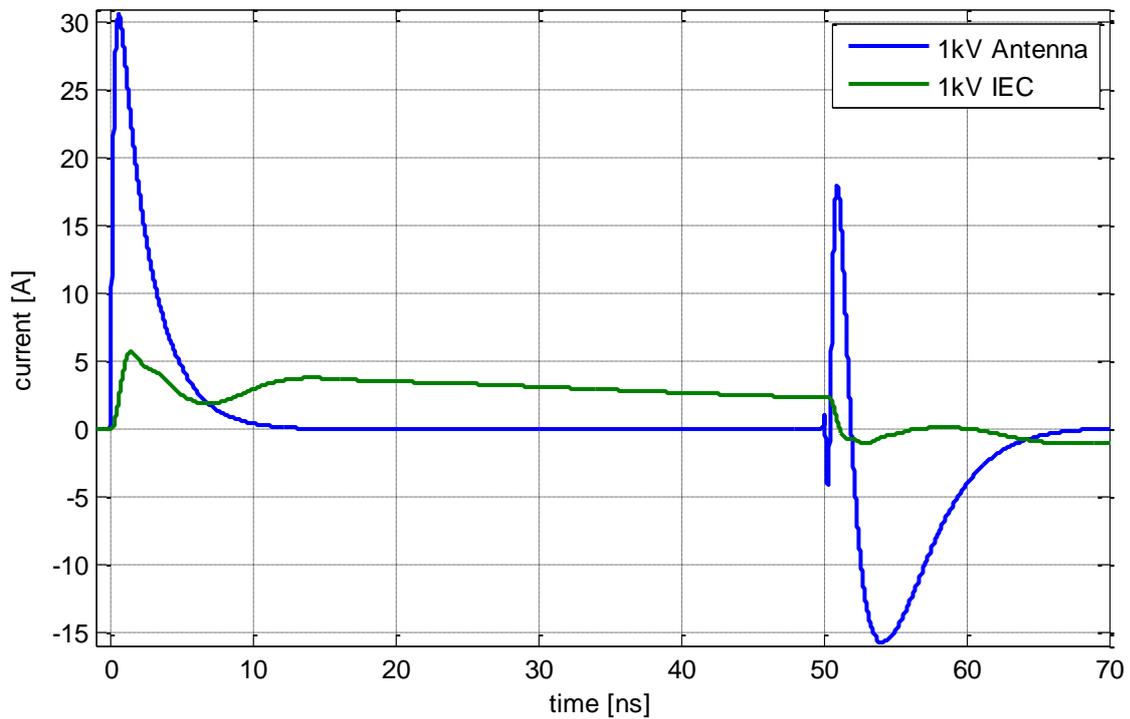


Figure 8.115: Comparison of simulated current at μC XC864

All simulated amplitudes are listed in Table 8.26. Additionally a safety factor is assigned to each energy value, as the reference value a critical energy 12.3 μJ of the

µC XC864 pin is used. No IC failure could be detected in simulation, but computed levels are not far away from failure levels.

ESD source	V _{charge} [kV]	V _{max} [V]	I _{max} [A]	E _{200ns} [µJ]	E _{crit} / E _{200ns}
Antenna	1	880	30.5	7.87	1.56
IEC	1	67	5.5	1.44	8.54

Table 8.26: Simulated amplitudes for XC864 Data pin

8.6.3 Case Study LED Rear Light

The combination of a dielectric close to a floating conducting plane can cause ESD. FAT members provided an LED rear light which shows malfunction due to electrostatic induction. Constructional details of the investigated device were already modified to prevent failure due to ESD when removing a protection foil from the front plastic plane.

Figure 8.116 shows separate parts of the device. It consists of plastic cover, reflector and PCBs. The reflector is made from chromed plastic. A connection between the conducting chrome layer and the PCB ground could not be measured. LEDs and other electronic components are distributed over two PCBs.



Figure 8.116: Exploded view of the LED rear light

ESD often occurs if the charge is kept by a charged device for a long time. The decay time of charge on the rear light is measured in the laboratory under environmental conditions of 20°C and a relative humidity of 35 %. The plastic cover is placed on a Styrofoam block for better isolation. The rear light can be charged using an ESD generator as voltage source. The source is discharged about 100 times on the plastic surface with a charging voltage setting of 15 kV. After charging the electric field

strength is measured using a field mill. In Figure 8.117 the measurement results are shown. Dissipation of charge is very slow. After 60 minutes still 4 kV can be measured, which is 40 % of the initial value.

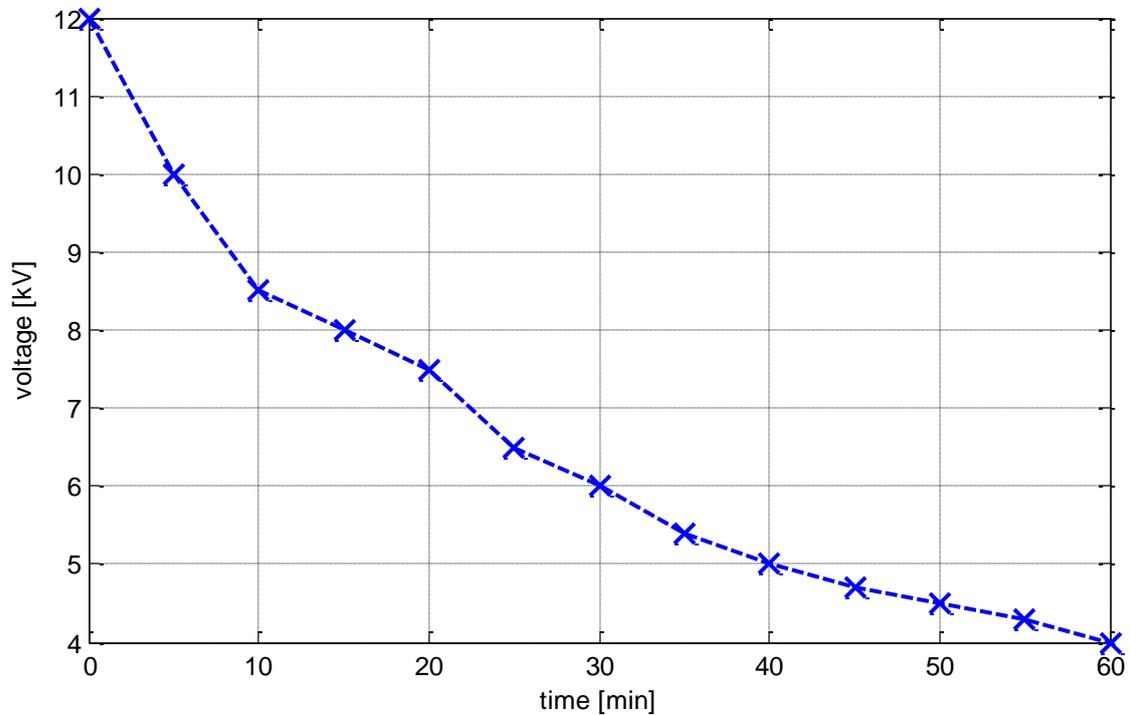


Figure 8.117: Dissipation of charge

Considering a charged plastic cover and the physical structure of the LED rear light there are two scenarios for ESD. A sketch of both ESD triggering mechanisms is shown in Figure 8.118.

ESD can occur if a charged device is plugged to the cable harness. The electrical charge is concentrated on the surface of the plastic cover. Due to electrical induction and good conducting properties of the reflector and the PCB, charge carriers are separated on top and bottom side of the components. Potential difference between PCB and ground is dissipated when plugging to the cable harness. This mechanism will be called *plugging*.

If the device is already installed in a vehicle and the plastic cover is charged, ESD can occur between the chromed reflector and the PCB. The potential difference is dissipated when V_0 exceeds a sparking voltage. The spark gap in air can be estimated by a rule of thumb with 3 kV per 1 mm. This mechanism will be called *internal sparking*.

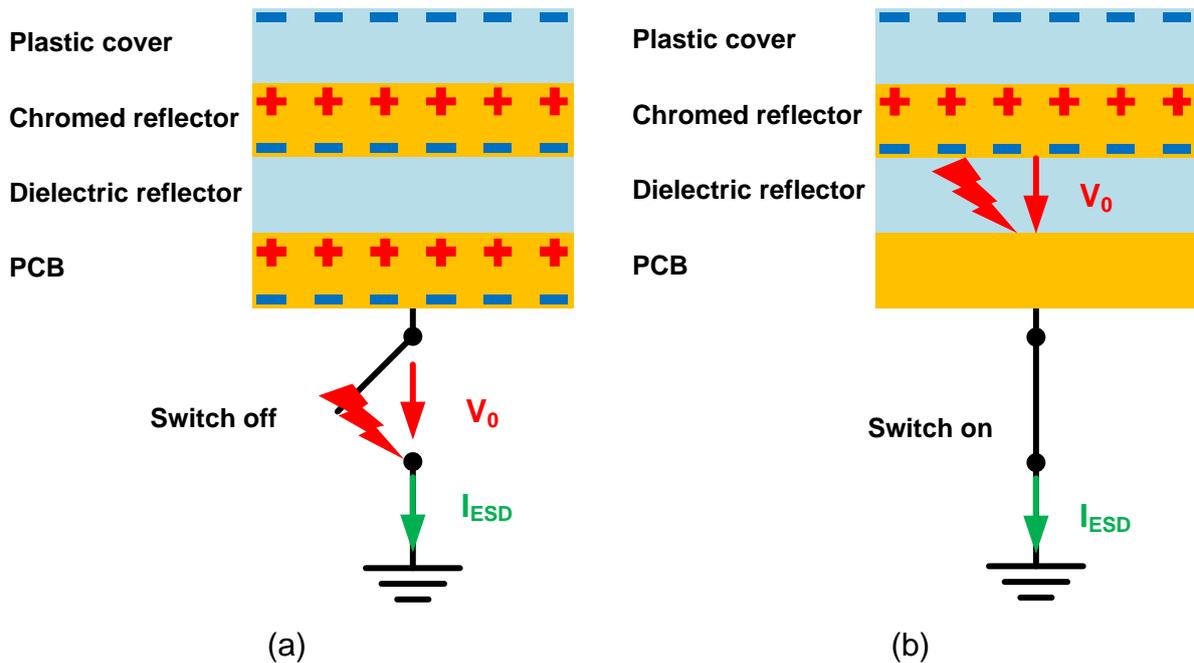


Figure 8.118: Discharge mechanism when *plugging* (a), when *internal sparking* (b)

In the measurement setup the plastic cover is charged using an ESD generator and ESD current through wiring harness is measured with a Fisher F65 current probe with specified bandwidth of 10 kHz to 1 GHz. The charging voltage level of the device surface is acquired using a field mill. In the *Plugging* setup the wiring harness is shorted manually to the HCP. Then *internal sparking* is triggered after sufficient charge was brought on the plastic cover with the ESD generator. Figure 8.119 shows the measured current shapes.

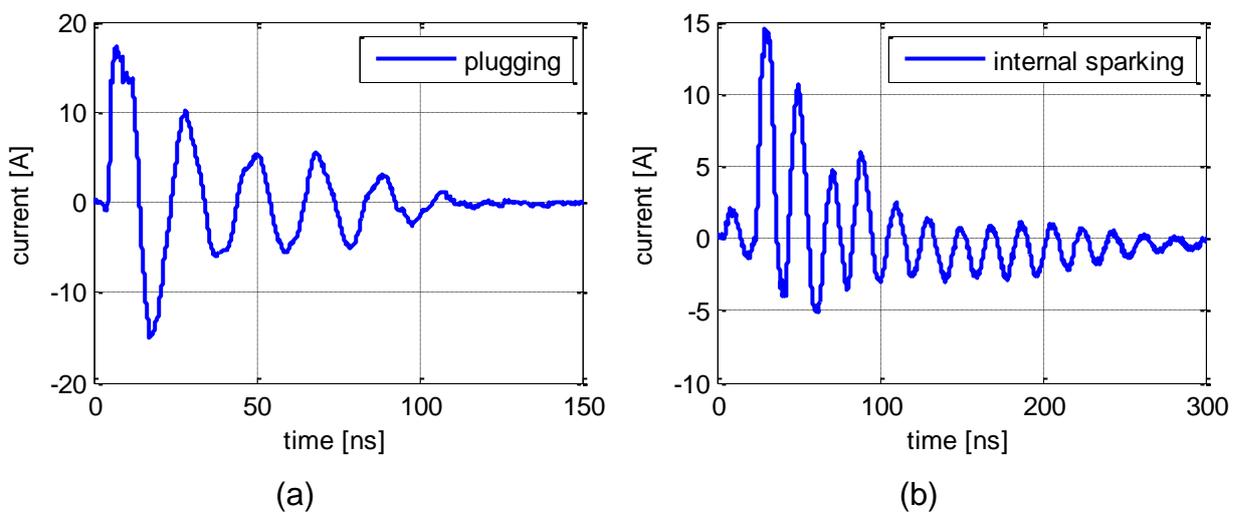


Figure 8.119: Measured current when plugging (a), internal sparking (b)

Amplitudes up to 15 A were observed. Both shapes have identical oscillation period of about 10 ns. The decay time after *internal sparking* is longer than for *Plugging*. The reproducibility of the waveform of internal sparking is low. Waveforms measured for plugging are stable. Short decay time indicates a low serial discharge resistance.

8.6.4 Demonstrator for Electrostatic Induction

A demonstrator is designed to reproduce the effect and verify considerations presented in the previous section.

Figure 8.120 illustrates the demonstrator manufactured in a rectangular form. The charged dielectric surface consists of a plastic foil placed on a paperboard (dielectric 1). The paperboard has a similar relative permittivity as air. The chromed plastic of the rear light is represented by a second paperboard (dielectric 2) covered by aluminum foil. A copper plate is used as the PCB. For the analysis of different current waveforms short wires with serial resistors are soldered to the copper plate. All dimensions are listed in Table 8.27.

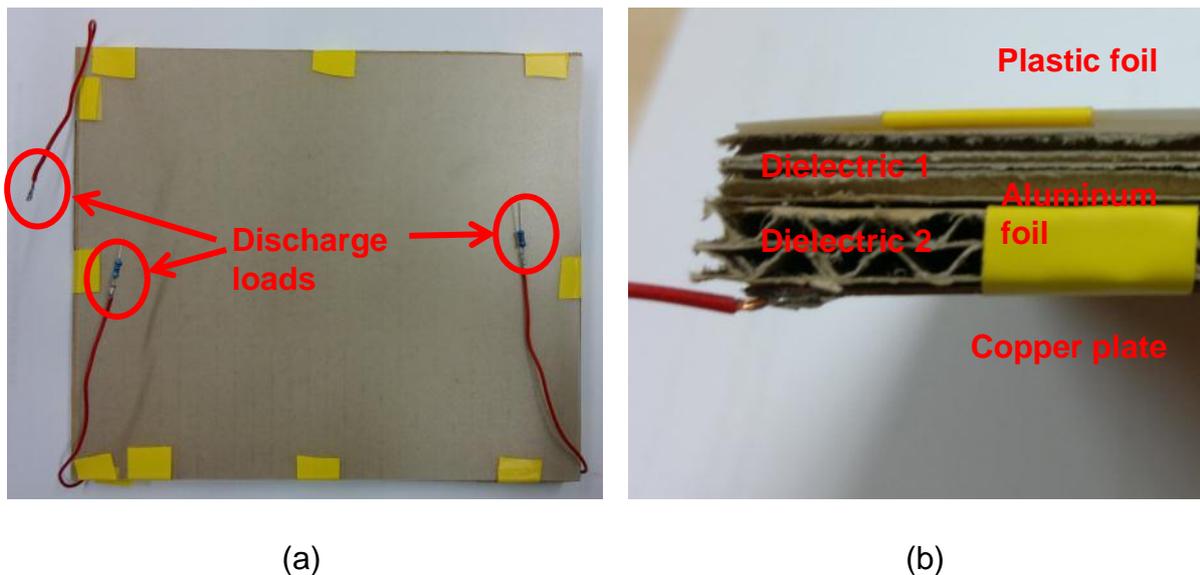


Figure 8.120: Demonstrator for electrical induction, top view (a), side view (b)

Property	Value
Surface area	150x170 mm
Dielectric 1 intensity	5 mm
Dielectric 2 intensity	5 mm
Connecting wire	100 mm
Discharge loads	0 Ω/ 50 Ω/ 1000 Ω

Table 8.27: Demonstrator dimensions

For the analysis *Plugging* waveforms are considered for reproducibility reasons. The plastic foil is charged by 100 discharges of an ESD generator distributed over the surface. Between consecutive tests, plastic foil is contacted for several minutes to the HCP to ensure a neutral state of the demonstrator at the beginning of each test. In Figure 8.121 results obtained with demonstrator are compared to current shapes measured with LED rear light.

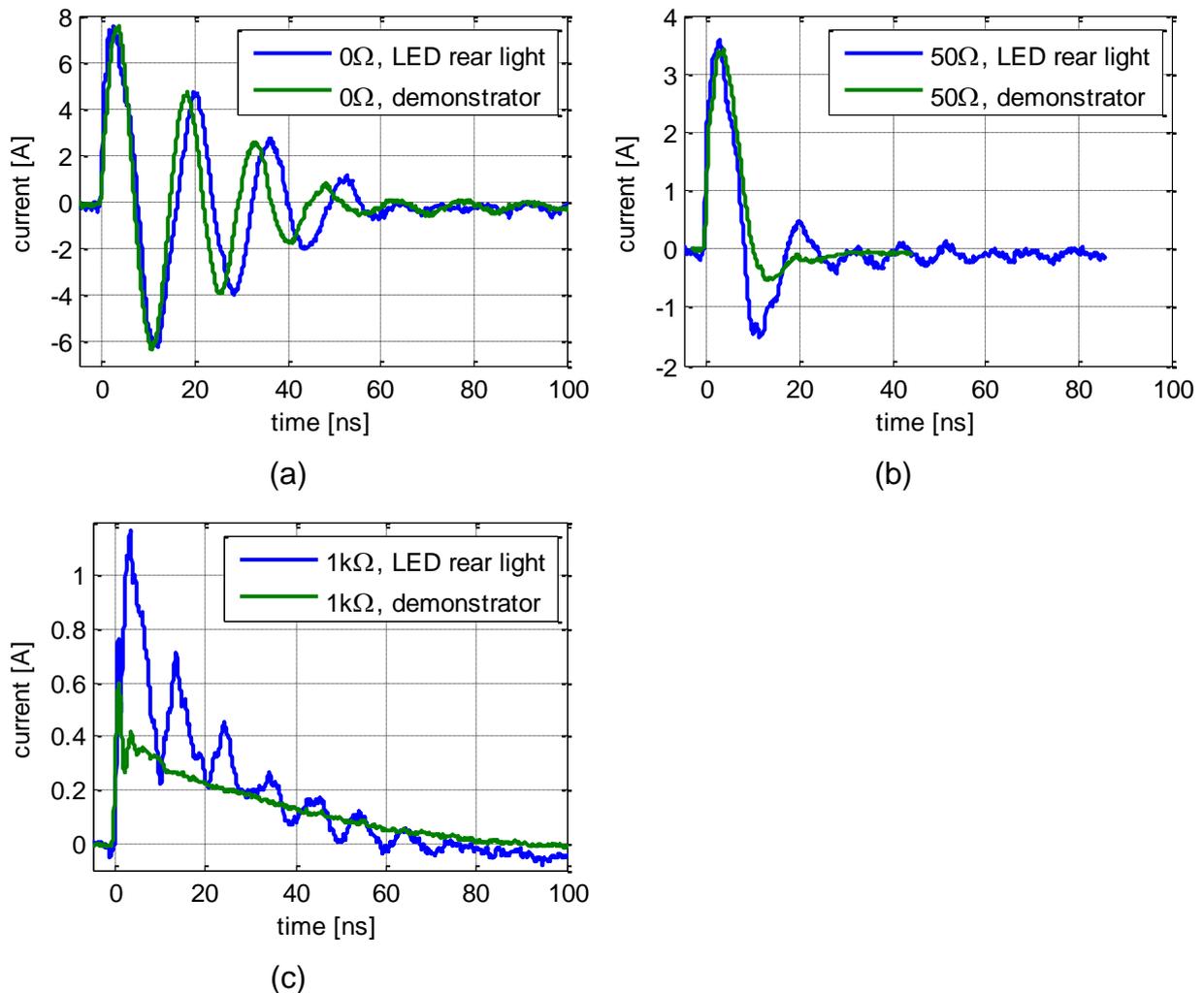


Figure 8.121: Current measurement for demonstrator $V_{\text{charge}}=1.7 \text{ kV}$ and for LED rear light $V_{\text{charge}}=15 \text{ kV}$ on $0 \text{ } \Omega$ (a), $50 \text{ } \Omega$ (b) and $1 \text{ k}\Omega$ (c)

Similar amplitudes were measured for charged demonstrator with 1.7 kV and 15 kV in case of the LED light (see Table 8.28).

Load	Demonstrator			LED rear light		
	V _{charge} [kV]	V _{FM} [kV]	I _{max} [A]	V _{charge} [kV]	V _{FM} [kV]	I _{max} [A]
0 Ω	1.7	0.85	7.5	15	10	7.5
50 Ω	1.7	0.7	3.4	15	10	3.6
1 kΩ	1.7	0.85	0.6	15	12	1.15

Table 8.28: Measured amplitudes on different loads for demonstrator and LED rear light

All waveforms can be reproduced well by the demonstrator. The difference between the charging voltages can be explained by different dielectric constants and dimensions of demonstrator and LED device. Current amplitudes are overlaid by an oscillation in LED rear light measurements.

The effect of electrostatic induction can be modeled by a capacitor. In particular two parallel plate capacitors switched in series are suitable as a model for demonstrator representing the different components inside the LED rear light. One capacitor exists between the charged plastic foil as a dielectric electrode and the aluminum foil. The second capacitor is distributed between aluminum foil and copper plate. Charging voltage of the plastic foil is equally divided between the two capacitors, due to identical paperboard intensity. Thus only one capacitor, charged to the half of the voltage measured on the plastic foil, has to be considered in the simulation model. The capacitor for a given geometry may be approximated with the parallel plate capacitor equation. The Inductance of the connector wires is estimated using rule of thumb by 1 μH per 1 m cable length. The serial load resistance of the structure is considered in simulation. In Figure 8.122 the equivalent circuit for simulation of the demonstrator is shown.

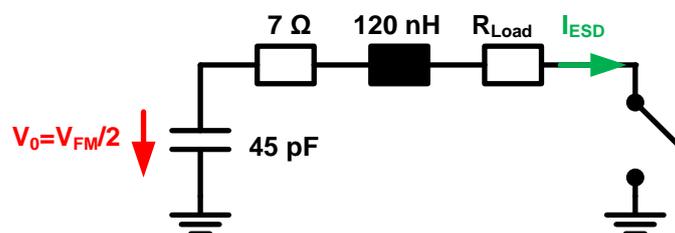


Figure 8.122: Demonstrator equivalent circuit

In Figure 8.123 simulated results are compared to measurement for 0 Ω and 50 Ω loads.

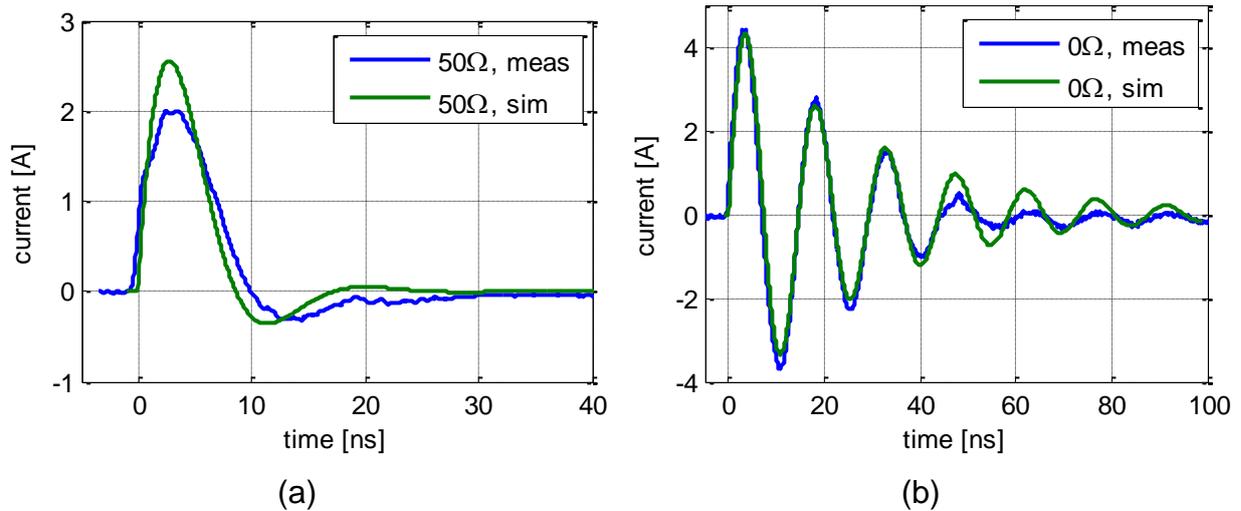


Figure 8.123: Demonstrator measurement $V_{\text{charge}} = 1 \text{ kV}$ (a), measurement and simulation (b).

Presented curves show a good matching between measurement and simulation. Deviations between the curves can be referred to the simplified demonstrator model and resistance tolerances of loads ($\pm 10\%$ components). The results show that the electrostatic induction can be modeled by an equivalent capacitor between the source and victim part of the device.

Demonstrator is used to reproduce a possible failure on electronic devices. A LED on the PCB is assumed to be a victim device. The LED is characterized in section 7.6.5.6.2 thus a simulation based analysis of the setup can be done. In measurement one contact of the LED is soldered to a connecting wire of the demonstrator. The demonstrator is charged by means of ESD generator. The discharge is triggered manually by shortening the LED to ground. Current through the LED is measured with a Fisher F65 current probe. LED failure is detected measuring leakage current at two DC spots. The critical ESD generator charge voltage is 20 kV. Figure 8.124 shows the measured critical current curve.

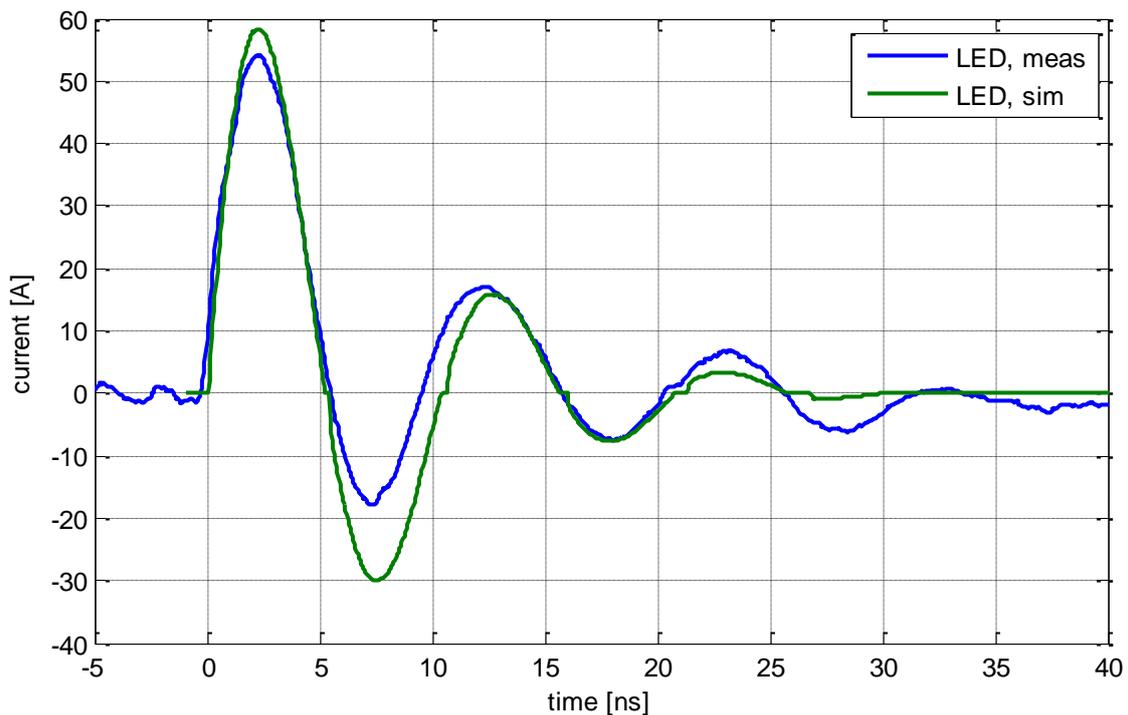


Figure 8.124: Comparison of simulated and measured critical current on LED

The failure is reproduced in simulation. Demonstrator equivalent circuit presented in Figure 8.122 is used in combination with LED. Figure 8.125 shows the simulated setup. Values for parasitic elements of the setup are adjusted to better fit the measured curve.

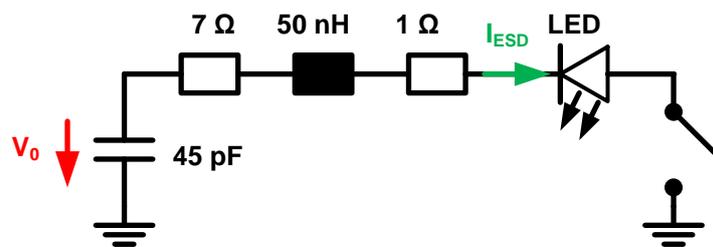


Figure 8.125: Setup for LED failure reproduction

Figure 8.124 compare the simulated and measured current on LED. Failure energy of the measured current shape is estimated using the modeled IV-curve of the LED. Table 8.29 compares all amplitudes. Simulated energy is similar to the measured one. The deviations to the 100 ns TLP measurement are only 2.5% and 6.2%. High measured current of demonstrator discharge in combination with similar failure energies states a thermal failure of the LED. High charge dissipation of the demonstrator results in considerable deviation in demonstrator charging voltage. Other materials for the charged surface of the demonstrator would provide more reliable results.

	V _{charge} [kV]	V _{max} [V]	I _{max} [A]	E [μJ]	Deviation [%]
Simulation	2.9	354	57	79	2.5
Measurement	20	-	55	76	6.2
TLP measurement	550	99	9	81	0

Table 8.29: Comparison of simulated and measured failure energies at LED

This study shows that ESD due to electrostatic induction can be reproduced with simple demonstrator. The simulated charging voltage of the demonstrator, which is required to damage the LED is only 2.9 kV. Compared to other studied ICs is the LED a robust one. A sensitive victim IC combined with more critical physical dimensions of the electrostatic induction setup may result in a failure by even less charging voltage.

8.6.5 Conclusions

Electrostatic charging of automotive parts as a result of triboelectric effect is widely spread in field and in automotive production lines. An increased application of plastic heightens achievable voltages. In general both conducting and dielectric parts may be affected.

Triboelectric charged conducting surfaces may directly threat sensitive electronics. According to low serial discharge resistance, high current peaks may arise. If the potential difference to an adjacent victim exceeds sparking voltage, a low ohmic air discharge of the source device will take place. It should be noted that all metallized plastic surfaces, like chromed décor parts, are conducting too. Depending on surface area considerable capacity up to several dozen pF is realistic. It is shown that LED rear light has a capacitance of about 50 pF. Combined with high voltages and low discharge resistance high amounts of energy may be accidentally released. This can lead to permanent damage of electronics.

Triboelectric charged dielectric surface by itself is not a threat. The electrons in a nonconductor are not free to move about the object. However, a sudden discharge with a freeing of sufficient amount of energy is impossible. But dielectrics may cause electrostatic induction in conducting parts nearby. Because of slow charge dissipation of dielectric, a potential threat may be much later than at the time of charging. In the case study still 40 % of the initial charge were measured after 1 hour under normal environment conditions (see Figure 8.117). Electrostatic induction may cause redistribution of electrical charge in floating conducting parts. As it was shown in the study an ESD event of the conducting object itself was triggered either when plugging e.g. a charged PCB or when exceeding the sparking voltage e.g. between a metallized part and a PCB.

Preventing charging due to electrostatic induction is only possible to a limited extent. It involves substantial costs. In general an ESD threat may be minimized by grounding of all conducting surfaces both metals and metalized plastics. This

measure reduces the chance of sparking for electrical induction. Good grounding combined with a connector with advanced ground contacts will safeguard the electronics when plugging in case of a charged PCB due to electrostatic induction.

If a good ground connection of the conducting part cannot be guaranteed over the service life, a possible ESD event should be assigned in a controlled way. This effect may be achieved in a constructional way. ESD voltage is assigned by the smallest gap from floating conducting parts to a PCB of the ECU. For all measures the discharge path should be realized by a distinct ground contact, such as conducting fixations. Spiky geometry of discharge contacts ensures field enhancement.

8.7 Charging Effects due to Heating, Cooling and Mechanical Deformation of Components

Charging of piezo-electric components can occur due to cooling and heating. Piezo elements are widely used in sensor and actuator systems such as pressure transducers, force sensors, acceleration sensor and injection elements for common rail motors. Other typical applications are quartz resonators and resonance transformers.

8.7.1 Piezo-Electric Materials

Polycrystalline ferroelectrical ceramics, e.g. BaTiO₃ (barium-titanate) and lead zirconate titanate (PZT) are common materials with high relative permittivity used in piezo applications [54]. Piezo elements are polarized by strong electric fields which arrange the Weiss domains and define a spatial direction of the element. Due to the tetragonal structure positive and negative charges are compensated along the spatial axis (Figure 8.126). A deformation by expansion or pressure on the piezo causes a separation of charge in the element (Figure 8.127) which is known as the direct piezo effect. A deformation of the piezo can be also achieved by the indirect piezo effect when applying a voltage on the terminals. Advantages of the effects are high adjustable dynamic resolution of actuation (nm) and load carrying capacity up to 30 t without any wear.

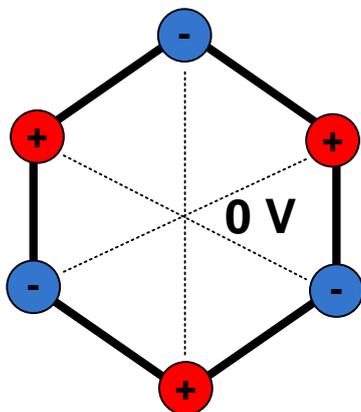


Figure 8.126: Compensation of positive and negative charged domains [54]

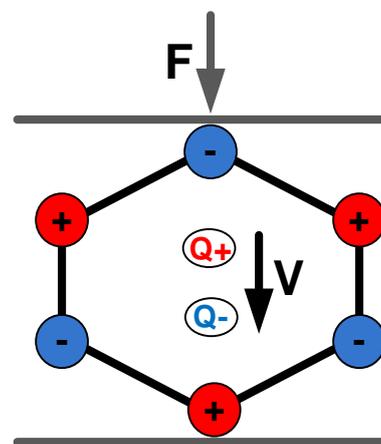


Figure 8.127: Deformation on the polarized axis causes a separation of positive and negative charged domains [54]

The deflection ability of piezo materials is increased by high temperatures. If the Curie temperature of about 150°C is exceeded the piezo crystal structure becomes cubic, which means neutral electric behavior.

8.7.2 Failure Description

ESD events occurred during assembly of piezo electric knock sensors. In Figure 8.128 constructional details of a typical knock sensor are shown [55]. Expansion of the material due to rising temperature is constricted because the piezo is placed into a none flexible housing. The sensor outputs are isolated from each other by the dielectric housing so that charge can be kept for a long time.

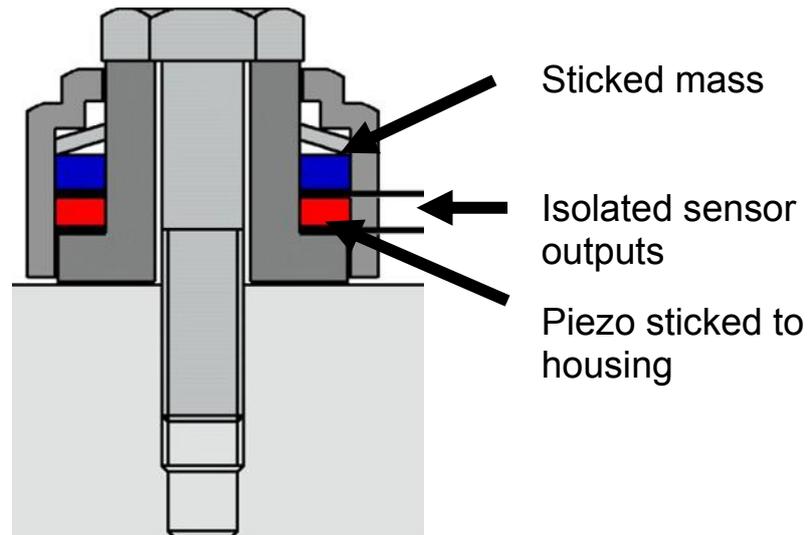


Figure 8.128: Knock sensor

The isolation material enclosing the piezo is sensitive to humidity. FAT members reported a decay time of charge of about 1 h with 20 % RH and < 1 min with 50 RH. A capacitance of 1 nF and 13 MΩ were measured with an RLC bridge at the terminal of the sensor type provided by FAT members.

ESD failure can occur during assembly as illustrated in Figure 8.129. The knock sensor is delivered and probably suffers cooling and heating causing pre-charging. Deformation of the sensor housing by screwing the sensor to motor block can increase the charge. After assembling the sensor the cable harness is connected and charged by sensor. Then the cable harness is connected to the ECU and charge is delivered to the PCB. ESD occurs when discharging the ECU by establishing the GND connection.

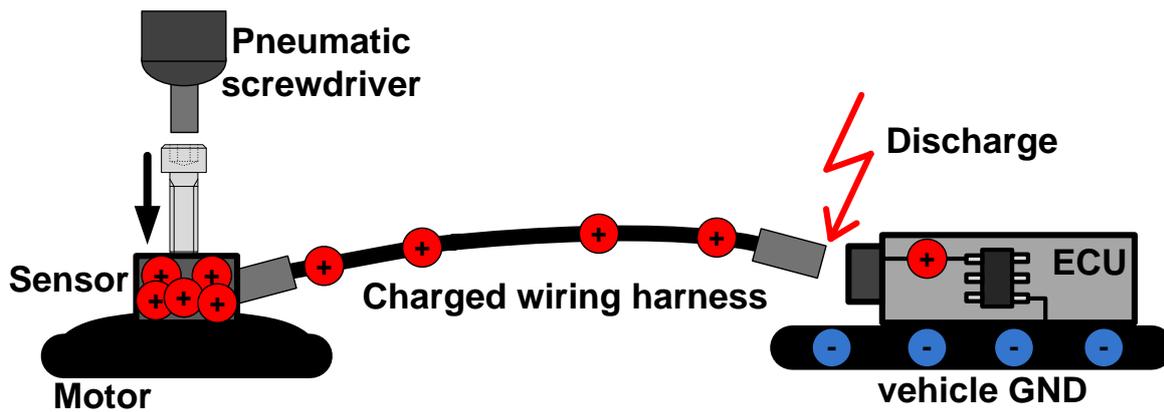


Figure 8.129: Possible ESD failure mechanism with automotive knock sensors

8.7.3 Failure Analysis

The charging voltage of piezo sensors was measured considering charging by temperature and charging by mechanic force.

8.7.3.1 Potential-Free Measurement Setup

In the setup shown in Figure 8.130 charge is brought from the sensor to one of the two electrode planes (20 cm x 20 cm) by the wiring harness with length of about 30 cm. The electric field between the planes at a distance of 5 cm is measured with a field mill. The voltage can be calculated from the field strength and distance of the planes. For calibration of the field mill a HV DC source is used.

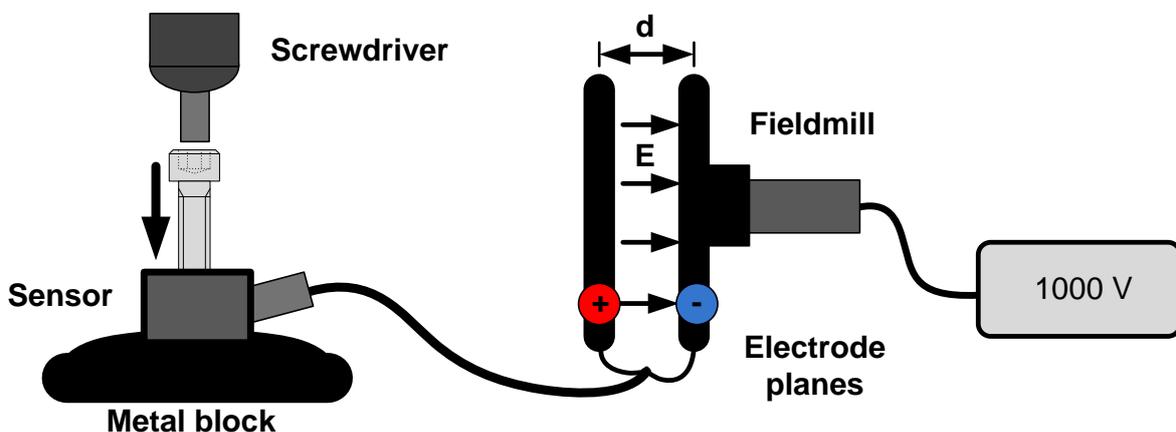


Figure 8.130: Measurement setup with field mill

8.7.3.2 Charging due to Temperature

To investigate pre-charging due to temperature knock sensors were cooled down from ambient temperature of 20°C to 0°C. Measurement results after cooling are listed in Table 8.30 for 35 RH. Either positive or negative voltages can be measured depending on the polarization of the sensor. Maximum voltage was 400 V.

Sensor 1	400 V
Sensor 2	- 200 V
Sensor 3	- 300 V

Table 8.30: Measured voltage for refrigerated sensors (0°C)

After cooling sensors were heated up by using a hot air gun. Temperature was adjusted to 100°C. Measured voltages after heating are listed in Table 8.31. Voltage increased by factor 2 after heating. Up to 800 V were measured with the field mill setup.

Sensor 1	800 V
Sensor 2	- 400 V

Table 8.31: Measured voltage after heating up to 100°C

8.7.3.3 Charging due to Mechanical Force

After cooling and heating process charge of the sensor can be increased by mechanical force on the housing. Like in assembly lines the sensor is screwed to a metal block manually or by using an electric screw driver (Figure 8.131).



Figure 8.131: Knock sensor screwed to a metal block

Measurement results are given in Table 8.32. 1400 V were measured after manual screwing to a metal block.

Manual screwing	1400 V
Electric screw driver	- 900 V

Table 8.32: Measured voltage for sensor screwed on metal block

8.7.3.4 Setup with Automotive Cable Harness

Typical ESD waveforms for a similar configuration described in section 8.7.2 were analyzed using the setup shown in Figure 8.132. The knock sensor first is tightened to a metal block by manual screwing. After charging a connection is established between the sensor and an automotive cable harness with a length of 1,6 m placed on a coupling plane. The charged wire then is discharged via an ESD current target and the waveform is measured using an oscilloscope.

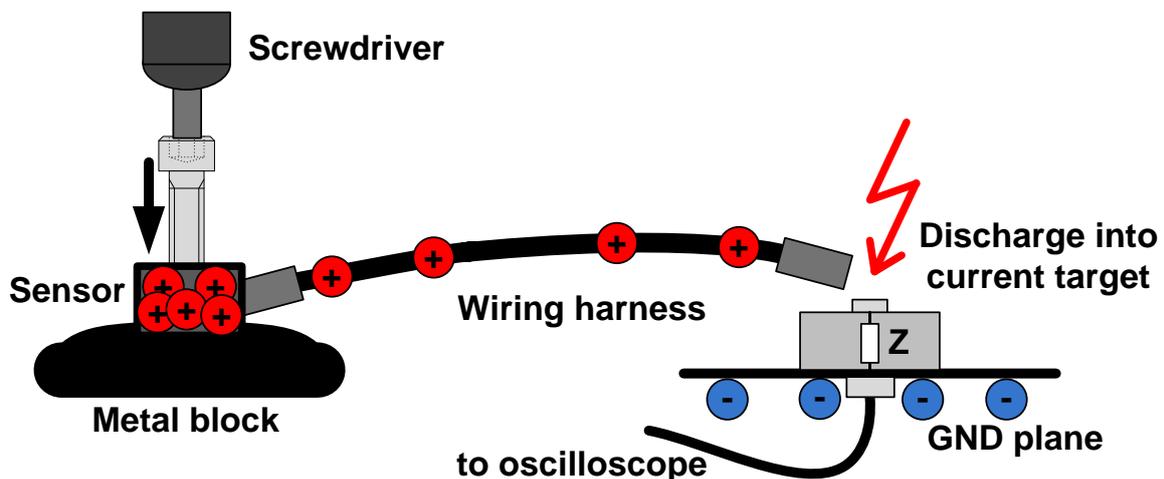


Figure 8.132: Measurement of a discharge from a charged cable harness

Two measured waveforms are shown in Figure 8.133 and Figure 8.134. Maximum measured current amplitude was 30 A. The estimated charging voltage of the cable harness is about 1200 V. The characteristic impedance of the wire can be calculated from the amplitude of the first plateau to about 120 Ω . Rise times of about 1 ns were obtained. Waveforms of repeating discharges are stable. The pulse energy reaches 89 μJ and can be compared to a 1 kV IEC generator discharge (75 μJ). Negative pulses can be measured when the sensor is released from the metal block.

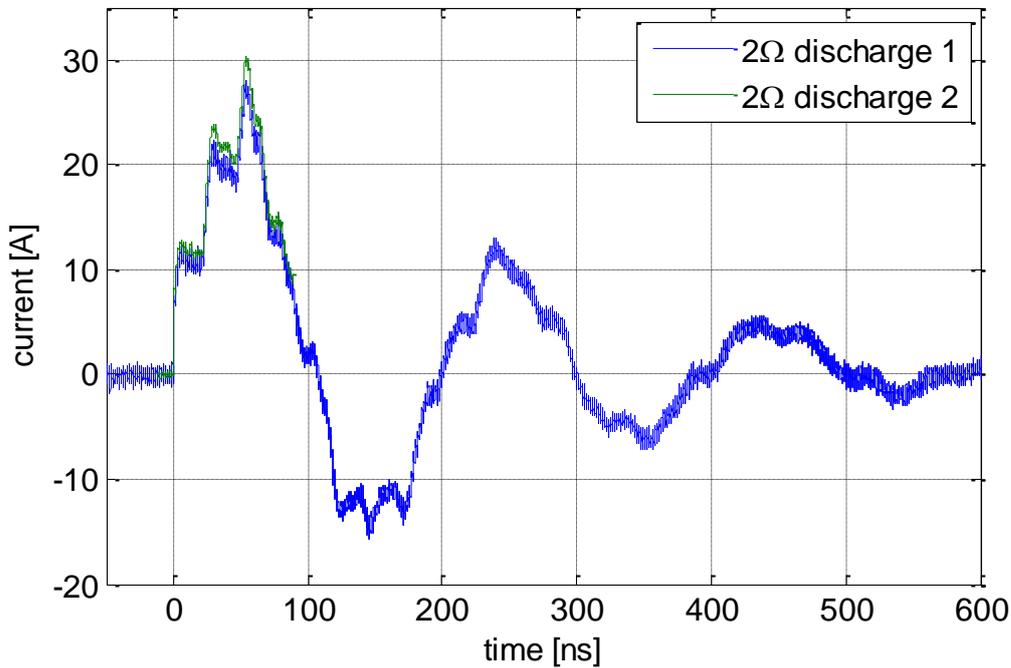


Figure 8.133: Cable discharge into 2 Ω current target

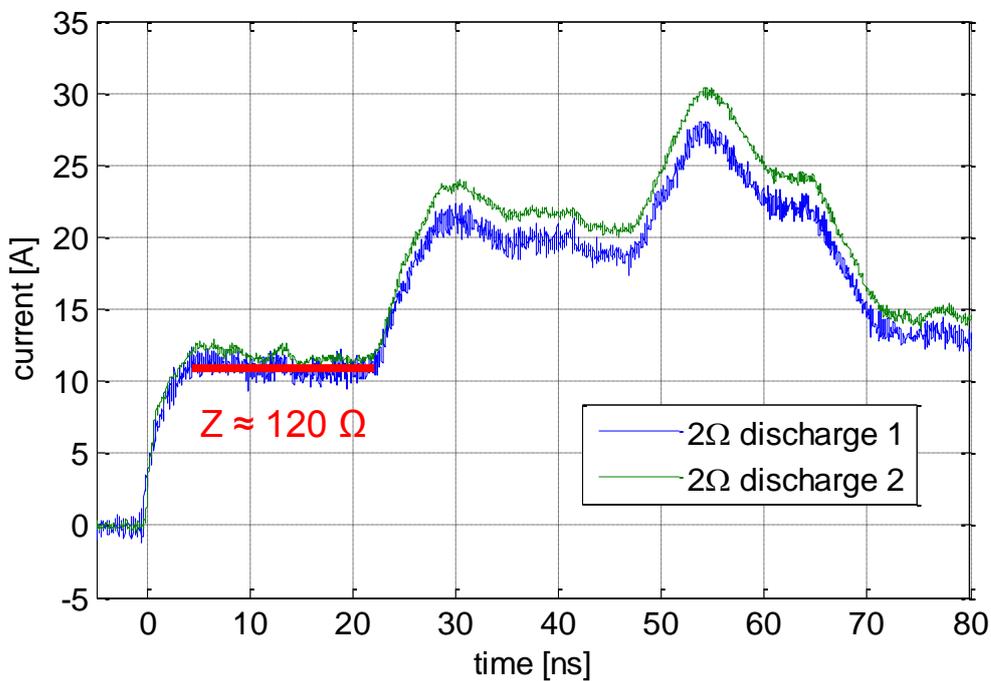


Figure 8.134: Peak current of cable discharge into 2 Ω current target

Discharges into 1 kΩ load impedance were measured using a circular PCB which can be screwed on top of the current target. A 1 kΩ SMD resistor was soldered in the discharge path on the PCB shown in Figure 8.135.

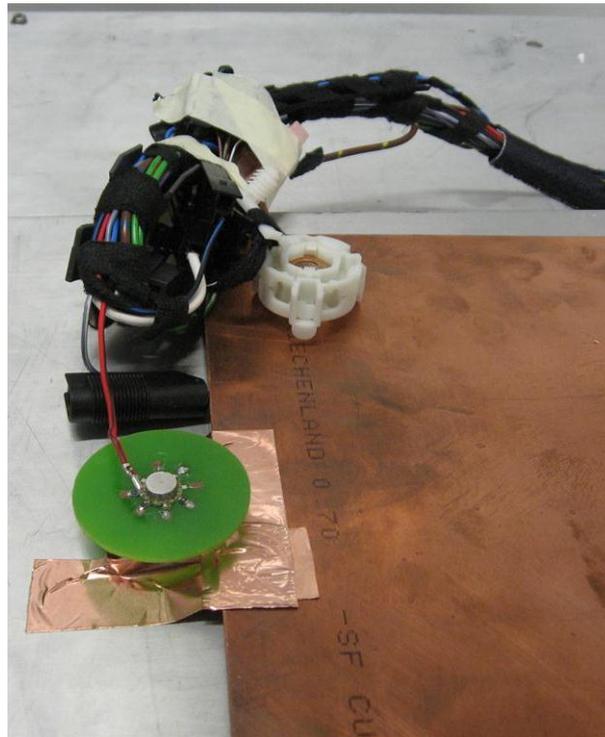


Figure 8.135: Discharge into current target

Measured waveforms of cable discharges into $1\text{ k}\Omega$ are given in Figure 8.136 and Figure 8.137. Maximum measured current amplitude was $1,6\text{ A}$ with an estimated charging voltage of the cable harness of 1200 V . Very short rise times of about 100 ps were observed. Due to the higher discharge resistance pulse energies exceed $500\text{ }\mu\text{J}$ with a pulse width of more than $2\text{ }\mu\text{s}$.

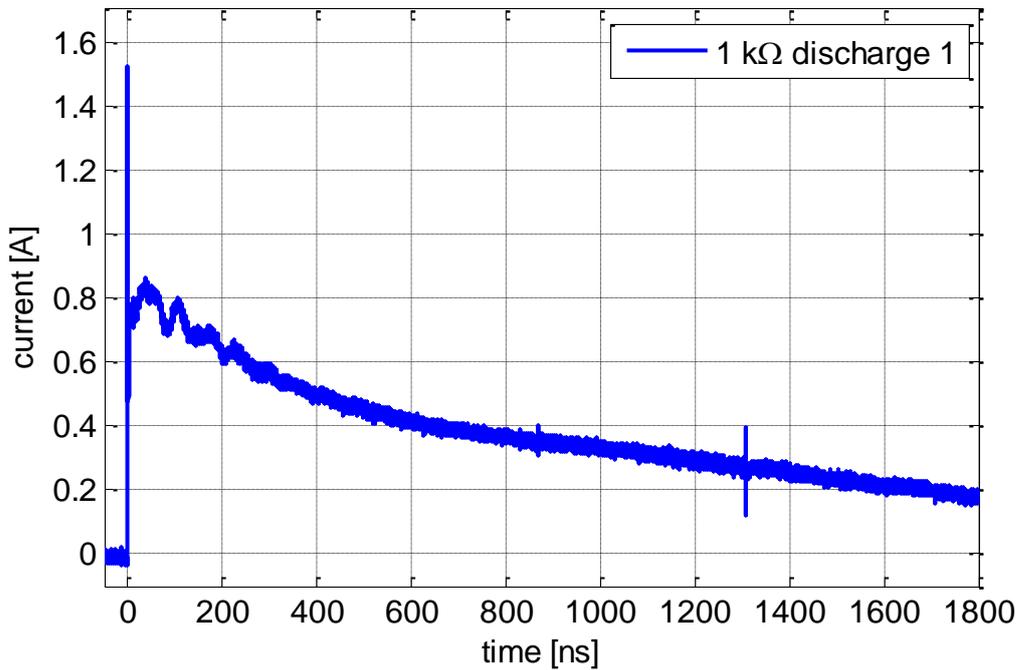


Figure 8.136: Cable discharge into 1 kΩ

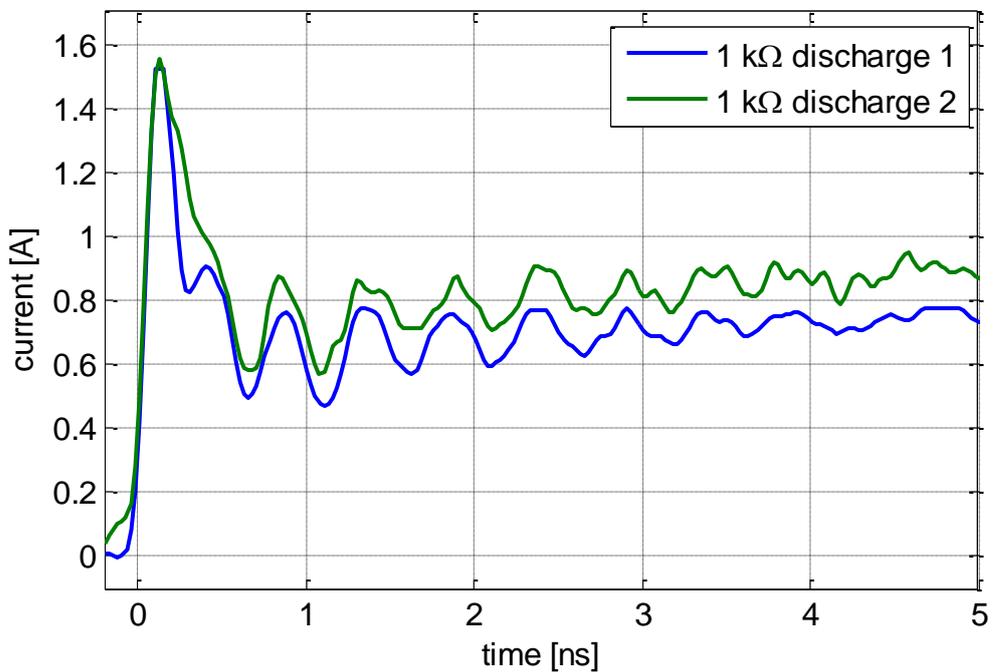


Figure 8.137: First peak of cable discharge into 1 kΩ

8.7.4 Conclusion

ESD events due to pre-charged knock sensors were analyzed. Charging can be caused by heating or cooling of the devices or by mechanical force on the housing. Maximum measured voltage at the sensor terminal was 1400 V. Charging of cable

harness on assembly lines by the sensor devices is possible. Discharge energy provided by 1,6 m wiring harness into a low impedance can be compared to a 1 kV IEC generator discharge. Nevertheless peak amplitudes of 30 A combined with short rise times were observed and can be serious threat to electronic devices when connecting the cable harness or establishing a ground connection of a charged device.

9 Impact of Selected Device Properties on System Level ESD Robustness

9.1 Connector Design with Advanced Ground Pin

Advanced ground contact is a mechanical measure to prevent ESD failures when plugging or unplugging ECUs to vehicle networks. In conventional automotive connector design all pins are arranged for coincidental contact. During plugging, the mate order of pins is not predictable. In connectors with advanced ground contacts pins, ground pins are few millimeters longer. This measure ensures that the ground pin is engaged first when plugging and removed last when unplugging.

In many industry sectors advanced ground contacts are already widespread. In [57] ESD immunity of a printer can be improved by an extended ground pin near the automatic document feeder. One of the most popular examples from consumer electronics is a USB connector. Few examples may be found in automotive area (see Figure 9.1).



Figure 9.1: Connectors with advanced ground contacts

9.1.1 Hot Plugging

Benefits of advanced ground contacts with hot plugging are discussed in a White Paper [52]. In this section main aspects are summarized.

Hot plugging refers to plugging/ unplugging ECU connectors under voltage. When hot plugging semiconductors can be destroyed by electrical overstress. It is valid for IGNITION ON as well as IGNITION OFF state. Current flows through vehicle network for several minutes after IGNITION OFF (see Figure 9.2). Each connection plugged or unplugged during this time can cause non-defined equalizing currents occurring in the vehicle network. These equalizing currents can pre-damage or permanently destroy electronic components. Investigations by Bosch revealed that a high percentage of automotive ECU failures can be prevented by using connectors with advanced ground contacts.

In a modern vehicle many ECUs are linked to each other via communication bus systems. During hot plugging it may happen that the ground contact mates last if the plug is inserted at an angle into the socket connector. Since there is no ground connection for a short time, transient currents on bus lines can affect semiconductors inside the ECU (see Figure 9.2). This failure mechanism can potentially affect all electronic components linked via communication busses.

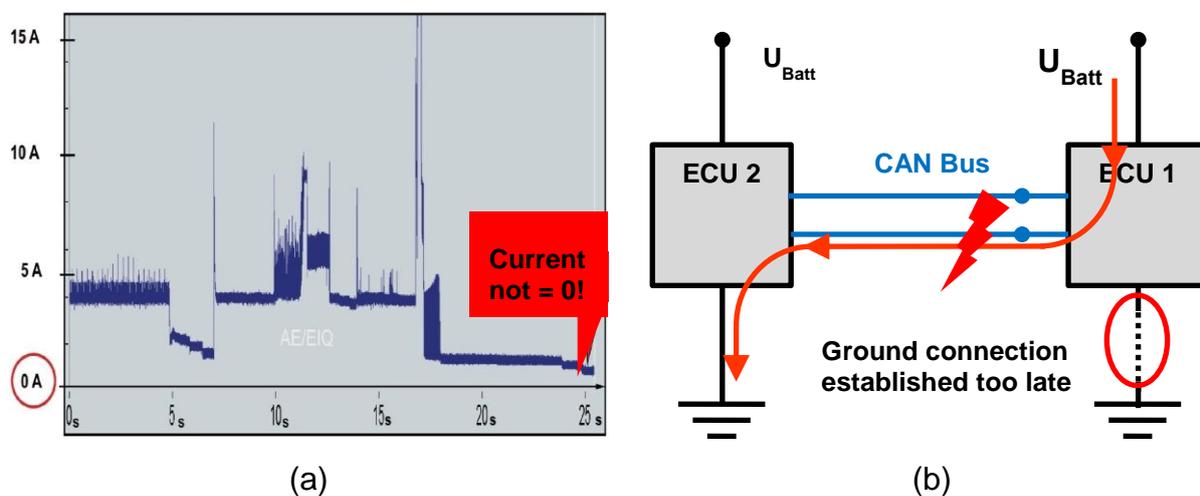


Figure 9.2: Current in the battery grounding cable after IGNITION OFF (a). Simplified circuit diagram of the failure mechanism in a data bus (b)

Damages according to hot plugging may be addressed with connectors with advanced ground contacts.

9.1.2 Charged ECU Plugging

Charged board assembly can occur in automotive production lines. In particular benefits of leading ground contacts to reduce ESD damages may be observed.

The trailer ECU discussed in Section 8.3.5 is used to show the effects of leading ground contacts in case of charged board plugging. Here Investigation focusses on qualitative results and not to measure the ESD robustness.

Test setup shown in Figure 9.3 is studied. Trailer ECU is placed on Styrofoam block. The vehicle body is represented by horizontal coupling plane. The isolated ECU is charged with 1 kV using an ESD generator. Current is measured on the PCB with an oscilloscope and CT1 probe placed between D1000 and D1001 diodes (see circuit diagram of the ECU Figure 8.74). Thus only the current through a potential victim electronic is measured and not the overall charge stored on the ECU. ECU can be discharged manually by connecting pins to HCP.

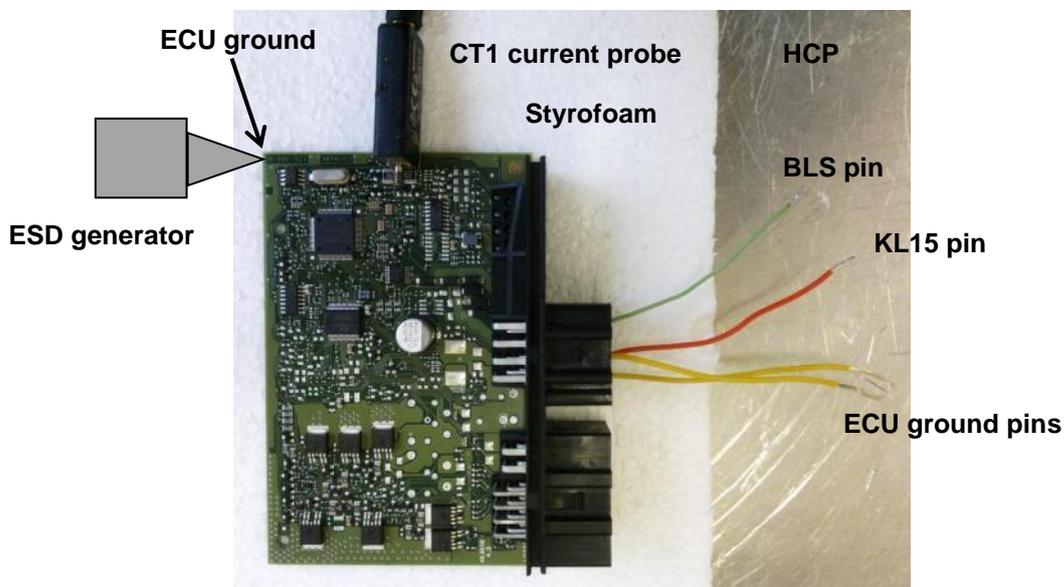


Figure 9.3: Setup for charged board plugging

In Figure 9.4 the measured current through the diodes is shown for the following setups concerning ground connection:

- BLS pin is connected first to HCP
- BLS and KL15 pins are simultaneously connected to HCP
- ECU ground, BLS and KL15 pins are simultaneously connected to HCP
- ECU ground pins are connected to HCP

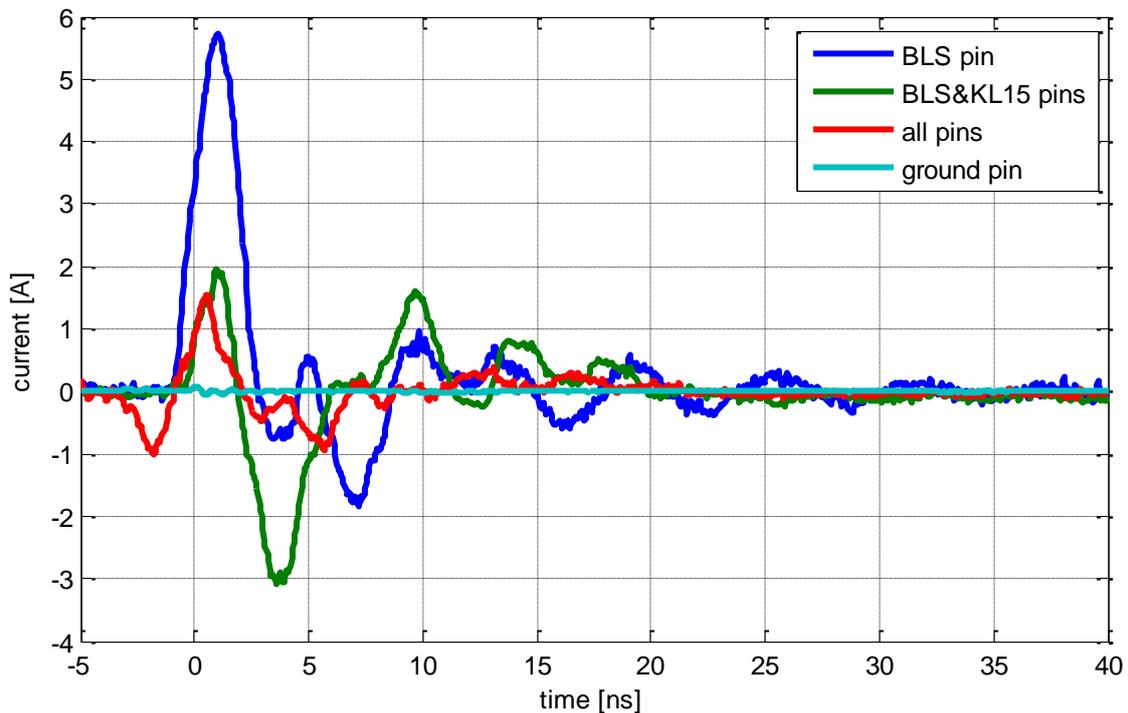


Figure 9.4: Measured current through diodes for different connection order

Very low current amplitude of about 70 mA was measured if ground pins are connected first and charge dissipates to HCP. If the BLS pin is connected first, the current flows from the ECU ground through electronic components to the HCP. Here maximum amplitudes up to 6 A were observed. If ground contacts are connected first, amplitudes are 81 times less and 733 times less energy is absorbed by the diode. Even if all pins are connected simultaneously during plugging, a significant current might be measured through electronic components.

In Table 9.1 peak amplitudes of the measured current shapes are given. Energies are estimated using the IV-curve for BAW156 diode. A security factor is assigned to each current and energy value.

Setup	I_{max} [A]	E [μ J]	$I_{max}/ I_{max, ECU_ground}$	E/ E_{ECU_ground}
BLS	5.7	2.2	81	733
BLS&KL15	3.1	1.1	44	366
all	1.5	0.4	21	133
ECU ground	0.07	0.003	1	1

Table 9.1: Amplitude of measured current shapes

If no ground connection is established most of electrical charge is stored on the floating ECU ground planes. In case ECU ground contacts are connected first to

cable harness, charges drain off to car body. Otherwise charges can be dissipated through sensitive electronics. This may cause a permanent damage or a pre-damage of component.

9.1.3 Conclusions

Connectors with advanced ground contacts are widespread among many industry sectors and already help to prevent ESD damages. This constructional change of the connector assures a specification of a discharge path when hot plugging and charged ECU plugging. Plugging and unplugging in a vehicle become more robust against ESD. According to statistics presented in [52] a large number of semiconductor ESD failures could be avoided if advanced ground contacts were used. This applies in particular for test, control and adjustment situations. The benefit from advanced ground contacts was analyzed in a case study with an automotive ECU, where a charged board was plugged in different grounding configurations.

Implementation of advanced ground contacts in future connector design should be taken into account.

10 Protection Strategies

10.1 External ESD Protection

External ESD protection elements may significantly improve system level ESD robustness of the overall system. The white papers from the Industry Council on ESD Target levels propose the SEED design process to optimize the PCB based overvoltage protection relative to the on-die ESD protection (www.esdindustrycouncil.org).

10.1.1 Nonlinear Shunt Elements

For ESD protection on fast signal pins a transient voltage suppressor diode (TVS diode), a varistor, a variable voltage polymer (VVP), or a spark gap may be used. Characteristic parameters are the breakdown/ firing voltage where the device becomes conductive, the clamping/ burn voltage where the device performs its suppression tasks, and the parasitic capacitance. Parallel parasitic capacitance to ground is in inverse proportion to the cut-off frequency. The breakdown/ firing voltage of the protection element should be smaller than the breakdown voltage of the IC. Nonlinear shunt elements do not store the ESD pulse energy, but conduct it directly to ground.

Characteristic parameters for several devices from different manufacturers were measured. The breakdown voltage is defined as a value at current of 1 mA, clamping voltage is at 1 A. Both parameters can be acquired by a source meter. VVP and spark gap characteristics are acquired by TLP. The capacity is measured by VNA at 10 kHz. Results are shown in Figure 10.1 and Figure 10.2. Commonly used

capacitors are also shown. A definition of a clamping/ breakdown voltage for a capacitor is not possible.

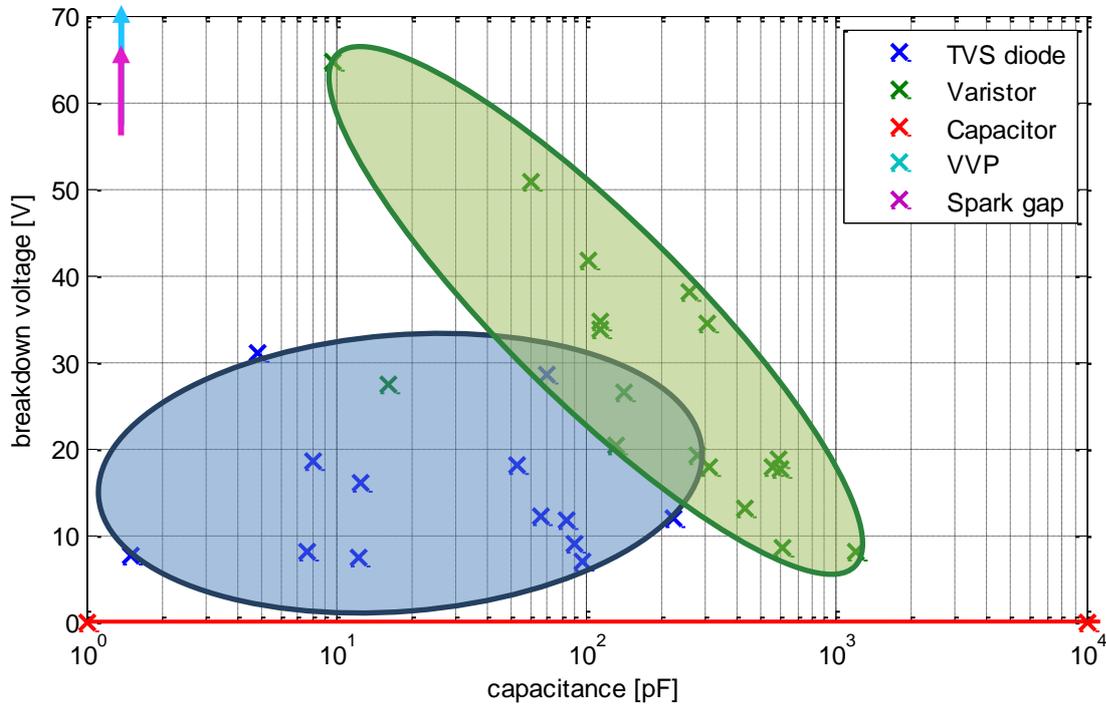


Figure 10.1: Capacitance vs. breakdown voltage for ESD protection elements

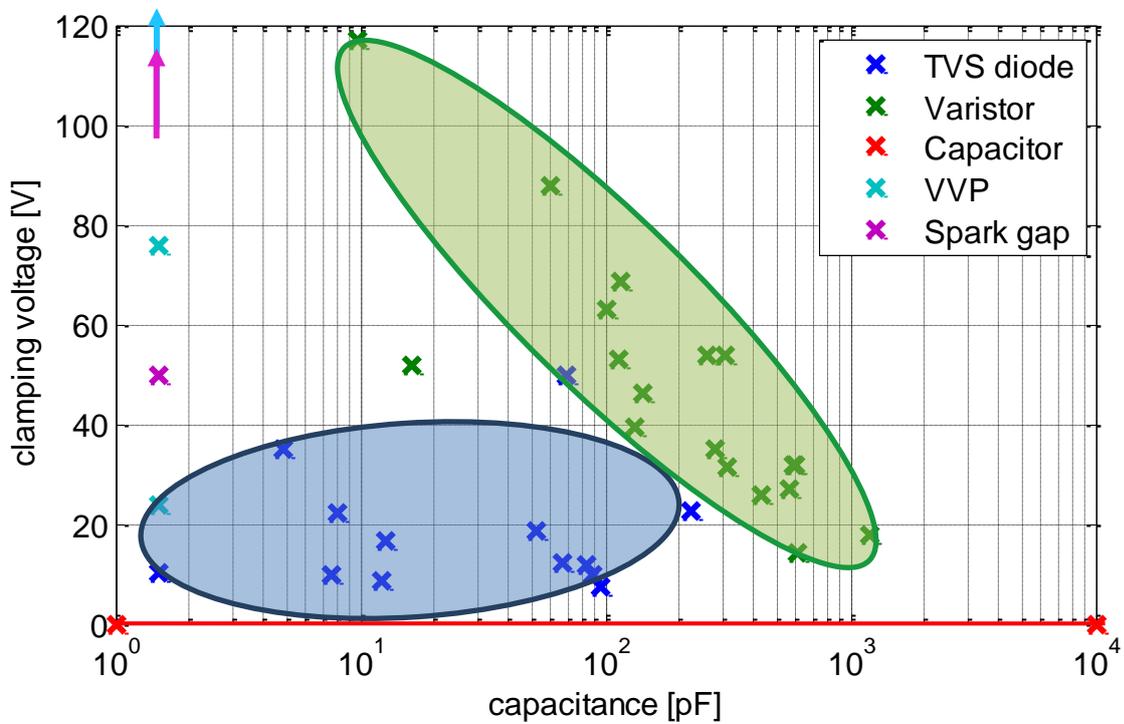


Figure 10.2: Capacitance vs. clamping voltage for ESD protection elements

TVS diodes combine low clamping/ breakdown voltage and low parasitic capacitance. Values of less than 1 pF could be observed. In case of varistors a trend of lower breakdown voltage by higher capacity can be seen. Spark gaps and VVPs capacitance is very low partly below 1 pF, the smallest firing voltage is about 350 V. A summary table of all characterized and modeled nonlinear shunt elements and their relevant characteristics is provided in the annex.

10.1.2 Voltage Variable Polymer

The non-linear polymer (by Littlefuse and EPI) acts somewhat like a spark gap, but important differences are:

- The spark gap does not limit the voltage before it avalanches, but the non-linear polymer does limit the voltage before it avalanches to a value of about 50-300V. People usually attribute this to inter particle tunneling effects, however the exact physics are not fully understood.
- The spark gap takes a relatively long time (microseconds) to avalanche. The non-linear polymers turn on much faster, usually within less than 1 ns. How fast depends on how much larger the voltage is relative to the voltage at which the device clamps during its first nanosecond (do not confuse with the clamping voltage of times > 1 ns, as this voltage is usually 25-40 V, both for non-linear polymers and for spark gaps).

Polymers varistors are popular devices for ESD protection. Their polycrystalline material creates a TVS device with very low capacitance; thus, polymers are effective devices for very high speed data line signals. A polymer's electrical characteristics are similar to a thyristor and the devices exhibit "snap-back" in their current versus voltage curve. The trigger voltage of a polymer can be as high as 1.0 kV, while the clamping voltage is usually 20 to 50 V. Polymers have a limited service life and their electrical characteristics are typically guaranteed for only one to five thousand surge events.

Polymeric material acts somewhat like a spark gap, but having a lower clamping voltage and a very fast response. As example, to illustrate the properties one device was investigated: EPI 0603 300 V

In the frequency band from 30 kHz to 6 GHz this device has very little influence, indicating that its capacitance is < 0.1 pF. The time domain characterization using a TLP shows the typical behavior for this class of devices: An overshoot up to about 300V, then a rapid collapse to a limiting voltage of about 25-40V.

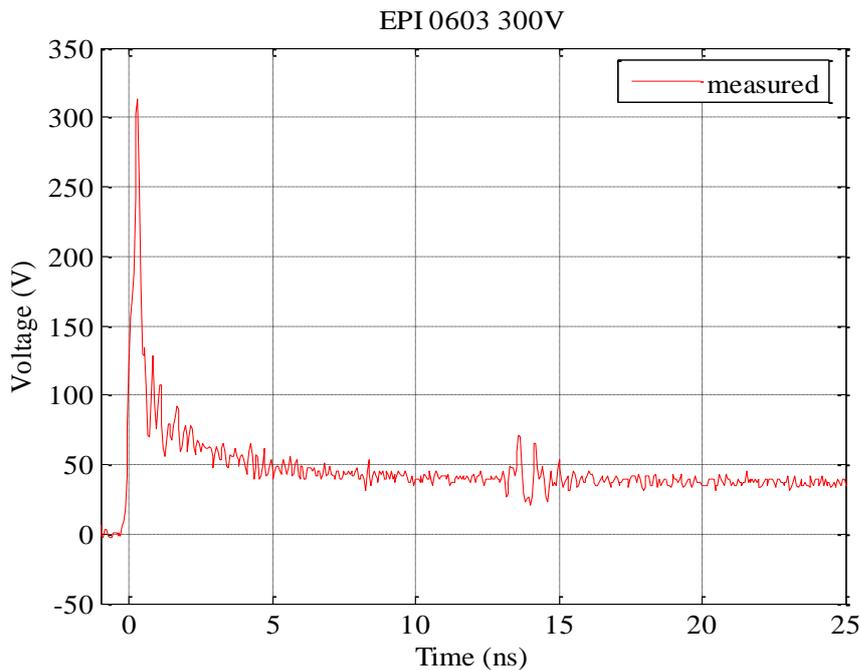


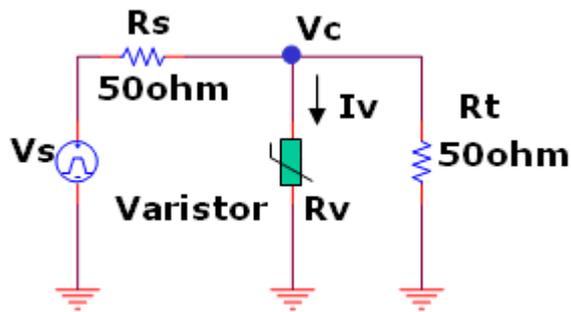
Figure 10.3: Time domain response under TLP source voltage of 1000 V.

10.2 Varistor

Varistor has various non-linear characteristics. It is characterized by a turn on voltage, below it, it acts as a capacitor. The behavior above the turn-on voltage is complex and cannot be fully modeled by a non-linear voltage source and a voltage independent capacitor. Turn on delays and possibly non-linear capacitances would be needed for a full model.

10.2.1 Time Domain Analysis

The time constant of the observed rising voltage depends on the applied voltage. The pulse response of Amotech 14V 160pF in Figure 10.5 shows no observable turn-on at 20V. Consequently, a longer rise time (time constant $\tau = RC$) is observed.



- Vs: pulse source voltage
- Rs: pulse source impedance (50ohm)
- Rt: termination resistance of scope (50ohm)
- Vc: clamping voltage on varistor
- Iv: current flowing on varistor for given clamping voltage
- Rv: resistance of varistor for given clamp voltage
- $R_v = 50 \cdot V_c / (V_s - 2 \cdot V_c)$

Figure 10.4: Test setup of the varistor. The varistor is placed between a 50 Ohm trace and ground. A voltage from a TLP is applied (50-Ohm source impedance) on one side of the trace, on the other side the voltage is measured using an oscilloscope with 50 Ohm input.

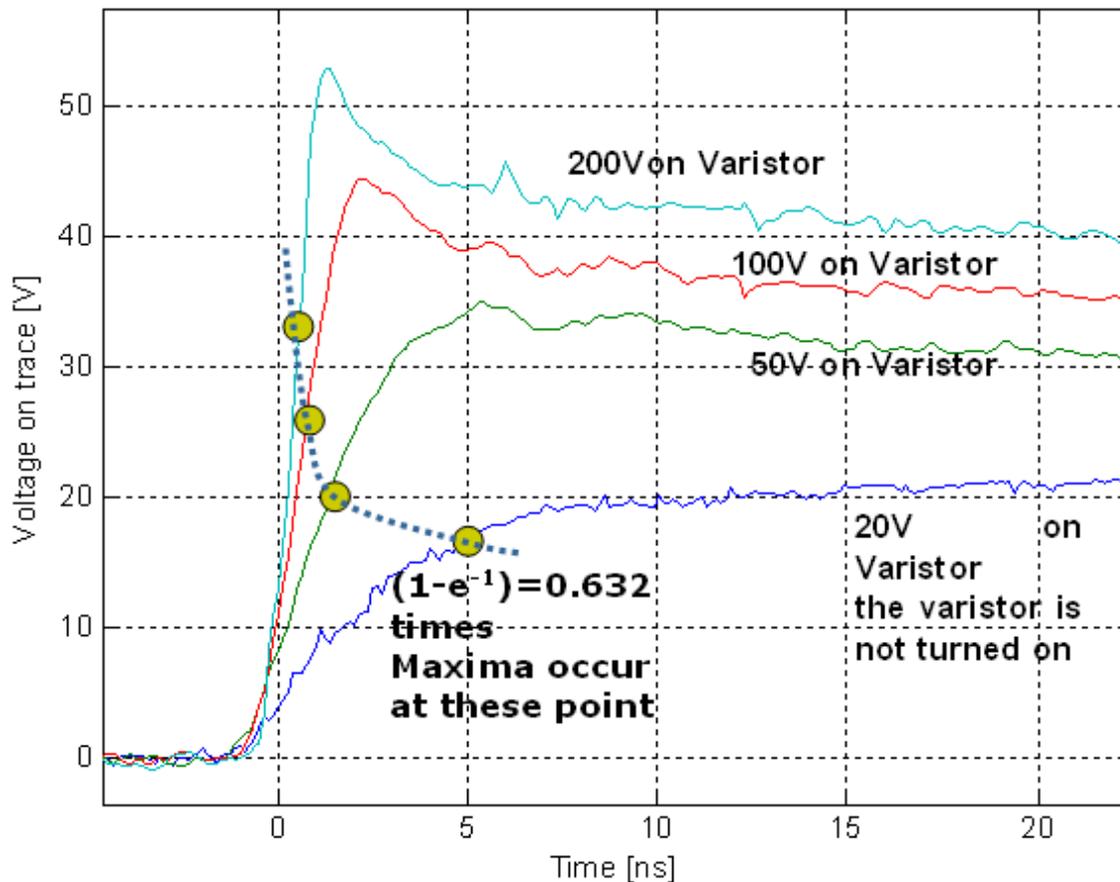


Figure 10.5: Rise time of the pulse response, there is a reduction in rise time with increased applied voltage.

10.2.2 V-I Relationship of Varistor

To observe long term response a longer pulse was needed. By changing the transmission line length, the pulse width of the TLP was increased.

- Source Voltage: 1 kV, 2 kV and 4 kV.
- Attenuator1: 22 dB.
- Pulse Width: 125 ns.

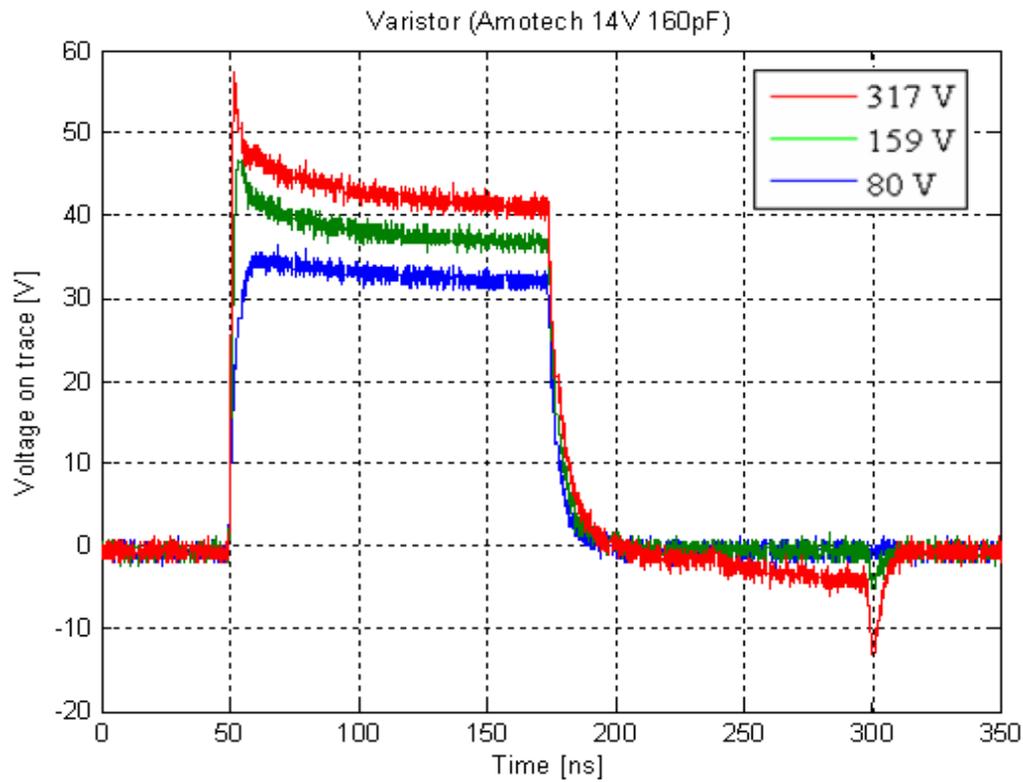


Figure 10.6: Pulse response of Amotech 14 V 160 pF under different Vs.

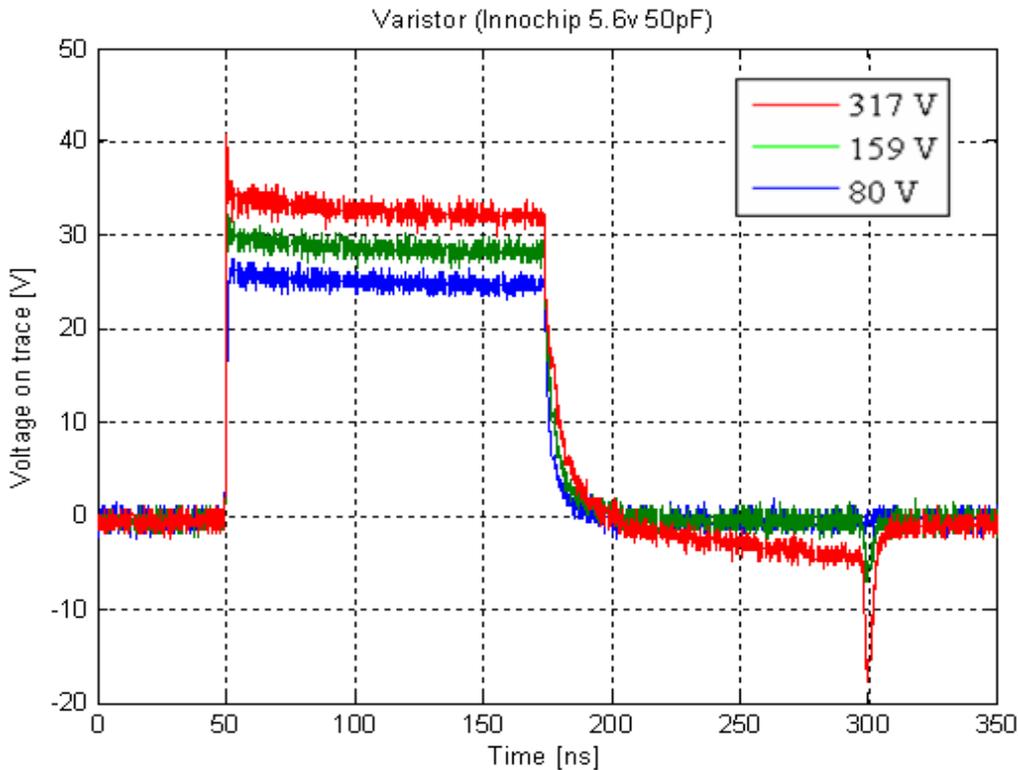


Figure 10.7: Pulse response of Innochip 5.6 V 50 pF under different Vs.

Calculation: V_c is read from Figure 10.5 and Figure 10.6, $R_v = 50 \cdot V_c / (V_s - 2 \cdot V_c)$

Vs(V)	Amotech 14V 160pF			Innochip 5.6V 50pF		
	Vc(V)	Iv(A)	Rv(Ohm)	Vc(V)	Iv(A)	Rv(Ohm)
80	33	0.28	117.8	24	0.64	37.5
159	37	1.7	21.7	28	2.06	13.6
317	42	4.66	9	32	5.06	6.3

Table 10.1: Voltage and current characteristics.

The resistance is calculated as the ratio of V and I at the voltage shown, not as the differential resistance (slope of the V-I curve) at the measurement point.

The non-linear resistance characteristic of the varistor can be expressed in exponential function $I = KV^\alpha$.

For Amotech 14V 160pF: $I = 5.5 \times 10^{-19} V^{11.66}$

For Innochip 5.6V 50pF: $I = 7.7 \times 10^{-11} V^{7.18}$

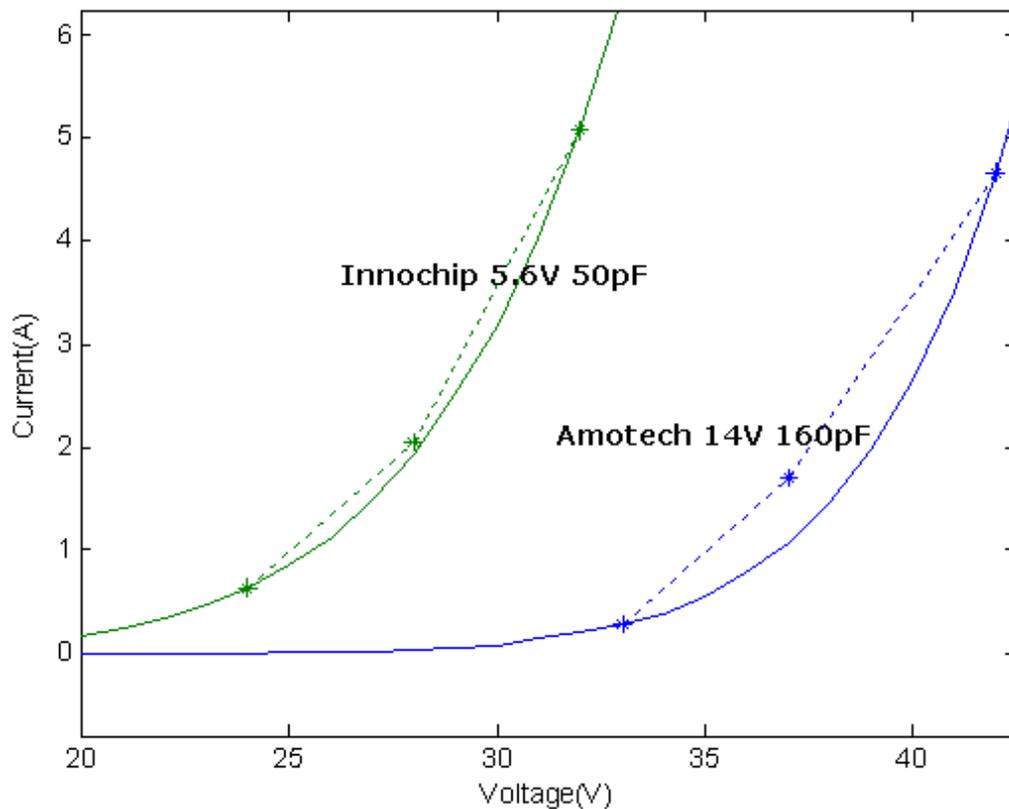


Figure 10.8: Voltage vs. current for the varistors. The solid lines are derived from the above equations, and the stars are from Table 10.1

Especially the Amotech varistor shows a complex turn-on. As shown in Figure 10.7, a voltage overshoot takes place. As shown later by the simulation model, this cannot be explained by a voltage independent capacitance and a non-linear V-I characteristic.

10.2.3 Frequency Domain Characterization of Varistors

The S-parameters are measured using Network Analyzer. The varistor is in a turn-off state during the measurement, the data show the effect of parasitic capacitance and loop inductance (via + mounting + self inductance, 0.45 nH as measured elsewhere).

In Figure 10.9 the resonance frequency is 600 MHz. Using 0.45 nH, a capacitance of 160 pF is calculated.

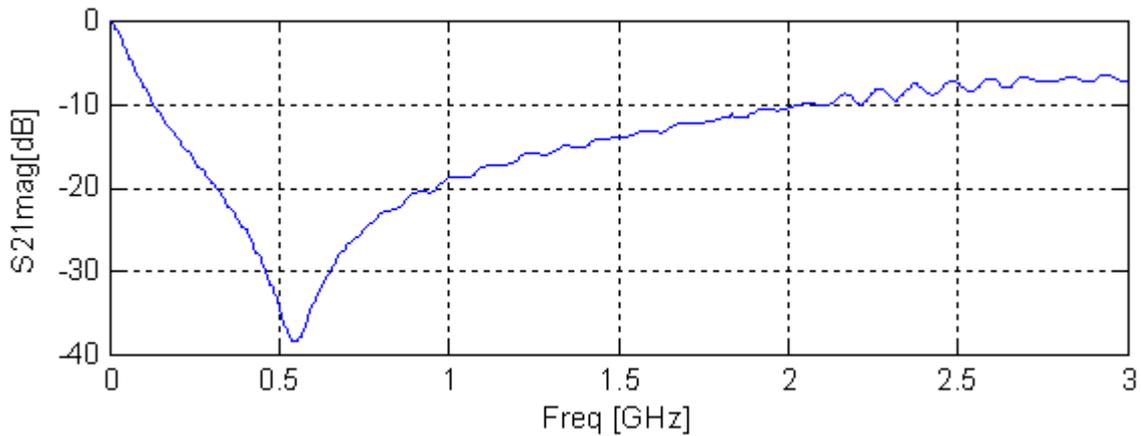


Figure 10.9: S21 of the Amotech 14 V varistor, showing 160 pF.

10.2.4 SPICE Model and Simulation

The basic response of the varistor can be modeled by a non-linear resistor parallel connected with a capacitor. The non-linear resistor dominates the clamping operation and can be expressed by a voltage controlled current source in SPICE. The relation between voltage and current of the controlled source can be expressed by the equation stated in 10.2.2 above.

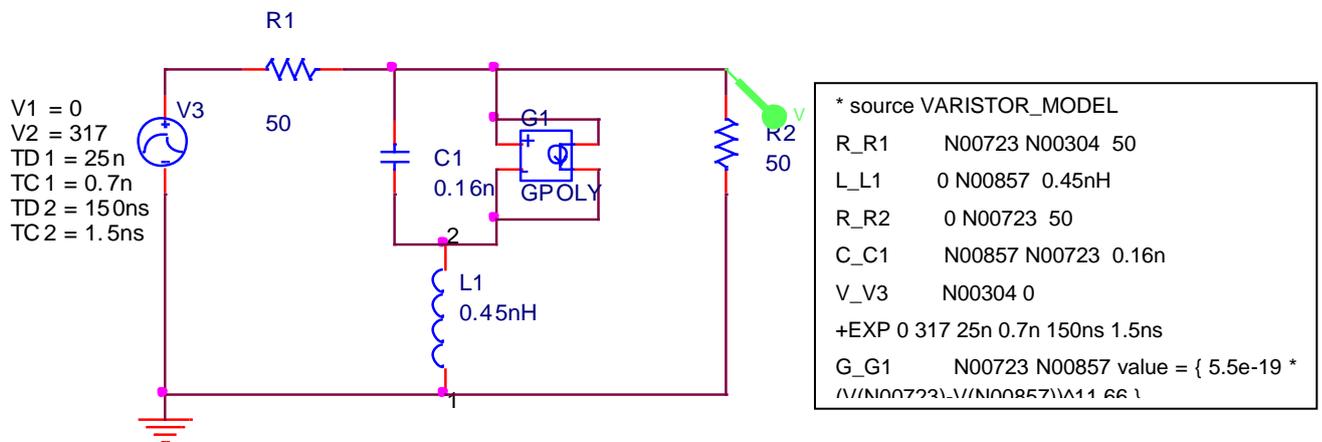


Figure 10.10: SPICE model for Amotech 14V 160pF

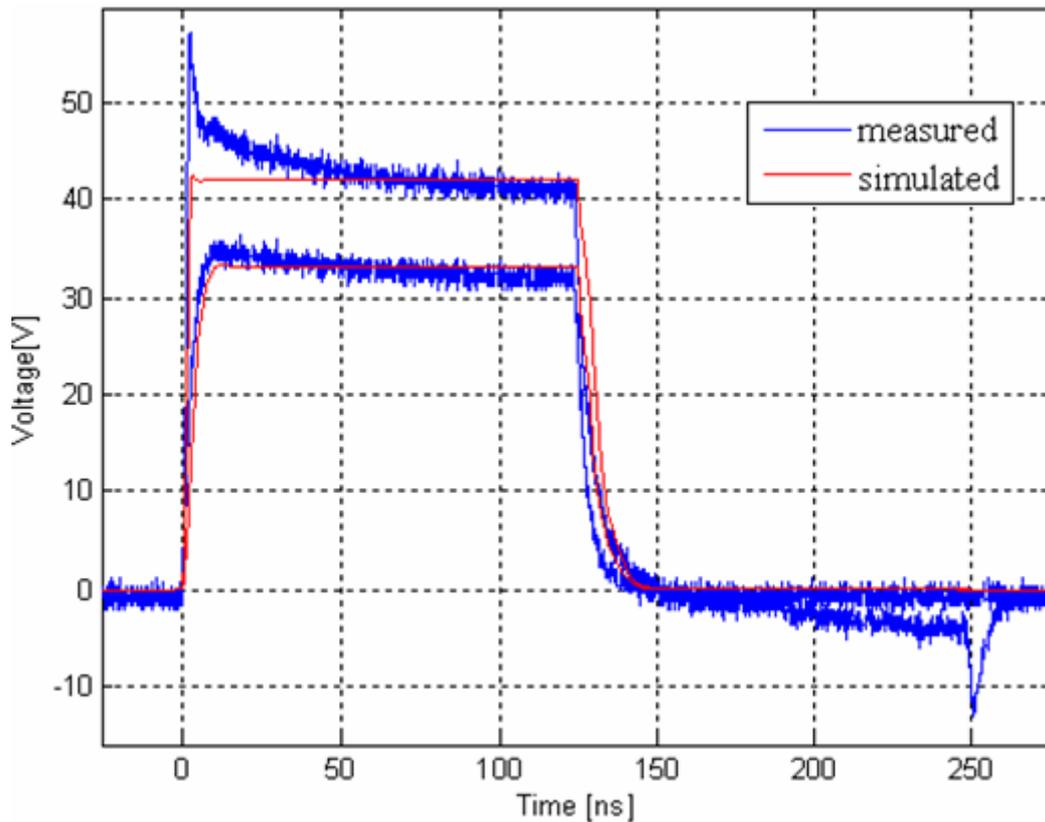
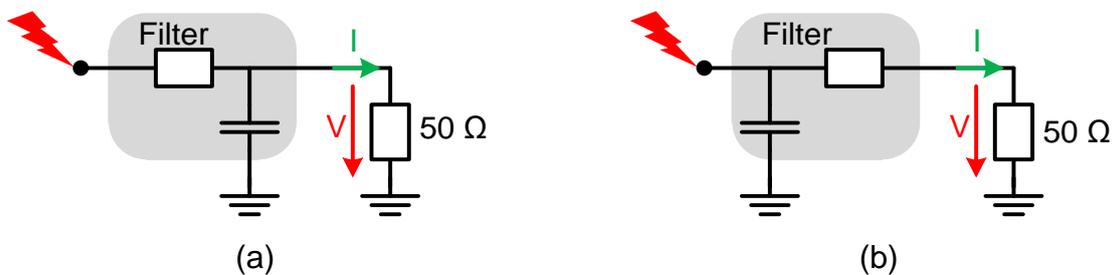


Figure 10.11: Simulation and measurement at $V_s = 80\text{ V}$ and 317 V .

The SPICE model estimates the clamping voltage pretty well. But it can't predict the overshoot and undershoot spike in high voltage range. Both of these effects are caused by physical processes that are presently not fully understood.

10.3 Frequency Selective Filtering

Frequency selective filtering as ESD protection can be a cheap and effective solution. A high frequency ESD event may be attenuated by an appropriately designed low pass filter. Figure 10.12 shows different designs terminated by a $50\ \Omega$ resistive load.



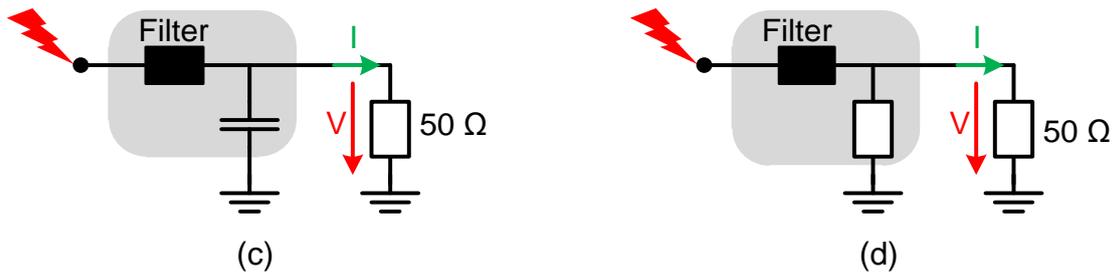


Figure 10.12: Low-pass filters with passive components

Filter in Figure 10.12 (a) consists of a resistor in series with a load and a capacitor in parallel. The capacitor should be placed close to a victim IC pin. Figure 10.12 (b) is a common design where a capacitor is located close to a socket. It filters the transients and can store most of the energy of an ESD pulse. Capacitor discharge time is controlled by a series resistor. Additionally the resistor reduces the first voltage peak on the IC pin. The design presented in Figure 10.12 (c) is a second order low-pass filter. Because of missing resistive part no energy can be absorbed, but the pulse duration is increased and amplitudes are reduced. Filter in Figure 10.12 (d) consists of an inductor in series and a resistor in parallel with a load.

The application of a frequency selective filter is uncomplicated for pins with a low signal frequency. For high frequency signals special band pass structures might be necessary.

The current and voltage shapes on a 50 Ω load of a 1 kV IEC discharge is shown in Figure 10.13. Simulation results for a 50 Ω load protected by filters presented in Figure 10.12 are compared in Figure 10.14, Figure 10.15, Figure 10.16 and Figure 10.17.

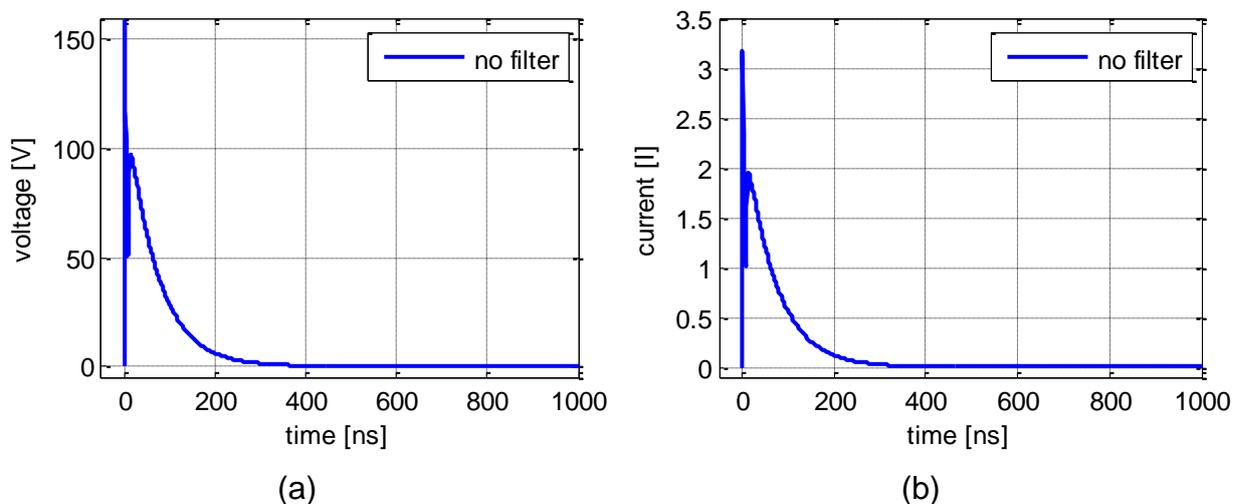
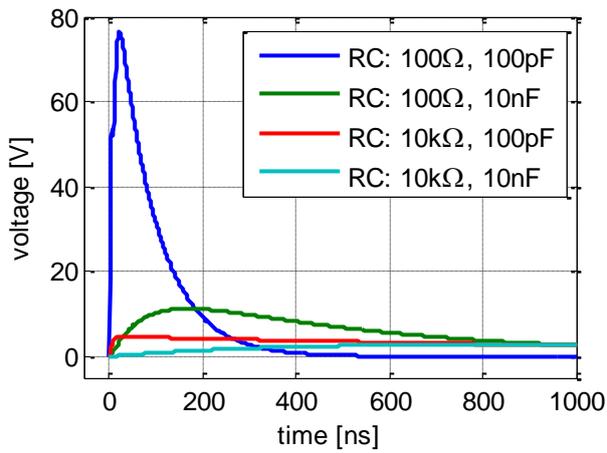
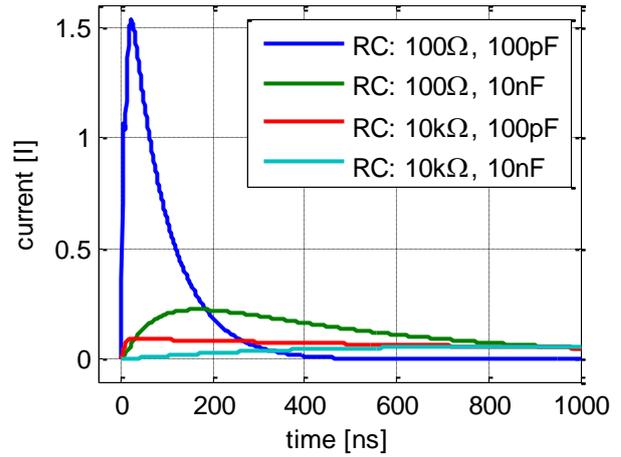


Figure 10.13: Simulated voltage (a) and current (b) at 50 Ω load for a 1 kV IEC discharge

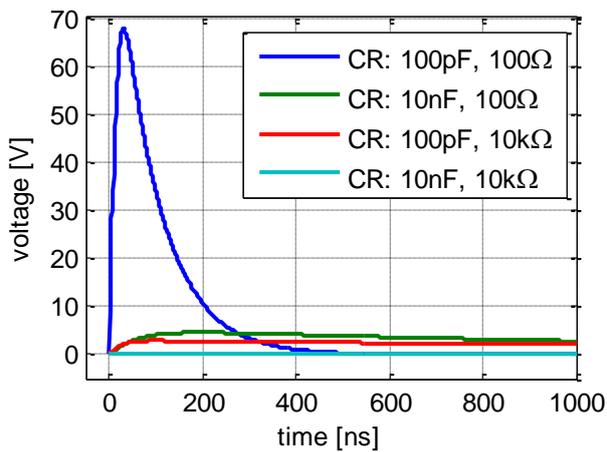


(a)

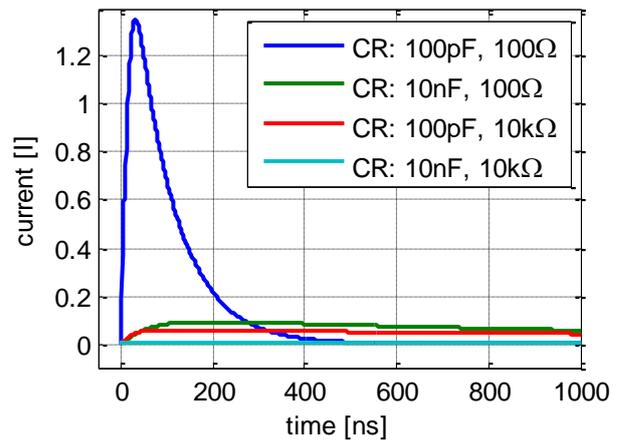


(b)

Figure 10.14: Simulation of 1 kV IEC discharge into 50 Ω load and RC-low-pass with different parameters. Voltage (a) and current (b).

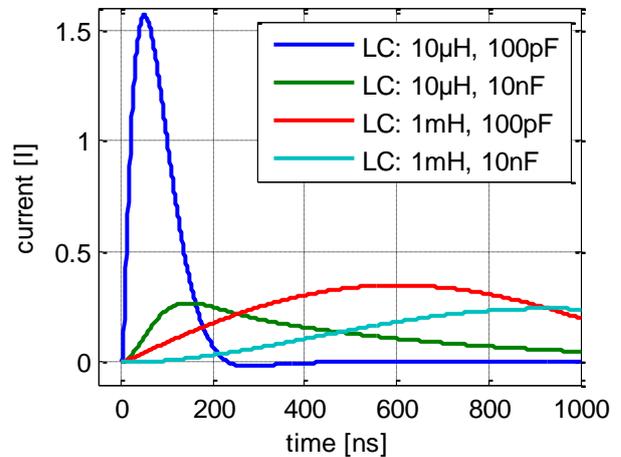
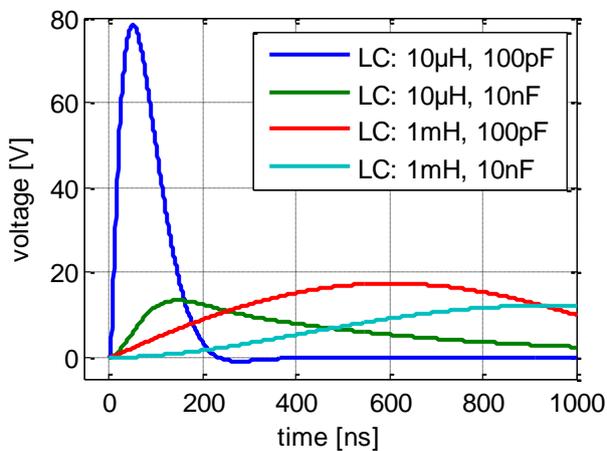


(a)



(b)

Figure 10.15: Simulation of 1 kV IEC discharge into 50 Ω load and CR-low-pass with different parameters. Voltage (a) and current (b).



(a)

(b)

Figure 10.16: Simulation of 1 kV IEC discharge into 50 Ω load and LC-low-pass with different parameters. Voltage (a) and current (b).

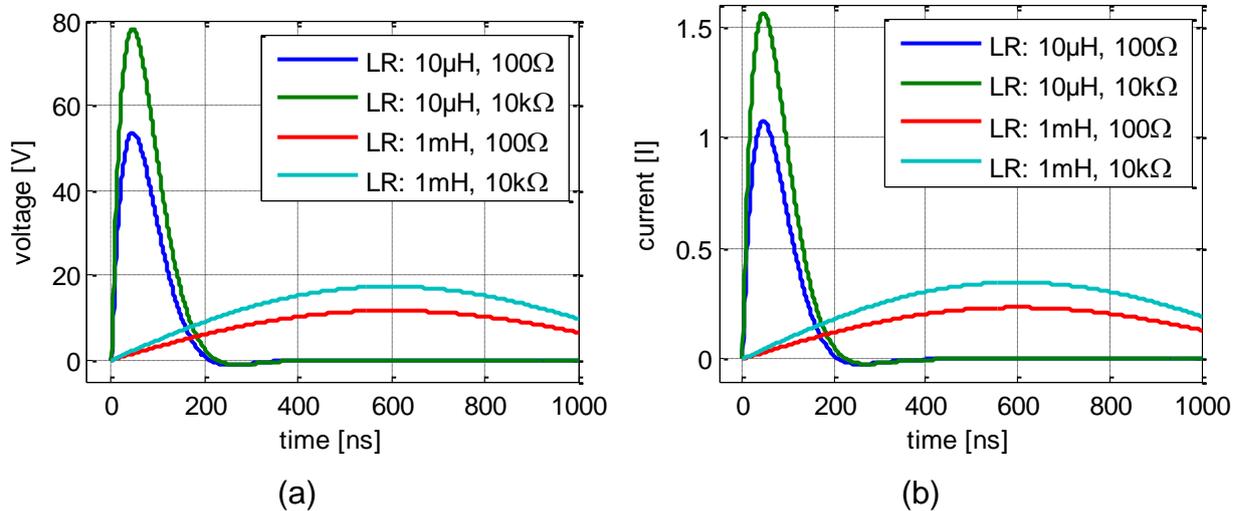


Figure 10.17: Simulation of 1 kV IEC discharge into 50 Ω load and LR-low-pass with different parameters. Voltage (a) and current (b).

All measured amplitudes are listed in Table 10.2. The amount of absorbed energy by the load is calculated only for the first 1 µs. The best ESD noise attenuation is observed for the 10 kΩ, 10 nF CR-low-pass filter. Despite missing resistive part of the LC low-pass, good results may be achieved. Every design may be tuned in order to obtain high noise attenuation. Care has to be taken that the designed filter does not affect signals on I/O pins.

ESD Filter		V_{max} [V]	I_{max} [A]	$E_{1\mu s}$ [μJ]
	no filter	158.5	3.17	9.07
	RC: 100 Ω , 100 pF	76.4	1.52	6.9
	RC: 100 Ω , 10 nF	11.2	0.22	1.04
	RC: 10 k Ω , 100 pF	4.73	0.094	0.26
	RC: 10 k Ω , 10 nF	2.83	0.056	0.1
	CR: 100 pF, 100 Ω	67.75	1.35	6.32
	CR: 10 nF, 100 Ω	4.58	0.091	0.27
	CR: 100 pF, 10 k Ω	2.88	0.057	0.12
	CR: 10 nF, 10 k Ω	0.077	0.0015	<0.01
	LC: 10 μH , 100 pF	78.3	1.56	9.03
	LC: 10 μH , 10 nF	13.42	0.26	1.13
	LC: 1 mH, 100 pF	17.4	0.35	3.64
	LC: 1 mH, 10 nF	12.1	0.24	1.3
	LR: 10 μH , 100 Ω	53.63	1.07	4.22
	LR: 10 μH , 10 k Ω	78.16	1.56	9.04
	LR: 1 mH, 100 Ω	11.68	0.233	1.63
	LR: 1 mH, 10 k Ω	17.33	0.35	3.61

Table 10.2: Comparison of simulated amplitudes for different filters

10.4 General Design Rules

The shown investigations provide directly rules for improving ESD robustness in automotive electronics. For general ESD protection many rules for system level ESD can be found in literature. System level ESD can be seen as a special branch of EMC and many EMC rules can be directly adapted to ESD. The following list provides well known rules for EMC compliant design in general and was taken in large parts from [98]. New and special automotive ESD guidelines are supplemented.

There might be situations when all rules cannot be completely satisfied. When this is the case, a conscious decision must be made about what must be sacrificed. Fortunately, most of the rules are compatible and many problems can be well addressed in a typical PCB design.

There are also many special rules for avoiding static charging and this way, ESD problems in manufacturing areas. These guidelines are not provided here.

10.4.1 ESD Prevention

The best countermeasure against ESD is to avoid ESD when possible. Three categories of potential effects related to ESD can be identified. It is useful to set priorities for prevention. In general, the following order of prevention priority should be followed:

1. Prevent charge injection into system circuitry.
2. Prevent problems due to transient fields generated by discharge currents.
3. Prevent electrostatic field problems.
4. Provide good (low impedant) ground connection for all systems

10.4.2 PCB Design Rules

The following guidelines are listed, in order of priority, for ESD problem prevention on PCB level. Please note that the appendix of this report discusses the foundations and merit of these rules::

1. Use ICs with appropriate robustness against ESD.
2. If sparks can reach the PCB it needs to be checked which electrical net the spark can hit and how the current flow path from this net to ground is.
3. Every signal at connectors that may receive ESD hits needs to have a filtering (for example a capacitor to ground) that is appropriate to absorb or reflect the ESD energy, but maintains signal integrity for the wanted signal.
4. Signal filters need to be placed as close as possible to the connector having ground connections as close as possible to the filter location.
5. If capacitors are used as ESD protection the consequence of non-linearity needs to be considered. This is mainly important for X7R and Y5V type ceramics and capacitor values $< 100\text{nF}$. Those capacitors will charge up to a voltage much greater than their nominal voltage if they receive for example, a 10 kV ESD discharge. This will reduce their capacitance momentarily such that their ESD protection effect is limited. X7R will lose 80 % of its capacitance if the voltage reaches twice the nominal voltage, Y5V will lose 80 % of its capacitance even at its rated voltage
6. Non-insulated chassis ground on the PCB must be separated from other traces by at least 2 mm. This applies to anything connected to chassis ground, as well as traces.
7. Chassis ground traces should have a length-to-width ratio of no more than 5:1.
8. Non-insulated electronics should kept at least 2 cm away from PCB areas that an operator can touch, or non-chassis grounded metallic objects that the operator can touch.
9. Power and ground traces should be kept one over the other on opposite PCB

layers.

10. Ground plane and ground traces must be connected to form a grid. There must be vertical ground lines connected to horizontal ground lines at least every 3 cm in either direction. Typically, on a double sided PCB, this means layer two may have vertical ground lines, layer one may have horizontal ground lines, and there must be a feedthrough at least every 3 cm to connect the two. Of course, connections at intervals of less than 3 cm are even better, and ground planes are better than ground grids.
11. All signal lines must be within 10 mm of a ground plane or line. The ground can either be on the same layer or the next layer above or below the signal line. If the signal line is 30 cm long or more, it must be directly beside a ground trace, or over a ground trace or plane on another PCB layer.
12. Bypass capacitors between power and ground must be no more than 4 cm apart.
13. Components with the most interconnects between them must be side-by-side, or end-to-end.
14. All components must be as close as possible to the I/O connector.
15. Fill all unused portions of the PCB with ground plane.
16. If possible, feed power or signals from the center of the PCB edge, not from the corner.
17. Long sections (30 cm or more) of especially sensitive signal lines should be transposed with their ground line.

10.4.3 Cable Design Rules

For cables and connectors also special rules can be applied. Many are general EMC rules. Please note that the appendix of this report discusses the foundations and merit of these rules:

1. Electric connections must use materials no more than 0,75 V apart from each other in electrochemical series.
2. The anodic (more positive) material must have a larger uncoated surface area than the uncoated surface of the cathodic material.
3. The shield material must be at least 0.025 mm thick. (100 percent coverage is preferred.)

The following rules take into account shielded cables that are not very common in automotive cable systems:

4. Use shielded cables and connect the shield only to chassis ground. The arc path from chassis to other pins must be at least 2 mm.
5. Connect the cable shield to chassis at both ends of the cable. A metallic connection is preferred, but a high frequency (capacitive) connection can be used if required to prevent a significant ground loop problem.

6. The cable shield must connect to the chassis within 2 cm of the cable entry/exit point, and the unshielded portion of the cable must be less than 2 cm.
7. Extra wires in the cable must be trimmed so they don't extend beyond the shield, or must be connected in parallel with the other lines.
8. A shield which is also a chassis ground path shouldn't normally go through a ferrite bead, and certainly not ferrite beads in common with other lines.
9. If ferrite beads are used, they should be at the receiver end of the cable.
10. If the shield can't be connected to chassis at one end of the cable, connect it to ground via a 4 nF, 1 kV ceramic capacitor. The provision for this capacitor should allow it to be an option.

10.4.4 Enclosure Design Rules

The following summary details enclosure design requirements necessary prevent ESD related problems. Please note that the appendix of this report discusses the foundations and merit of these rules::

1. The enclosure design must ensure that uninsulated electronic components and conductors have at least a 2 cm arcing distance from ungrounded metal objects that may be touched by the operator.
2. The enclosure design must ensure that uninsulated electronic components and lines are at least 2 mm away from any item connected to chassis ground.
3. The enclosure design must ensure that uninsulated electronic components and lines should have at least a 2 cm arcing distance from the operator, or that a chassis ground point/ area is between the operator and electronics.
4. The enclosure design should allow the electronic devices to be grouped together. (If possible, the I/O connector should be centrally located in order to minimize line lengths.)
5. The enclosure design must allow sufficient room for the PCB, so PCB design guidelines can be followed.
6. All shield materials should have an EMF within 0,75 V (in the electrochemical series) of the metal they connect to. If not, an intermediate metal connection device should be used.
7. All designs should make provision for the addition of further shielding concepts.
8. The above given distances can be reduced, when an insulating layer of appropriate size is used for avoiding arcing.
9. Connect all conducting parts (metals and metalized plastics) to ground
10. If a good ground connection of the conducting part cannot be guaranteed over the service life, the smallest gap from floating part should be over ground surface

The following specifications refer to shielding design against electromagnetic field coupling:

11. No slot seam or hole in the shield may have an opening dimension greater than 2 cm, unless the length-to-opening ratio of the hole is at least 5 to 1.
12. Seam gaps must have an overlap of at least five times the gap width.
13. If requirement 9 can't be met for shield seams, use conductive gaskets to fill the seam gaps, or use fasteners every 2 cm along the seam.
14. If several holes are required, the space between holes should equal the largest diameter of the hole.
15. Use several small openings instead of one large opening.
16. Do not place a shield hole near a point where the shield connects to chassis ground, or near sensitive devices or lines.
17. If foil tape is used, it must make electrical contact with the shield.
18. Keep bonding straps short and wide (less inductance).

10.4.5 System Design Rules

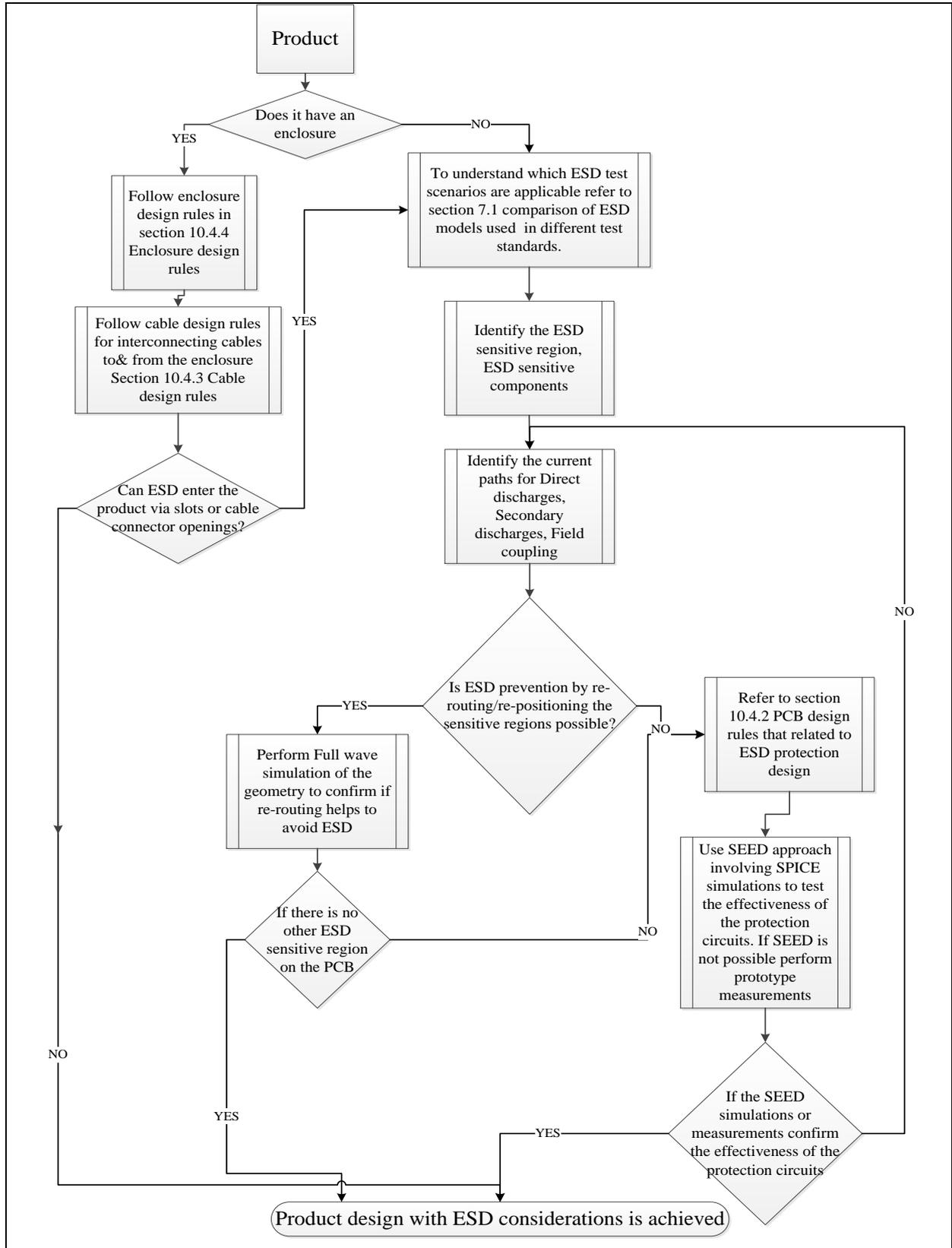
The following are ESD-related design practices that should be followed whenever possible. Please note that the appendix of this report discusses the foundations and merit of these rules:

1. No design should force a component to operate outside those levels which are specified by the vendor.
2. No design should result in a circuit that can disable itself indefinitely.
3. Use less sensitive and slower devices whenever possible.
4. Avoid extra ESD antennas, such as long reset lines.
5. Connect all floating inputs either high or low.
6. If ferrites are used for ESD problem prevention, follow these guidelines:
 - a. Put ferrites next to the "input" they are filtering (within 2.5 cm). (Ferrites for ESD should be on inputs, not outputs.) If the electronic components are shielded, then the cable input is the entry point into the shielded region.
 - b. No other component (except a connector) should exist between the ferrite and the input it is filtering.
 - c. Each input to be filtered normally should have its own ferrite bead. Common mode filtering normally is not good for ESD protection.
 - d. Use proper ferrite material.
 - e. Be careful with multiturn ferrites.
 - f. Don't let ferrites touch each other, or other PCB lines, or ground grids.
 - g. Design in ferrites only as an option.
7. Implement advanced ground contacts in every connector

10.4.6 Firmware/ Software Design Rules

1. All inputs should be double sampled, and the samples should be several microseconds apart.
2. Use parity and frame error checking whenever possible.
3. Integrate Watchdog circuits with appropriate checking intervals.
4. Refresh memory cells as often as possible, checking data and restore data.
5. Integrate powerful and robust error handling routines.

10.4.7 Flow Diagram for ESD Robust PCB Design



11 Proposal of Improved Testing and Design Methods

11.1 IC or Module Characterization by a TLP

The characterization should determine the failure thresholds of the components and modules. The characterization should be done on a suitable evaluation boards. Details should be defined in collaboration with the semiconductor industry. The recommendations of the Industry Council for System-Efficient ESD Design (SEED) [22] should be taken into account.

11.2 ESD System Simulation

It could be shown that system simulation of thermal failures is possible. Also simulation of other failure mechanisms seems to be possible. Based on ESD simulator, IC, and protection element models PCBs can be optimized to withstand ESD threats. With simulation, already in early design stages, ESD robustness can be ensured.

A systematic simulation based process, ensuring the needed ESD protection levels, should be established in industry in order to fulfill high quality demands of automotive electronics.

11.3 Test Methods for Trailer/ Vehicle Interfaces and Chassis Discharges

11.3.1 Theoretical Background

11.3.1.1 Trailer/ Vehicle Interfaces

Trailer ECUs and other electronic components directly connected to trailer connector can be compromised due to ESD coming from trailer. The trailer chassis can be electrically isolated from the vehicle. Trailer hitches do not ensure a low impedance ground connection. Even a ground wire connection of the trailer cable harness to the body might not be established. According to different physical effects and environmental conditions an electrostatic charging of trailer chassis is possible. A discharge from the trailer chassis to single wires of the cable harness is possible.

The crucial parameter of a trailer ESD is its capacitance. From physical point of view many trailers consists of a metallic base plate mounted on a chassis in parallel to the road. A qualitative analysis of dimensions governing the capacitance can be achieved applying a parallel plate capacitor assumption.

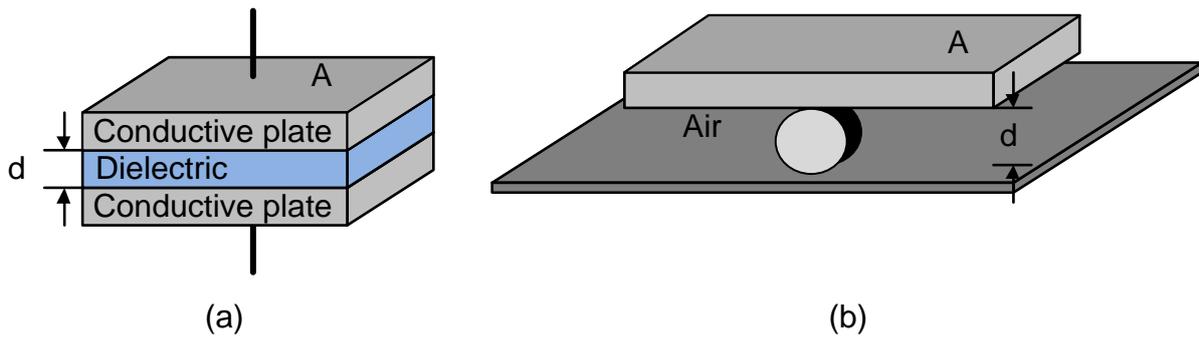


Figure 11.1: Parallel plate capacitor (a), trailer geometry (b)

If the capacitance increases with area A and decreases with separation of electrodes d an approximation is given by:

$$C_{Trailer} = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d} \quad 15$$

The trailer bottom is separated from the road by air ($\epsilon_r=1$, $\epsilon_0=8,854e-12$ F/m). According to STVO traffic regulations the maximal trailer dimensions are defined with maximum overall length and width for passenger car and truck trailers. Maximum trailer dimensions are given in Table 11.1.

Vehicle type	Width [m]	Length [m]
Passenger car	2.50	8 (4 m car length)
Truck (semi-trailer)	2.55	13.68

Table 11.1: Trailer dimensions

Figure 11.2 shows the calculated trailer capacitance as a function of the distance between the road and the trailer bottom.

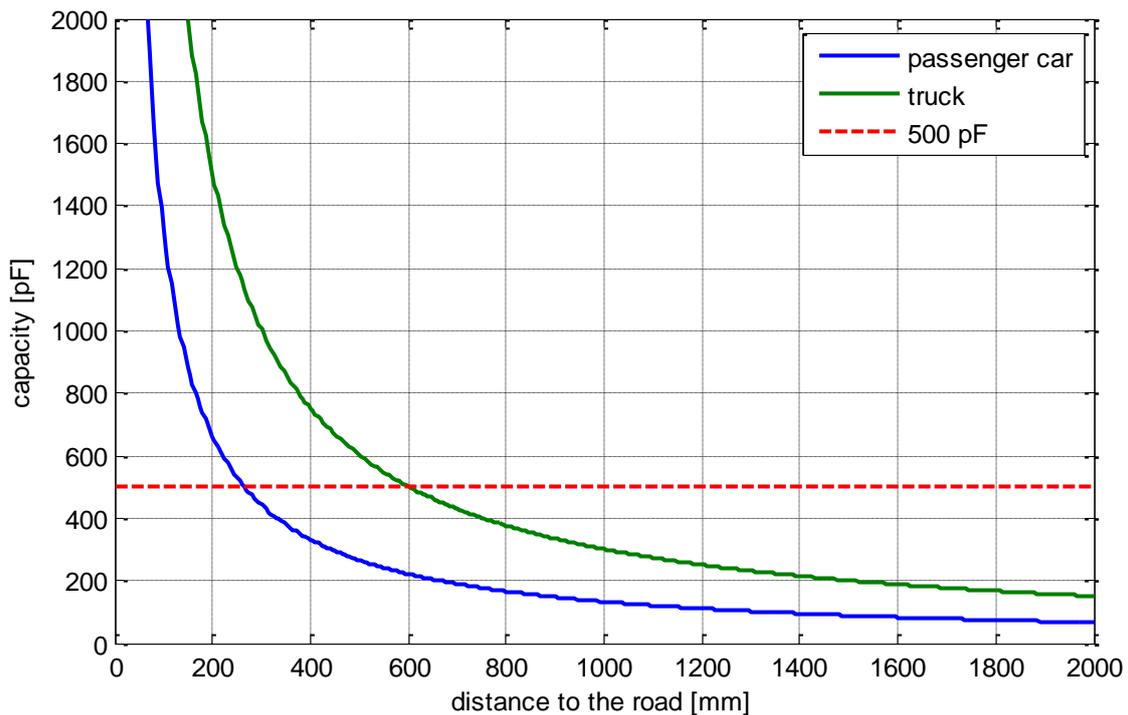


Figure 11.2: Trailer capacitance depending on the distance between trailer bottom plane and the road

A capacitance of about 500 pF is obtained for a passenger car setup. In case of a truck trailer the capacitance can exceed 1 nF.

11.3.1.2 Chassis Discharge

Because of constructional details some chassis parts like an axle may be mounted electrically isolated from the vehicle body. According to different physical effects and environmental conditions an electrostatic charge of the axle can occur. A discharge between axle and surrounding cables or electronic components is possible. Particularly wheel speed sensors (used e.g. for anti-lock braking system) are located close to the axle and can be exposed to ESD.

A threat may be assessed by estimation of the axle capacitance. From physical point of view an axle consists of a metallic enclosure mounted on a chassis in parallel to the road. A qualitative analysis of capacitance regarding dimensions can be achieved applying a wire parallel to a wall capacitor model (Figure 11.3).

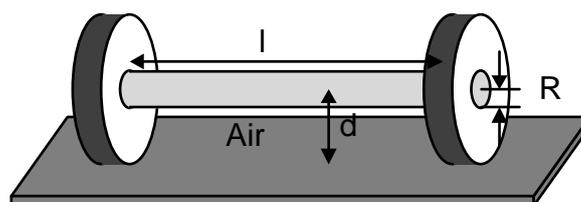


Figure 11.3: Chassis geometry

An approximation for that configuration is given by:

$$C_{axle} = \frac{2 \cdot \pi \cdot \epsilon \cdot l}{\operatorname{arcosh}\left(\frac{d}{R}\right)} \quad 16$$

where l is the axle length, R its radius and d the distance to the ground. The axle is separated from the road by air ($\epsilon_r=1$, $\epsilon_0=8,854e-12$ F/m). Considering a truck axle a length of 2 m and a radius of about 0,2 m appear realistic. Figure 11.4 shows the calculated capacity as a function of the distance between the road and the axle center. For a common trailer setup capacitance below 150 pF is obtained. If capacitance of other chassis parts is of interest, the parameters in equation 16 have to be adjusted.

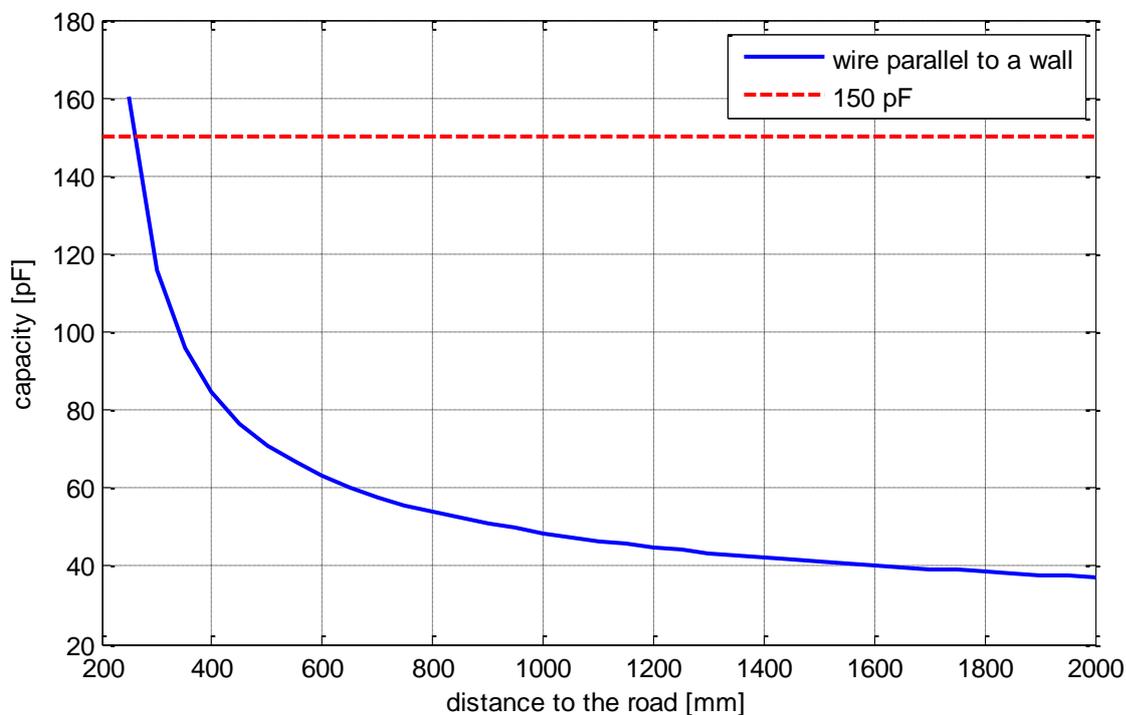


Figure 11.4: Axle capacitance depending on the distance between axle center and the road

11.3.2 Proposal for Test Method

11.3.2.1 Modified Generator

A low cost option to provide more appropriate test results may be achieved by modifying an IEC ESD generator similar to the test method for airbag squibs discussed in Section 4.3.1. According to calculated results, energy storage capacitor of 500 pF represents well a severe case for a conventional trailer and a capacitor of 150 pF a severe case for charged axle. Both trailer and a chassis parts are metallic devices with low serial resistance. To prevent damages of ESD generator relays a discharge resistor of around 100 Ω should be used. Such discharge networks are available for most ESD generators.

11.3.2.2 Test Procedure for Trailer/ Vehicle Interface

A set up according to ISO 10605 should be used as specified for vehicle tests on external points.

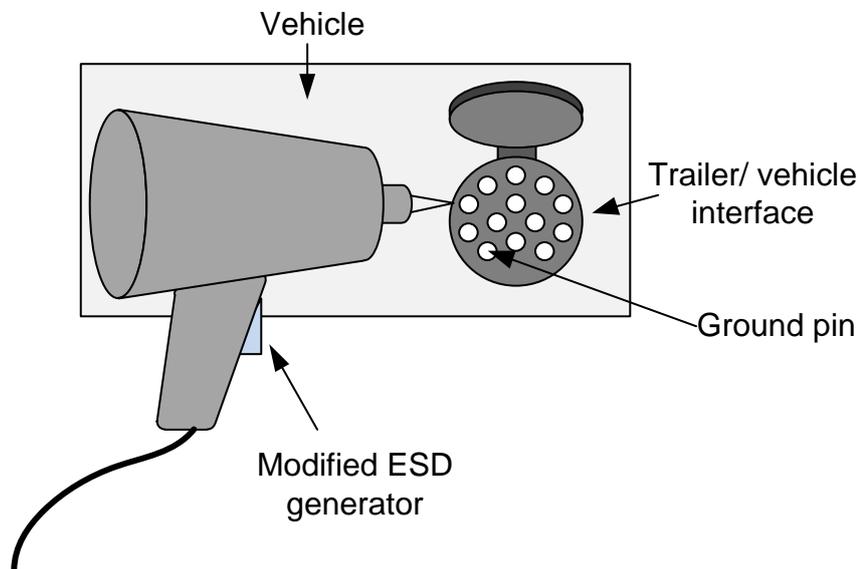


Figure 11.5: Test set up for trailer/ vehicle interface

The following exceptions apply:

- ESD generator discharge network has to be modified.
- The ESD generator has to be operated in contact discharge mode.
- All pins of the trailer socket have to be tested

Voltage test levels according to ISO 10605 could be appropriate.

11.3.2.3 Test Procedure for Chassis Discharges

A set up according to ISO 10605 should be used as specified for the component level.

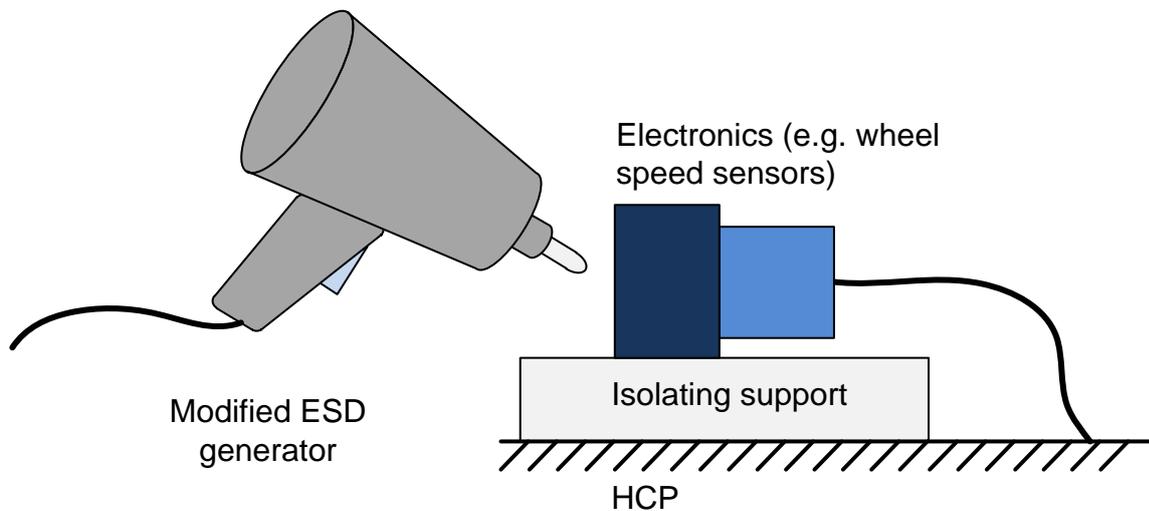


Figure 11.6: Test set up for axle discharges on wheel sensors

The following exceptions apply:

- The ESD generator has to be used in air discharge mode.
- An isolating supply has to be used.
- The sensor unit has to be connected to wires having a length of 1 up to 5 m. The original connectors and cables should be used and shorted, when needed.
- All wires have to be connected at the end to ground.

The electronics to be tested (e.g. wheel speed sensors) should be placed on an isolating support and connected to the HCP. The tip of the ESD-generator has to be moved slowly ($< 10 \text{ mm/s}$) above the sensing surface. Care has to be taken that the voltage is kept constant during the test. Packaging and handling voltage levels could be appropriate.

11.4 Cable Discharge Test

11.4.1 Theoretical Background

During automotive manufacturing process electronic systems are often affected by Cable Discharge Events (CDE), when numerous cables are connected to electronic devices. In contrast to an IEC discharge up to five times faster rise times can be observed. Figure 11.7 compares the energy on a 260 Ω DUT for a cable discharge and an IEC discharge estimated by equations 10 and 13. A 5 m, 260 Ω cable has comparable energy to an IEC generator.

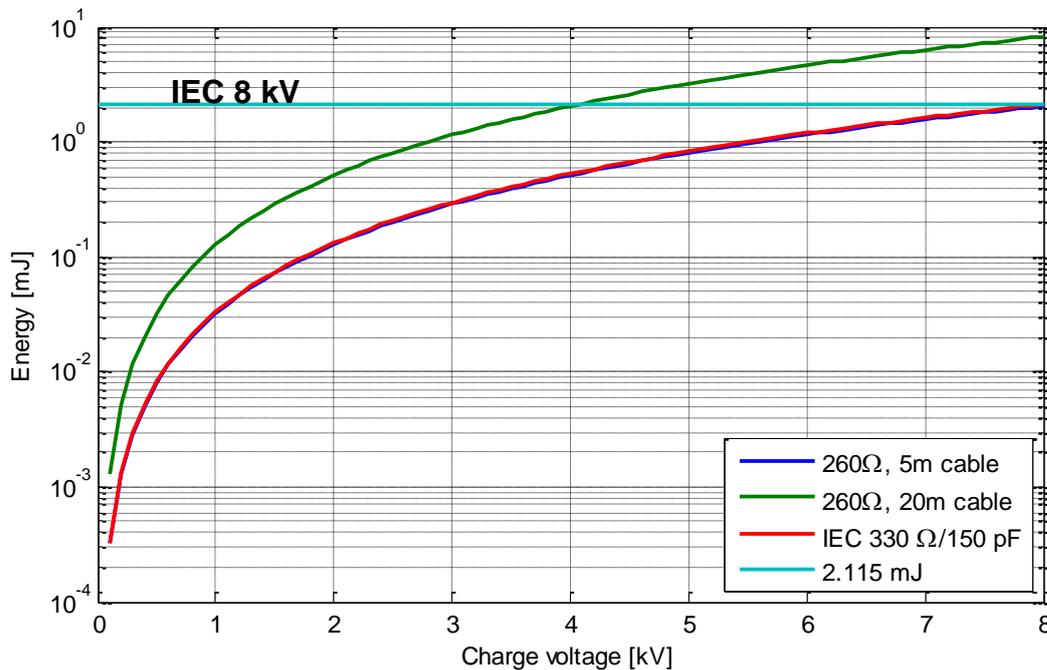


Figure 11.7: Energy of cable discharges (260 Ω impedance) over charge voltage compared to an IEC discharge on 260 Ω DUT

11.4.2 Cable Discharge Generator

Cable discharge generator should be realized on a PCB. A 25 mm discharge tip with a spring has to be connected at one end of the trace. The connection to a HV is established by a socket. A 100 MΩ charge resistor should be assembled either on the PCB or externally. The trace should be 35 μm thick, 5 mm wide and 5 m long. Rectangular routing of the trace has to be avoided. Meander-shaped routing could be appropriate.

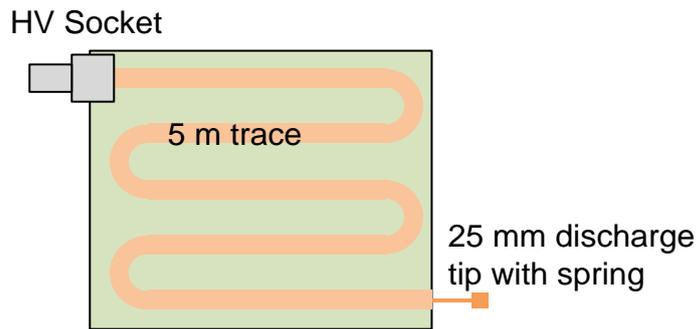


Figure 11.8: Proposal for a cable discharge generator

11.4.3 Test Procedure

The device to be tested has to be placed on HCP. DUTs ground connection to HCP has to be established. The cable discharge generator can be mounted on a robot or placed on a styrofoam block. A robot makes an automated test possible. Height over the HCP has to be $50 \text{ mm} \pm 10 \%$, to establish 260Ω impedance. The discharge is triggered by moving the generator PCB, such the discharge tip hits the selected DUT pin. Height of DUT should be varied using appropriate supports. The HV source has to be capable for 8 kV.

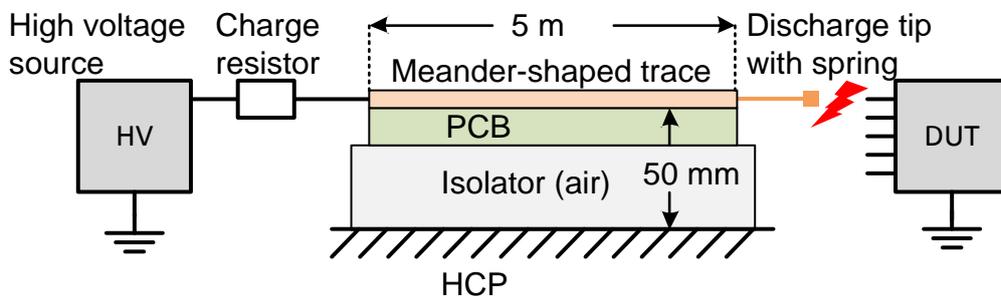


Figure 11.9: Test set up for cable discharges

Powered and unpowered DUT immunity to cable discharge can be tested. Voltage test levels according to ISO 10605 could be appropriate.

11.5 Test Method for Insulation Resistance of Switches

11.5.1 Theoretical Background

Electronic components can be compromised due to ESD also after assembly. In many cases a discharge will not happen directly close to the component. More likely it is that the attached cables will lead a discharge current from distant locations into the component. Critical can be cables connected to switches or other operating units. Discharge currents from humans can flow through slots and holes via the arc to attached cables. Paschen's law can provide a first estimation for critical distances. In Figure 11.10 the minimum arc length is given over the voltage. Edges and tips can prolong the arc length significantly.

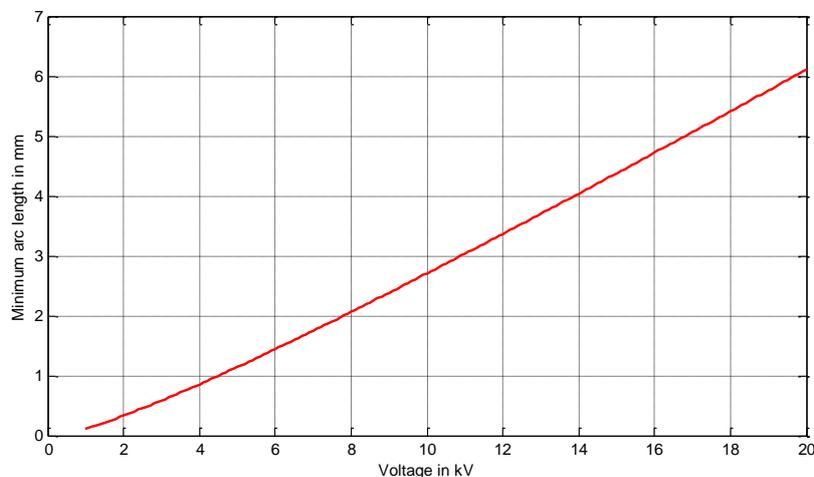


Figure 11.10: Minimum arc length according to Paschen's law for normal conditions in air

Figure 11.10 shows a critical configuration. Current can flow through attached cables into an attached control unit.

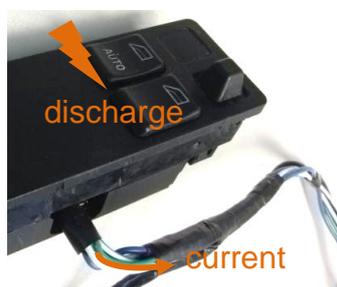


Figure 11.11: Switches with attached cables

In order to prevent critical currents high voltage isolation between the parts that can be touched, and the cables connecting the electronic components, are needed. Isolation can be realized with large distances or isolating material protecting slots and holes in operating units.

Effectiveness of isolation must be checked with proper test procedures.

11.5.2 Test Procedure

A set up according to ISO 10605 should be used as specified for the component level.

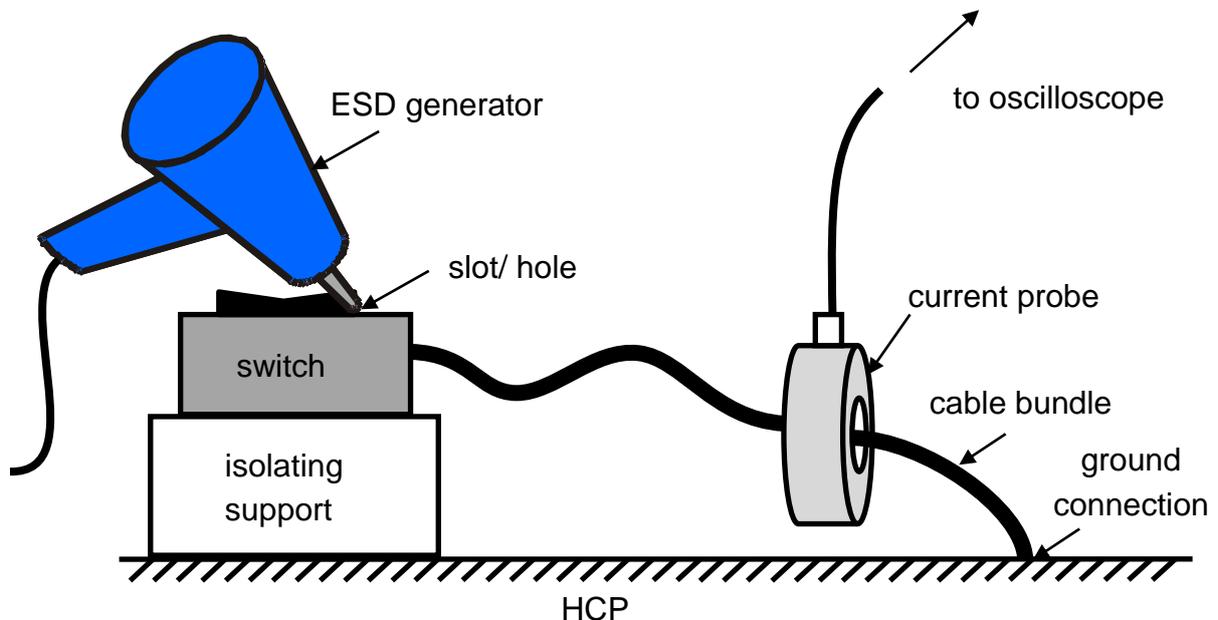


Figure 11.12: Test set up for switches

The following exceptions apply:

- The ESD generator has to be used in air discharge mode.
- An isolating supply has to be used.
- The switching unit has to be connected to wires having a length of 200 up to 400 mm. The original connectors and cables should be used and shorted, when needed.
- All wires have to be connected at the end connected to the current probe or to ground, when an inductive probe is used.
- It might be necessary to assemble the switching unit in an isolating holder. In this case care has to be taken that the holder does not affect the test results.

The switch to be tested should be placed on an isolating support and connected to the current probe (or directly the HCP). The ESD-generator has to be operated in air discharge mode. Voltage has to be adjusted to +25 kV. All areas that can be touched by vehicle users must be tested. The tip of the ESD-generator has to be moved slowly (< 10 mm/s) above the surface. Care has to be taken that the voltage is kept constant during the test. The test has to be repeated with -25 kV charge voltage.

The test is passed, when the current flowing through the current sensor is below 2 A during the complete test procedure.

11.5.3 Current Sensors

Current flowing through the cable bundle must be measured. Several methods can be applied. Either an inductive current probe with bandwidth of more than 200 MHz like the Fischer Custom Communications F-65 or a shunt current probe can be used. Shunt current probes should have a resistance between 1 and 2 Ω . A current sensor according to IEC 61000-4-2 is preferable. Alternatively, a simple coaxial current probe can be assembled according to Figure 11.13. At least 5 composite carbon resistors should be used in parallel in order to reduce inductance. Wires should be as short as possible. The current sensor should be connected through an attenuator to an oscilloscope with a bandwidth of at least 300 MHz.

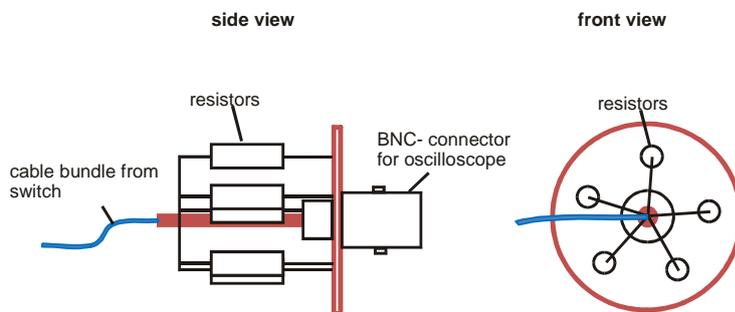


Figure 11.13: Simple current sensor

11.6 TLP Testing Method on System-Level

TLP testing is used as an ESD characterization tool to obtain IC's voltage-current pulse parameters, failure levels, and ESD metrics. A testing method on component level is described by ESD-Association in [99]. However, no classification on voltage levels is done. There are four fundamental TLP methodologies:

- Current source TLP
- Time Domain Reflectometer TLP
- Time Domain Transmission TLP
- Time Domain Reflection and Transmission TLP

Figure 11.14 shows the current source TLP setup. This setup may be adopted for system level ESD testing. The voltage, current and energy may be increased by removing the 500 Ω serial and 50 Ω termination impedances. An IEC stress pulse duration is about 100 ns, its rise time is less than 1 ns. Most of commercial TLPs support this or similar parameters. However, faster rise time and larger pulse width will make the test more severe.

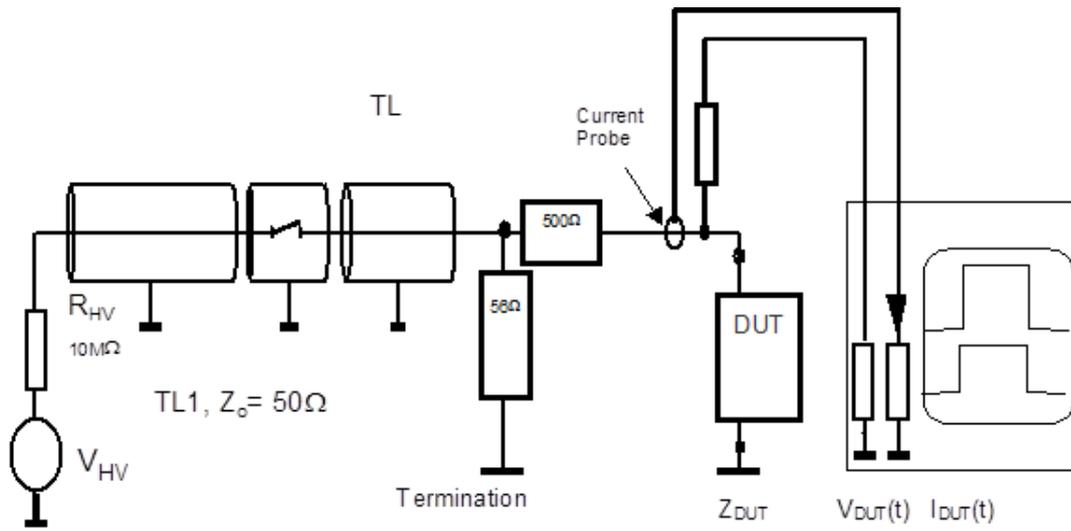


Figure 11.14: Current source TLP [99]

A set up according to ISO 10605 should be used as specified for electronic modules.

11.7 Investigation into ISO 10605 2nd. Ed. Optional test set-up: Indirect discharges

11.7.1 Background

In automotive ESD testing a cable harness connects the DUT and the peripheral or support equipment. ESD will initiate waves traveling on the metallic surfaces which couple to the harness. The effect of such coupling can be tested using the ISO “Rinne” which has been analyzed. In this study the voltage induced on one end of the cable (Field coupling plane end) due to ESD discharge on the field coupling strip is measured and compared to different models. The other end of the cable is terminated with 50Ω . The results are compared to simulation and it is deduced that a TLP test can approximate the input voltage at the DUT.

11.7.2 Test Setup

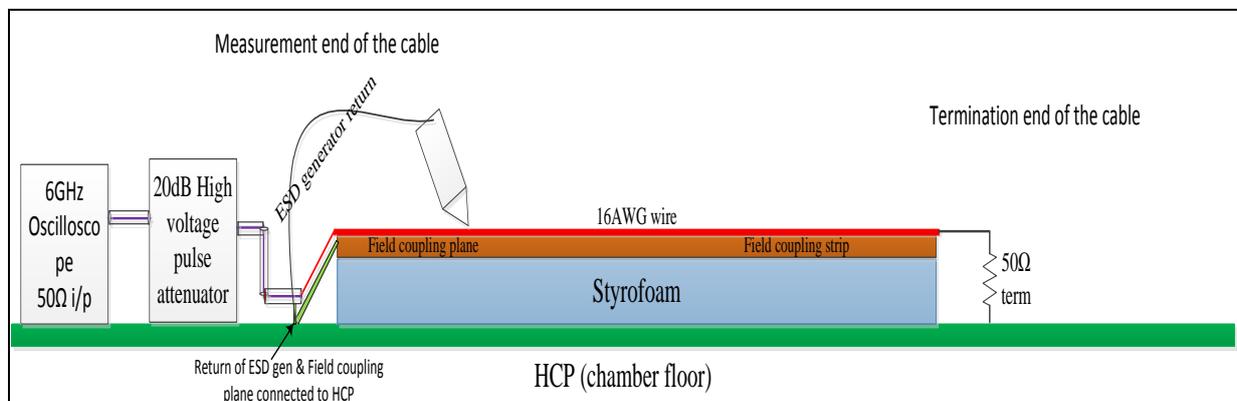


Figure 11.1: Test setup

- As per (ISO 10605) the test setup consists of a Horizontal coupling plane (HCP), a field coupling plane along with a field coupling strip, the DUT and the cable harness. In the measurement setup shown in the Figure 1, instead of using a DUT, a port is defined on this end of the cable and the coupled voltage on the cable due to ESD discharges on the field coupling strip is measured by a 50Ω system. The other end of the cable is terminated with 50Ω to the HCP.
- The measurement setup has been setup inside an anechoic chamber, only with the intention of using the chamber floor as the Horizontal coupling plane (HCP). The pictures of the measurement setup are shown in the Figure 2
- A 16 AWG wire is used as the test cable. The field coupling plane and the field coupling strip are made of a brass sheet conforming to the dimensions provided in the ISO 10605 standard document.
- The field coupling plane and the field coupling strip are elevated 5cm above the HCP using Styrofoam.

- On the measurement end of the cable, the field coupling plane is bent to allow good electrical connection with the HCP. The ESD generator is referenced to this point on the HCP.
- The voltage on the cable is measured using a 4GHz 50Ω oscilloscope. (Figure 2b)
- A 20dB high voltage pulse attenuator is connected between the cable and the oscilloscope. The attenuator also serves as protection against overvoltage.

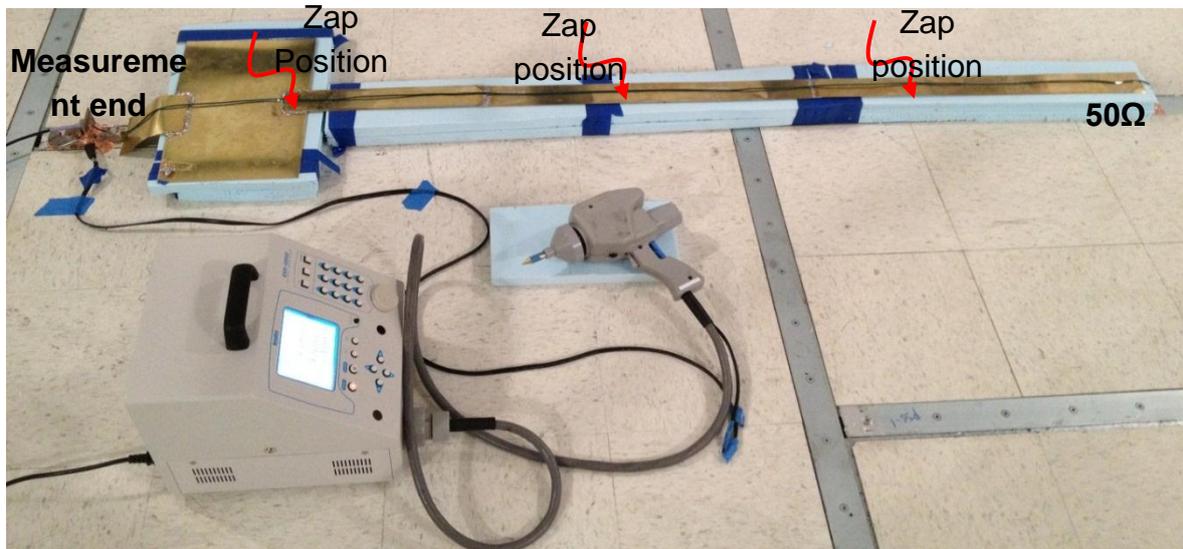


Figure 11.2: Test setup

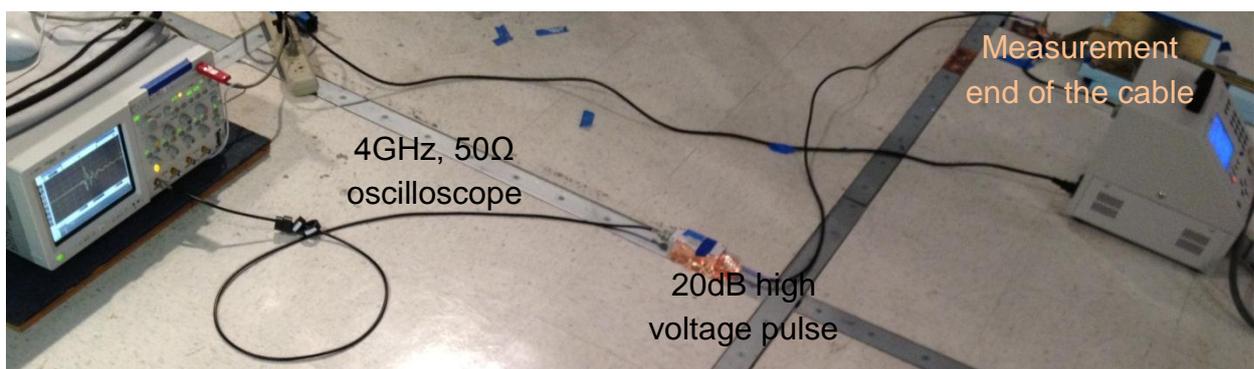


Figure 11.3: Measurement end of the test setup

11.7.3 Verification of ESD Generator Current Waveform

- To verify the functionality of the ESD generator its output waveform has been captured using an F-65 current clamp. The ESD generator is discharged into the HCP at 1kV charge setting. Both a Noiseken and a Teseq ESD generator have been used.

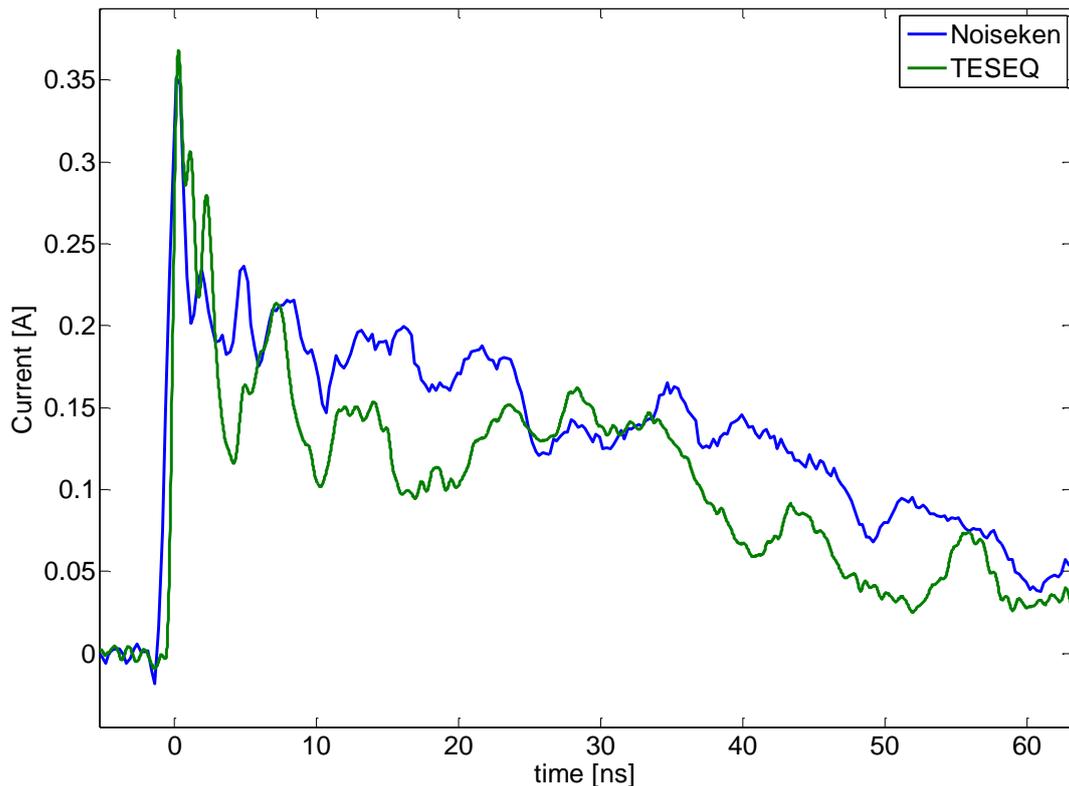


Figure 11.4: Discharge tip current waveforms of the Noiseken and the Teseq ESD generators

11.7.4 Coupled Voltage Measurement

The Noiseken ESD generator is set to 1kV and discharges are applied at 3 different locations along the field coupling strip. The results are shown in Figure 5.

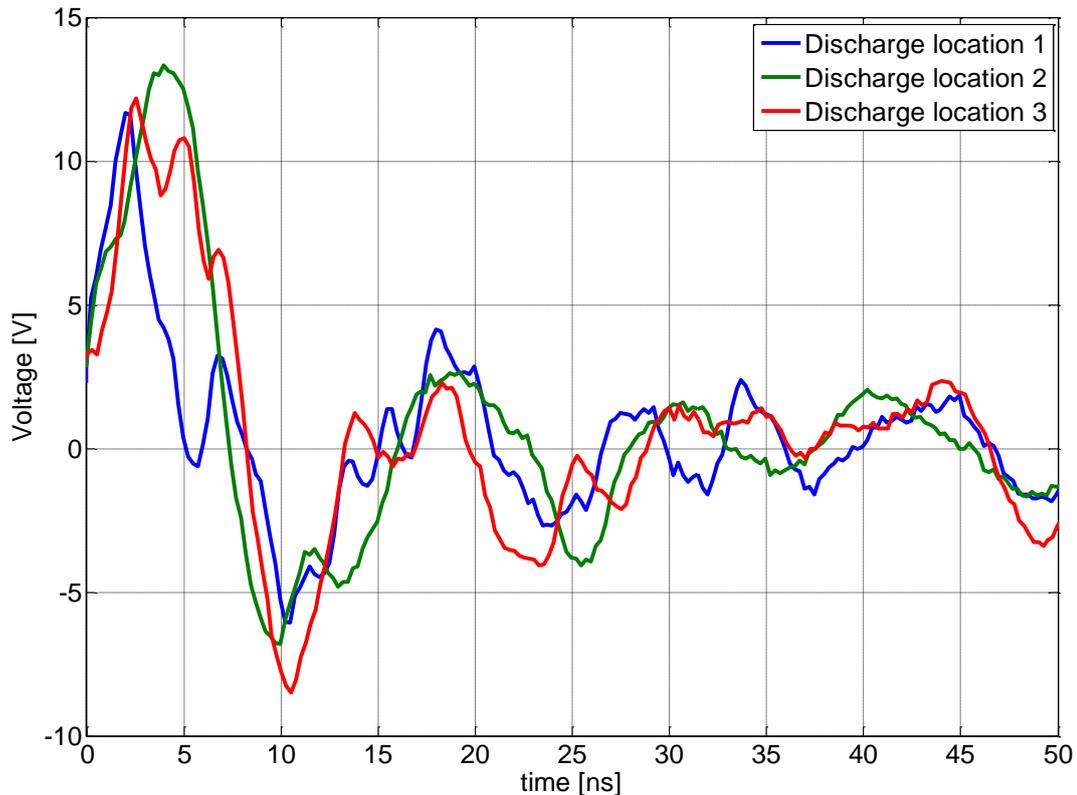


Figure 11.5: Induced voltage for three different discharge locations

The waveform in the Figure 5 is dominated by a wave traveling on the coupling strip which couples to the wire harness. The periodicity of about 12ns is caused by the length of the test structure. The magnitude will depend on the distance of the wire to the coupling strip, on the type of wires, the number of wires in the harness etc. In this experiment, about 12.5V has been induced into the 50 Ohm load for 1kV charging voltage. There is no DC path from the coupling strip to the wire harness; the coupling is via capacitive and inductive means. Although the value of the coupled voltage will depend on the wire geometry results from this geometry are used as guidance to compare to simulations and to compare the ISO-Rinne setup with a direct TLP injection.

11.7.5 SPICE Simulation of the TLP Test Setup

The SPICE simulation uses a transmission line pulser as substitute for the ISO Rinne setup. It creates a TLP voltage that can be directly injected into the DUT. It causes approximately the same voltage and current at the DUT.

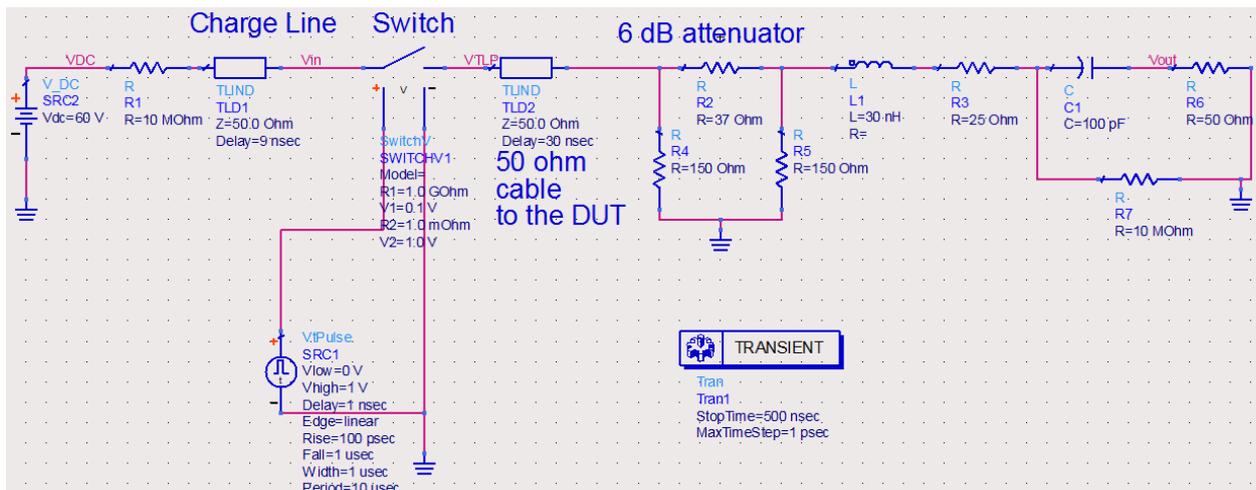


Figure 11.6: SPICE simulation model of the TLP test setup

- The set up shown in the Figure 6 has a Transmission line pulser circuit consisting of a 50 ohm charge line, charged by a DC voltage source via a 10 MΩ resistor. The TLP charge voltage is increased by 60 V for every 1kV of ESD charge voltage. Thus, to emulate a 1kV ESD discharge the TLP is set to 60V
- The charge line length should be 6ns to ensure a repeat rate of 12ns
- The cable connection from the TLP to the input of the DUT should be kept short. A 30nH inductance is used to emulate a 5cm real connection.
- The TLP is coupled to the DUT using a 100pF and 25 Ohm in series connected capacitor. The capacitor value is derived from the coupling capacitance between the cable harness and the coupling strip.
- A 6 dB attenuator is used to reduce reverse reflections into the TLP and to allow the charge voltage setting at the TLP to be larger.

11.7.6 Comparison between the SPICE Simulation and the Measured Data

The SPICE simulation is compared to the measured voltages for discharges at different locations. The voltage waveform induced by the TLP approximates the measured waveforms as shown in the following figure.

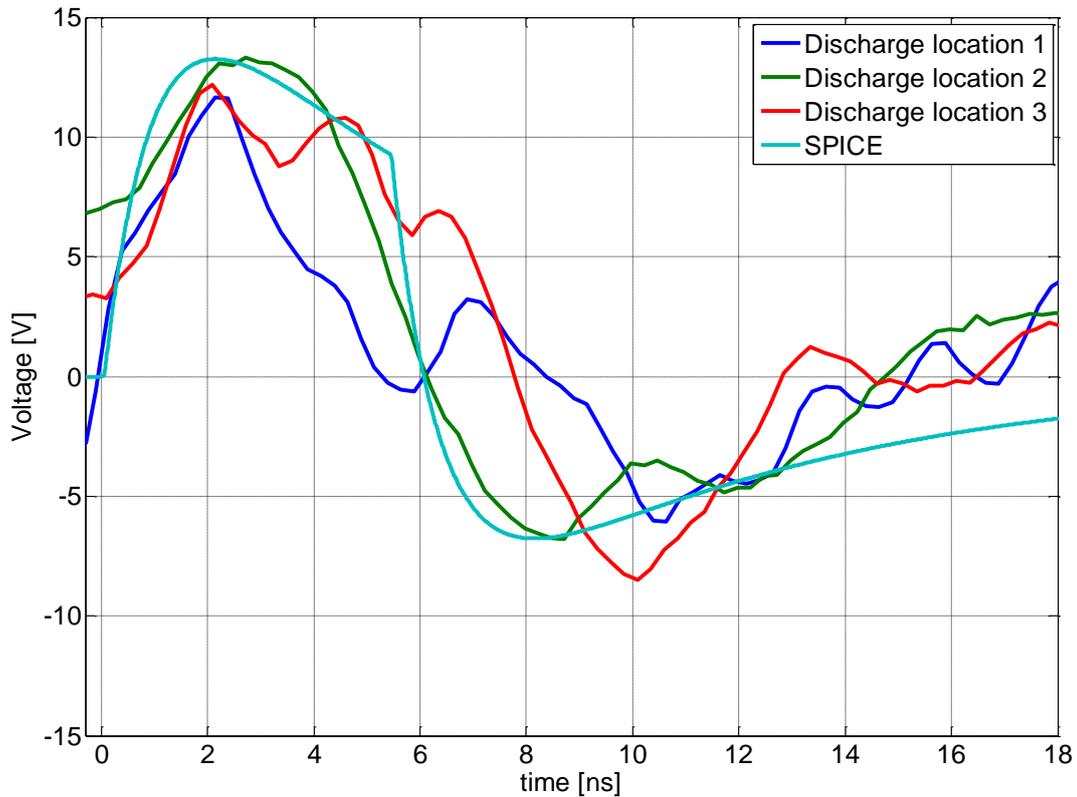


Figure 11.7: Measured voltages at different discharge locations vs. SPICE simulated voltage (data is time shifted)

As a second modeling method a full wave simulation model has been created. Its main properties are:

- The full wave model of the ISO Rinne test setup is created in CST. All the dimensions of the field coupling plane and the field coupling strip conform to the dimensions given in the standard ISO 10605
- A time domain solver is used between the frequencies 30MHz to 3GHz which accommodates the 850ps rise time of the ESD generator discharge waveform.

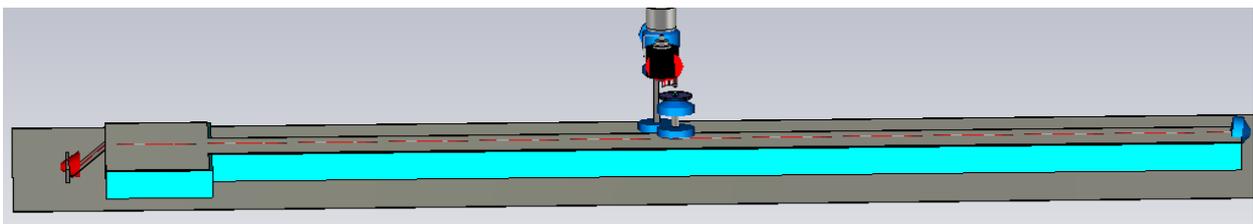


Figure 11.8: CST full wave model of the ISO Rinne test setup

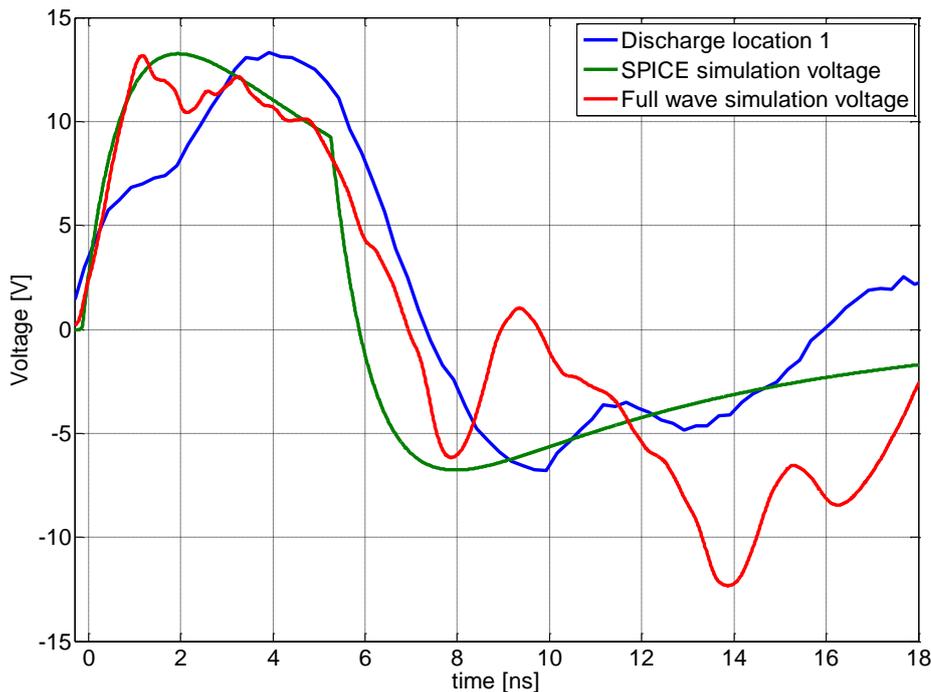


Figure 11.9: Comparison between measurement, SPICE and full wave simulation

The dominating parameters of the simulation results match to the measurements and the SPICE simulation. A further refinement of the simulation does not seem warranted as the coupling in the real measurement will be strongly influenced by the type of cable bundle used and the termination conditions at the DUT and support equipment side of the cable bundle.

11.7.7 Conclusions

The ISO Rinne test setup is inducing a voltage on the cable bundle by coupling between the bundle and a traveling wave which is initiated by the ESD discharge. A voltage ratio of about 1:100 was observed relating the induced voltage to the ESD generator charge voltage. Similar voltages can be achieved by using a transmission line pulser via a capacitive-resistive coupling network. The main difference to the ISO test setup and the TLP injection is that the ISO test setup allows to operate the DUT while testing, while the direct injection would only allow to test for destruction as it would be an off-line test.

12 Conclusions/ Summary

High voltage pulses in automobiles were analyzed intensively based on the example of the special pulse source ESD. The current status of the literature was summarized and field problems were collected and described. With a newly developed simulation approach several ESD models were created. The simulation approach and the models were used to answer several important questions regarding high voltage pulses. Field problems were analyzed and the root cause could be found in most cases. Improved test methods might be required to increase the robustness against possible ESD events. The test methods were developed and are described in detail.

It has been shown that based on simulation many ESD problems can be detected early in the design phase. The initiated efforts should be continued in order to reach a more complete and accurate simulation based ESD design process soon.

12.1 Analyzed Field Problems

In section 4.3 ESD failures identified from literature were described. Individual failure mechanisms for published case studies were briefly summarized. It was shown that in some cases a failure could not be detected with common system level or IC level ESD test methods. This high diversity of ESD failures was confirmed in analysis of field problems provided by FAT members.

For studies on devices where a victim IC was known and characterized, robustness levels to different testing methods are compared in Table 12.1. A representative input of an automotive IC was used as a victim IC for antenna structure discharge. A BAW156 diode was destructed in a trailer ECU. A LED was affected in a rear light assembly. TLP and IEC level robustness have been simulated and verified by measurement. HBM level is simulated using the model described in 7.3.1. Only the energy based failures have been considered.

	IEC Network: 150 pF/330 Ω	TLP width: 100 ns rise time: 1.2 ns	HBM Network: 100 pF/1.5 kΩ
Diode BAW156	3 kV	350 V	5.5 kV
LED	6 kV	550 V	13
Automotive IC input	5.5 kV	450 kV	11.45

Table 12.1: Energy based robustness levels of ICs for different ESD testing methods¹

¹ For other investigated components not enough samples were available for different tests or characterization.

As it can be observed all ICs have more than 2 kV IEC system and 4 kV HBM IC ESD robustness level.

Often ESD failures could be prevented obeying general design rules presented in section 10.4. The next sections summarize failure mechanisms of the case studies. Design rules which could at least minimize probability of ESD failure are assigned.

12.1.1 Trailer ECU

Failure mechanism of the trailer ECU can be referred to its impaired grounding connection. Because of ECU design a capacitive current coupling from the ground plane to the victim diode branch was observed. The ESD Prevention Rule:

4. Provide good (low impedant) ground connection for all systems

could help prevent ESD damages. Often metallic body components are exchanged by plastic parts. This might prevent short grounding in some cases. ECU ground connection has to be made by cables of increased length and this leads to inductive decoupling from the vehicle body. ESD can follow a way through electronics and cause considerable damage. To consider the impact of grounding on ESD tests artificial vehicle network boxes, known from EMC testing could be adopted for ESD system level test as well.

12.1.2 LED Rear Light

Electrostatic charging of automotive parts as a result of triboelectric effect is widely spread in field and in automotive production lines. An increased application of plastic heightens achievable voltages. In general, both conducting and dielectric parts may be affected. Charged dielectrics may cause redistribution of electrical charge in floating conducting parts by electrostatic induction. As it was shown in the study an ESD event of the conducting object itself was triggered either when plugging e.g., a charged PCB or when exceeding the sparking voltage e.g., between a metalized floating part and a PCB.

The ESD prevention rule

1. Prevent charge injection into system circuitry

could eliminate the effect of electrostatic induction. A practical realization is only possible to a limited extent. It involves substantial costs. In general, an ESD threat may be minimized by grounding of all conducting surfaces both metals and metalized plastics. Following enclosure design rules:

3. The enclosure design must ensure that uninsulated electronic components and lines should have at least a 2 cm arcing distance from the operator, or that a chassis ground point/ area is between the operator and electronics.
9. Connect all conducting parts (metals and metalized plastics) to ground

10. If a good ground connection of the conducting part cannot be guaranteed over the service life, the smallest gap from floating part should be over ground surface

sensitive electronics will be safeguard. Rule 10 may be obeyed in a constructional way. ESD voltage is assigned by the smallest gap from floating conducting parts to a PCB of the ECU. For all measures the discharge path should be realized by a distinct ground contact, such as conducting fixations. Spiky geometry of discharge contacts ensures field enhancement.

The system design rule:

7. Implement advanced ground contacts in every connector will safeguard the electronics when plugging the LED rear light to wiring harness in case of a charged PCB due to electrostatic induction.

12.1.3 Rear Window Antennas

The antenna amplifier IC may be exposed to ESD in different ways. For example, a person might directly touch the antenna structure, or, during polishing the window surface will accumulate charges which induced charges in the antenna structure. This may also result in an ESD event. The study showed that no thermal failure occurred as a result of the ESD. Simulations showed high voltage and current amplitudes after polishing. Depending on the amplifier-IC used these may damage the IC. Damages of the amplifier-IC may be prevented following the PCB Design Rule:

3. Every signal at connectors that may receive ESD hits needs to have a filtering (for example a capacitor to ground) that is appropriate to absorb or reflect the ESD energy, but maintains signal integrity for the wanted signal.

RF signals are received by the antenna, this limits the choice of protection methods. As presented in sections 10.1, 10.2, and 10.3, frequency selective filtering may result in a conflict with the wanted signal. A nonlinear shunt element with low parasitic capacitance and appropriate breakdown voltage is a good solution. Table 14.1-Table 14.4 may be used to select an appropriate protection element on the basis of its measured parameters.

12.1.4 Knock Sensor and cable discharge

The investigation of a knock sensor induced ESD problem reiterated the known large diversity of ESD scenario. Due to its physical structure and the usage of piezoelectric materials, knock sensor's charging can be caused by heating or cooling of the devices or by mechanical force on the housing. ESD failure may occur during assembly. The knock sensor can charge the connected cable harness. When electronic devices connect the cable harness or a ground connection of a charged

device is established an ESD event may take place. Here the discharge of the piezo capacitance poses a larger risk than the discharge of its capacitance to ground.

Following ESD Prevention rule:

1. Prevent charge injection into system circuitry.

ESD failure could be prevented, e.g. by providing a high ohmic discharge path within the sensor. This measure will eliminate the charge and maintain signal integrity. At the same time the rule:

3. Every signal at connectors that may receive ESD hits needs to have a filtering (for example a capacitor to ground) that is appropriate to absorb or reflect the ESD energy, but maintains signal integrity for the wanted signal.

will prevent failures on the victim ECUs. Care has to be taken when selecting the protection element, because of the fast rise time of a cable discharge. Parasitic inductances can make filters inefficient. Table 14.1-Table 14.4 may be used to select an appropriate protection element on the basis of its measured parameters.

The system design rule:

7. Implement advanced ground contacts in every connector

solves the problem only to a limited extend. It will only ensure a harmless discharge of the charges between ground and the piezo assembly but it cannot discharge the charges that are stored inside the piezo element. This case study has shown a need of a cable discharge test on system level.

12.1.5 PCB Structure enclosed by enclosure

As discussed in section 8.4 the enclosures define the entry points for ESD. A metallic enclosure will not allow ESD currents or fields to penetrate through its metallic walls. The currents will flow on the surface and guide the fields. At apertures, slots or other imperfections of the metallic enclosure the ESD current will flow into the enclosure and spread on the PCBs and the inside of the enclosure.

The other entry paths are cables entering the enclosure. A shielded cable will guide the ESD current on the outside of its metallic shield layer. Upon reaching the enclosure the current will only flow in a harmless way to the outside of the enclosure if the shield is very well connected to the enclosure. The simulations have shown that even a small connection inductance such as 2nH will allow a large amount of energy to penetrate into the enclosure at the cable entry point. For example, if an ESD is applied to the connector shell at 8kV, causing a current pulse of 20A and is rising in about 1ns a voltage of 40 V will be induced across the 2nH connection. This voltage will be visible on the inside of the enclosure between the PCB and the enclosure driving a current often sufficient to cause upsets or other soft errors. The simulation results emphasis the importance of ESD filtering, overvoltage protection and shield

connections directly at the enclosure entry point, such that the ESD current can be shunted to the enclosure wall. Even a small interconnect inductance strongly increases the risk of upset problems of the electronics.

The second aspect revealed by both simulations is the importance of resonances. The enclosures, their openings and all cables form resonant structures. ESD can excite these resonant structures causing high amplitude voltages and currents.

The final aspect relates to non conductive enclosures. Those will not guide the ESD current and no discharges are possible to the enclosure. However, even small openings in the enclosures, as they typically exist at interfaces, will allow ESD sparks to penetrate into the enclosure. To avoid discharges to the PCB a distance of 1kV/mm up to 10 kV and 1.3 kV/mm above 10 kV should be kept. None conductive enclosures also carry the risk of upset errors by field coupling as they do not provide any shielding against electromagnetic fields.

12.1.6 Remote Key Antenna

The impact of both direct and indirect ESD on the remote key fob was investigated.

A full wave model of the ESD critical sections of a remote key fob PCB was created. The key elements of the model are the loop antenna, the transmitter IC connected to the antenna and the impedance matching circuitry. Different ESD mechanisms have been investigated, this includes, direct discharges to the loop antenna and field coupling to the antenna due to a nearby ESD. As output variables we selected the voltages at the IC input pin and the Vcc as they form typical entry paths into the IC. Similar to the IEC 61000-4-2 contact mode waveform, a test voltage of 10kV with a rise time of 0.85ns is used for these simulations. A set of basic protection schemes were also evaluated using full wave and SPICE simulations.

Direct discharge:

Direct discharges to the antenna were simulated under two different conditions. In the first case it was assumed there is no ESD protection on the output pin and a low value decoupling capacitor is placed on the Vcc pin. The second case includes a protection diode on the input pin and assumes a higher value decoupling capacitor on the Vcc pin. The voltage swings in both the cases are listed in the table 12.2. It can be observed that even with a diode having 1Ω dynamic resistance, a voltage of -15V is induced which may be enough to damage the IC, or to cause latch up or changes in the data stored in memory. Hence prevention of the discharge by designing the plastic accordingly is needed to avoid any discharges to the antenna. Further, it needs to be known how the IC reacts to strong noise pulses on its pins. More specifically, it needs to be determined that the IC will not latch up, be destroyed or loose memory information for the noise levels that can be induced on the pins even if direct discharges are avoided.

Condition	Output pin voltage swing	VCC pin voltage swing
No protection on the output pin and 330 pF decoupling capacitor on the VCC pin	-415 V to 185 V	-45 V to 28 V
Diode on the output pin and 10 nF decoupling capacitor on the VCC pin	-15 V to 12 V	-7 V to 5 V

Table 12.2: Voltages on the TX pin with and without protection during direct discharge to the antenna

Indirect discharge:

In this modeling case the ESD generator is discharged to a large ground plane while placing the remote key PCB 1.5 cm away from the tip of the ESD generator. The field coupled to the antenna gives rise to a voltage swing on both output and VCC pins of the TX IC relative to the ground of the PCB. As in the direct discharge case, simulations have been performed under two conditions and the results are shown in the Table 12.3. The resulting values are still large enough to upset the IC, while damages are less likely.

Condition	Output pin voltage swing	VCC pin voltage swing
No protection on the output pin and 330 pF decoupling capacitor on the VCC pin	-25 V to 40 V	-6 to 6
Diode on the output pin and 10 nF decoupling capacitor on the VCC pin	- 2 V to 5 V	-7 V to 1 V

Table 12.3: Voltages on the TX pin with and without protection due to field coupling

Another ESD failure scenario is the direct field coupling to the IC. An ESD of 10kV, 0.85ns rise time in contact mode results in a peak current of 35A leading to 370 A/m at 1.5 cm distance. Based on the IC ESD sensitivity database [94], this field strength would give rise to a 70% IC upset probability. Here it should be reminded that the database is based on physically larger ICs which allow stronger coupling. Still, the possibility of direct field coupling to the ICs inside the fob should be considered as possible ESD entry path leading to changes in the memory content or latch up.

This investigation has quantified the impact of different ESD events on the remote key fob PCB and has shown a need for IC soft error characterization to accurately predict the type of failure and the IC failure levels.

12.2 Investigations on ESD Coupling

Possible IC destructions and disturbances due to indirect ESD on PCB and in cables were investigated.

A model based ESD failure analysis method was developed in section 7.6. IC failure mechanism was investigated that is supposed to be energy based. Failure modeling was done in thermal domain. Electrical characteristics and failure behavior of common automotive ICs was analyzed and verified in two different setups by means of TLP and IEC ESD generators. Generated IC models were used to analyze possible permanent failures due to indirect ESD.

Soft failures can be triggered already by a low energy portion of the ESD pulse. Section 7.7 gives an overview on typical soft failure categories. A general modeling approach is difficult, as they fall into many different classes. Failure behavior differs with different IC-pins and transfer of results from one to another device is only in some cases possible.

In case of a direct discharge of a charged part into a car body or trailer body critical voltages can couple into wires close to the discharge current path. In section 7.5 a new method to model such a configuration was presented. In section 8.2 the method was applied to model a configuration where an IEC generator discharges into coupling plane close to a transmission line with 1 m length. The setup is shown again in Figure 12.1.

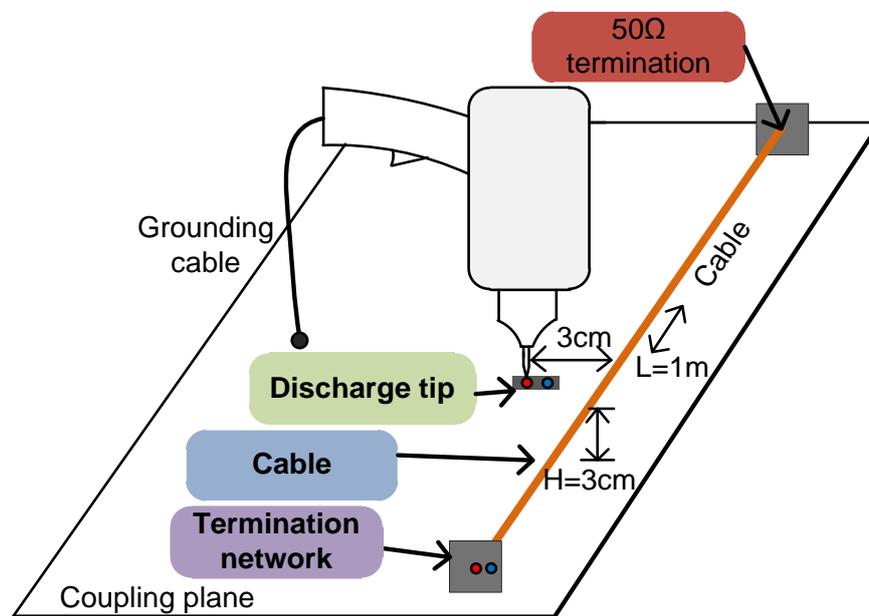


Figure 12.1: ESD generator-cable configuration for ESD coupling simulation

In simulation, signals on different loads of the transmission line were analyzed. No energy based failures on ICs can be expected. Possible failures were analyzed considering coupled voltage amplitudes. Figure 12.2 and Figure 12.3 compare

simulated voltage and current on the input capacitor for different termination networks for 1 kV and 4 kV IEC discharge.

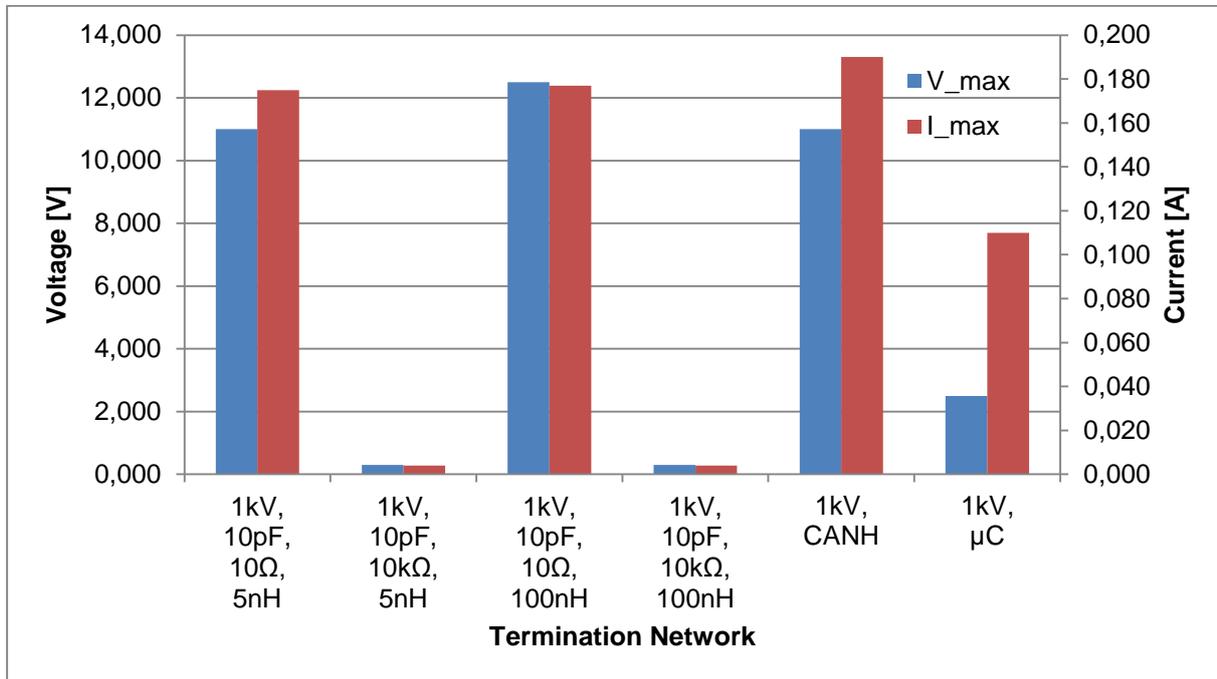


Figure 12.2: Simulated amplitudes on the input capacitor of the termination network for field coupling of 1 kV IEC discharge

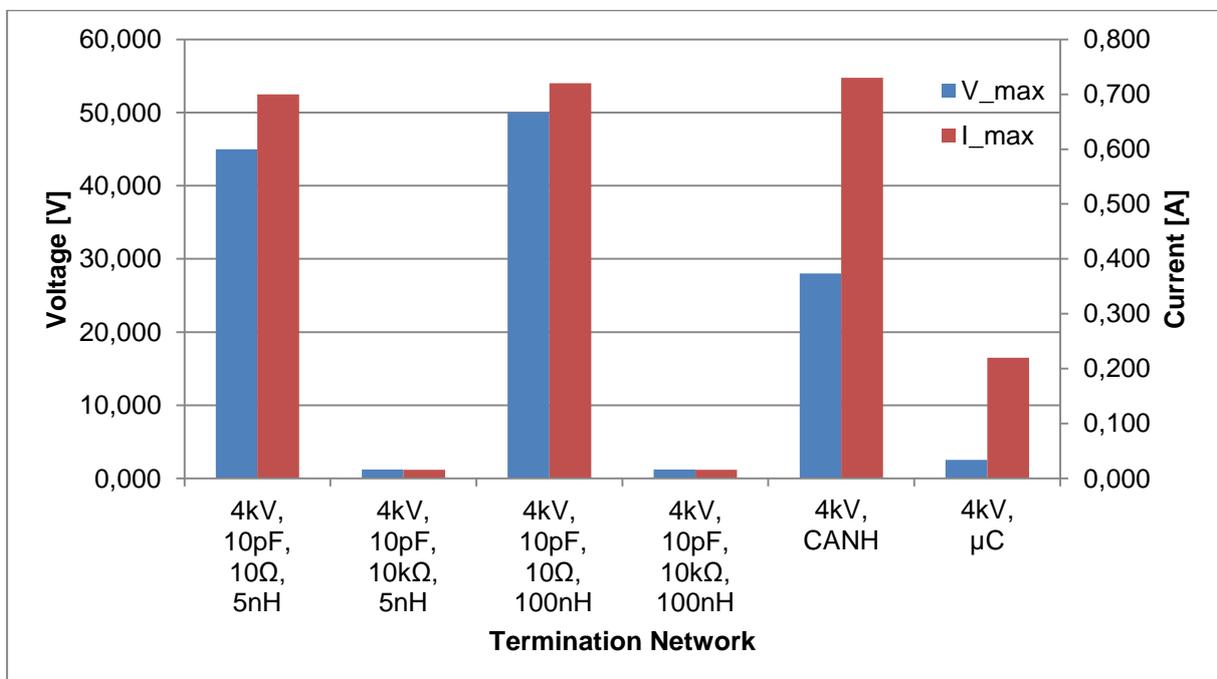


Figure 12.3: Simulated amplitudes on the input capacitor of the termination network for field coupling of 4 kV IEC discharge

A voltage level of 10 V on CANH pin can be reached for charge voltage of 3 kV. More general statements can be made by modeling an IC input with a serial circuit of a 10 pF capacitor, a 5 nH inductor, and a variable resistor. Signals current and voltage waveforms at the 10 pF capacitor were analyzed. Coupled voltages and currents increase with smaller input resistance. Amplitudes increase linear with charging voltage level of the ESD generator. A level of 10 V is exceeded for an input resistance of 1 k Ω and 5 kV charging voltage. In a second step different values for serial inductance were simulated. An effect of the inductance could be only observed for small input resistances. Inductors can be useful as ESD protection only in case of low input resistance.

In case of a direct discharge into a connector pin connected by a PCB trace to a well protected IC pin, the ESD pulse can couple to other parallel PCB traces terminated by IC pins or other loads that are weakly protected. Coupling can be modeled by a multi conductor transmission line model presented in section 7.4. The model is parametrised for typical PCB geometries in automotive ECUs. In section 8.3.4 system verification is done on the demonstrator PCB with resistive loads and a parallel protection element on one end of the victim line. Good matching between simulated and measured curves could be reached. A common case in automotive ECU where two ICs build up a communication channel with a line was studied in 8.3.3 by simulation only. Figure 12.4 demonstrates the setup.

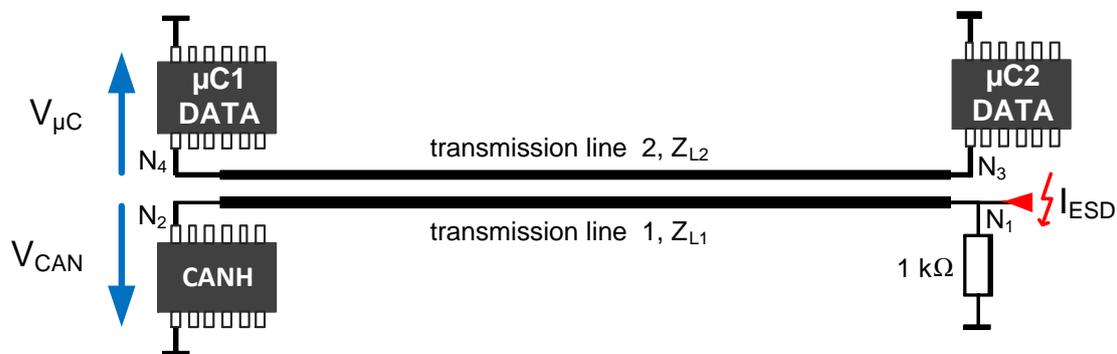


Figure 12.4: Simulation setup with microcontrollers as loads on the victim transmission line

For a victim line terminated by μ C data pins and an 8 kV IEC discharge at node 1 no thermal failure could be simulated. The scaled model of μ C data pin to 1 kV HBM robustness has a failure energy of 350 nJ. Even this worst case failure level has not been reached for an 8 kV IEC discharge. Nevertheless oscillating voltage and currents with notable amplitudes could be simulated. Even when coupled energy is low, it can not be excluded that the high voltage and current amplitudes can cause permanent failures on some ICs.

Simulated amplitudes on the source and victim lines are compared in Figure 12.5 and Figure 12.6.

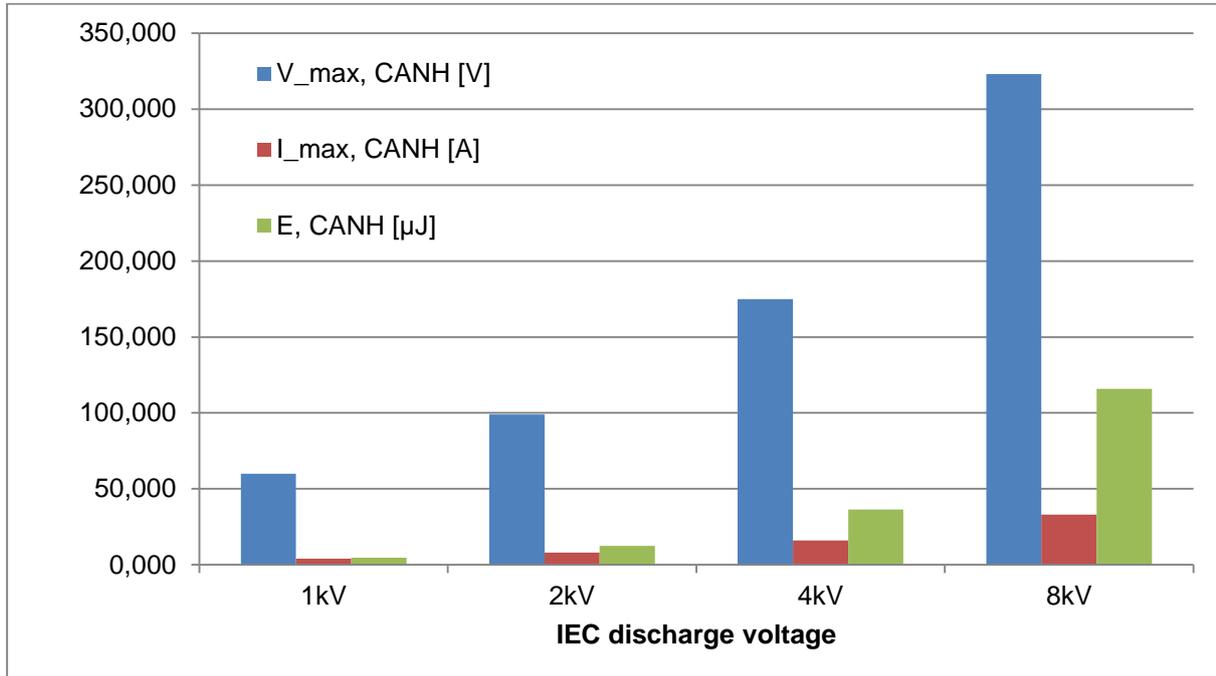


Figure 12.5: Simulated measures on CANH pin depending on IEC discharge voltage. Note that the energy scale is in μJ .

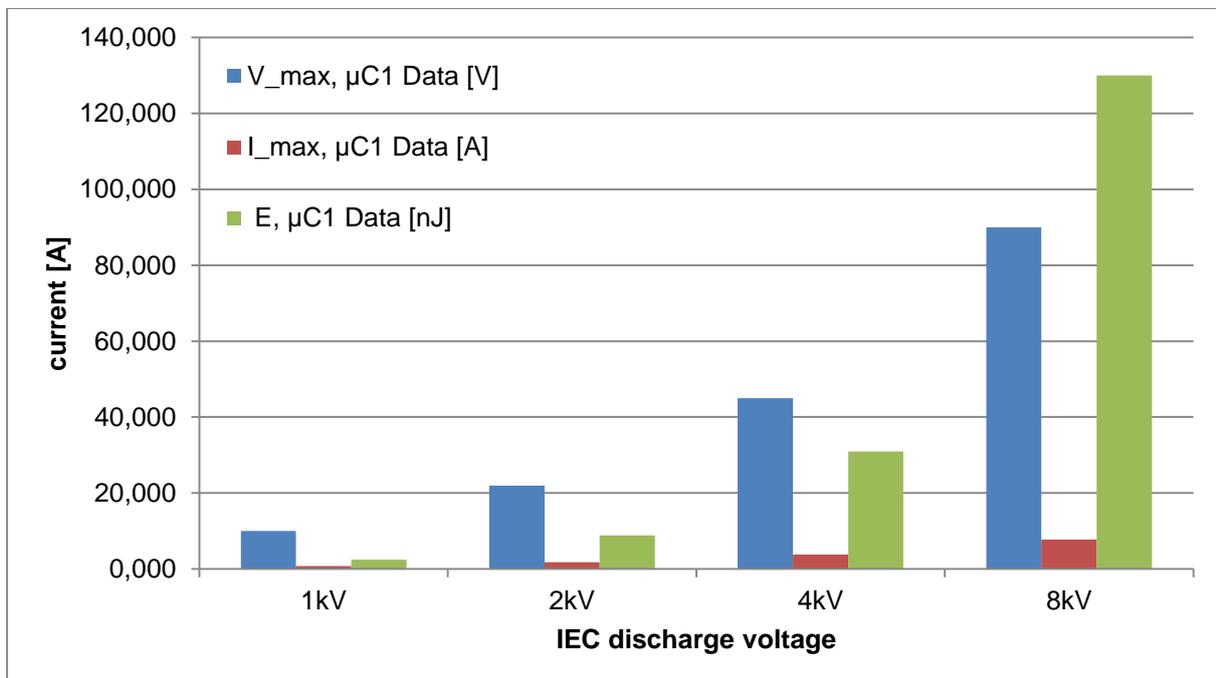


Figure 12.6: Simulated measures on $\mu\text{C1 Data}$ pin depending on IEC discharge voltage. Note that the energy scale is in nJ .

All results are very sensitive to variations of the topology and termination parameters. In order to verify ESD robustness of a design with high confidence, individual simulations of a PCB configuration are necessary.

13 Acknowledgement

This project was supported by AK23 in der FAT - Elektromagnetische Verträglichkeit. Some fundamental modeling approaches and phenomenon knowledge necessary for this project are based on former projects supported by national and international founding and ESD Forum Germany.

14 References

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Annex A: Lists of Characterized Protection Elements

Manufacturer	Type	V_{BD} [V]	V_{Clamp} [V]	C_{par} [pF]	L_{ser} [nH]	Model accuracy
Protek	GBLCSC05	8,02	9,86	7,64	3,93	good
Protek	GBLCSC05C	7,62	10,17	1,51	5,36	good
Protek	GBLC12	16,03	16,77	12,56	4,17	good
EPCOS	CDS3C09GTA	11,92	22,41	224,2	3,58	satisfying
EPCOS	CDS3C20GTA	28,45	49,82	69,62	6,37	satisfying
NEC	NNCD6.8D-A	6,91	7,25	95,58	2,82	very good
NEC	NNCD12D-A	12,07	12,4	66,29	2,59	very good
Bourns	CD0603-T05C	7,48	8,51	12,22	3,4	satisfying
Bourns	CD0603-T12C	18,43	22,3	8	3,37	good
Bourns	CD0603-T24C	30,99	35,1	4,84	2,3	good
Taiwan Semiconductor	TSZU52C9V1	9,012	9,73	88,87	2,28	very good
Taiwan Semiconductor	TSZU52C12	11,73	11,99	83,71	2,42	very good
Taiwan Semiconductor	TSZU52C18	18	18,6	52,4	2,28	very good

Table 14.1: TVS diodes characteristics: breakdown voltage V_{BD} measured at 1 mA in TLP-IV-curve, clamping voltage V_{Clamp} measured at 1 A in TLP-IV-curve, parallel capacity C_{par} and serial L_{ser} inductivity measured with VNA, and model accuracy

Manufacturer	Type	V_{BD} [V]	V_{Clamp} [V]	C_{par} [pF]	L_{ser} [nH]	Model accuracy
EPCOS	CA05M2S14ACC1G	50,79	87,67	59,8	15,2	satisfying
EPCOS	CT0603K14G	20,34	39,23	130,3	7,53	satisfying
EPCOS	CT0603L25HSG	64,61	117,13	9,66	15,47	satisfying
EPCOS	CT0603S5ARFG	/	530	1,15	3	sufficient
EPCOS	CT0603S14AHSG	27,49	51,97	16,13	6,73	satisfying
Vishay	MLV0603E30403T	8,125	17,77	1190	3,2	good
Vishay	MLV0603E31103T	17,6	31,8	597,3	2,2	satisfying
TDK	AVR-M1608C080M	8,517	14,33	603,8	2,7	very good
TDK	AVR-M1608C180M	17,94	27,16	559,7	2,72	very good
TDK	AVR-M1608C390K	38,02	53,77	259,15	2	very good
AVX	VC060309A200	13,13	25,62	432,5	4,18	sufficient
AVX	VC060314A300	19,28	34,93	277,3	5,68	sufficient
AVX	VC060318A400	26,44	46,1	141,1	8,12	sufficient
AVX	VC060326A580	33,72	68,69	114,6	12,66	sufficient
AVX	VC060330A650	41,65	63,14	101,2	10,14	sufficient
AVX	VC080514A300	17,93	31,25	310,8	4,9	sufficient
AVX	VC080514C300	18,86	31,62	583,7	2,6	satisfying
AVX	VC080526A580	34,57	53	112,7	9,7	sufficient
AVX	VC080526C580	34,51	53,79	305	3	sufficient

Table 14.2: Varistor characteristics: breakdown voltage V_{BD} measured at 1 mA in TLP-IV-curve, clamping voltage V_{Clamp} measured at 1 A in TLP-IV-curve, parallel capacity C_{par} and serial L_{ser} inductivity measured with VNA, and model accuracy

Manufacturer	Type	V_F [V]	V_B [V]	C_{par} [pF]	L_{par} [nH]	Model accuracy
Bourns	CG0603MLC-05E	706	24	<1	5	good
Cooper	0603ESDA-MLP7	485	76	<1	5	good
Littlefuse	PGB1040805MR	330	139	<1	5	sufficient

Table 14.3: Voltage variable polymer characteristics: firing voltage V_F , burn voltage V_B , parallel capacity C_{par} and serial L_{ser} inductivity measured with VNA, and model accuracy

Manufacturer	Type	V_F [V]	V_B [V]	C_{par} [pF]	L_{par} [nH]	Model accuracy
Mitsubishi	CSA20-141N	344	50	<1	5	good
Mitsubishi	CSZ30-201N	842	160	<1	5	good

Table 14.4: Spark gap characteristics: firing voltage V_F , burn voltage V_B , parallel capacity C_{par} and serial L_{ser} inductivity measured with VNA, and model accuracy

Annex B: Merit of published ESD guidelines and application of guidelines to the reported failure cases

Analysis of published ESD guidelines with respect to failure cases analyzed in this report

Objective of this section is to analyze published ESD guidelines with respect to their foundation and results reported in this report.

Many rules for system level ESD can be found in literature. A set of guidelines has been selected based on their relevance to the automotive industry. The complete list of references used for creating these guidelines can be found in the references section.

Firstly, the general design guidelines have been categorized into different aspects of product design such as “PCB design”, “Enclosure design” etc., secondly, remarks with respect to their foundation and to research reported in the report have been added. The guidelines are presented in a tabular format and the references are shown alongside.

Guidelines			
#	PCB Design	Remarks	Reference
1	<p>Use ICs with appropriate robustness against ESD.</p> <p><i>Some of the following parameters will help in determining the robustness:</i></p> <ul style="list-style-type: none"> - Are just fast and sensitive enough to do the job. - Have enough noise margin that small series resistors on their inputs and outputs will not affect them. - Have high noise/noise-energy immunity. - Have good ESD damage threshold voltage values - Have differential inputs and outputs. - Can read back all internal registers. - Are immune to latch-up.[98] 	<p>ESD robustness has multiple aspects:</p> <p>One needs to distinguish damage (hard error) and upset failure. A third class of errors is fast transient latch up, which may or may not be destructive.</p> <p>Damage robustness for non-powered conditions which his expressed in HBM, CDM and possibly in MM model robustness. This gives a first orientation towards the expected hard error robustness, however, these tests are performed in none powered conditions. Due to changes inside the circuit (for example, the turn off of power clamps in powered up condition), and the low impedance path provided by a PCB from VDD to VSS one cannot directly expect that the system level robustness is the same as the IC level robustness even if the same tests waveforms are applied.</p> <p>The IC level test methods differ from the system level test methods, for example the IC level HBM test is</p>	<p>Section 10.4.2 PCB Design Rules</p>

		<p>modeled after the discharge of a human from the skin, while the system level ESD discharge, now often called HMM (Human Metal Model) is modeled after the discharge from a small hand held piece of metal. The difference is a much lower source impedance (about 300 Ohm vs. 1500 Ohm), and a faster rise time about 1ns to 5 ns.</p> <p>IC level testing only looks at damage, not at soft errors. But system's need to be robust against both types of ESD related problems.</p> <p>ICs should only be as fast as needed for the purpose, an input should not be faster than needed for the application, as ESD coupled noise often are pulses having only < 2ns width that might be ringing at a frequency determined by the coupling path. If the IC is sufficiently slow such that it can "overlook" such type of noise at an input it improve the system level robustness if this input receives noise. In other cases low pass filtering at the input is advisable.</p> <p>The soft error robustness of ICs can be determined using scanning and direct injection methods {Section 3.2}</p> <p>VI curve characterization and testing against fast transient latch up characterizes the IC for possible damage {Section 3.1.2}</p>	
2	<p>If sparks can reach the PCB it needs to be checked which electrical net the spark can hit and how the current flow path from this net to ground is. [98]</p>	<p>The rule is useful. Objective is to identify if the ESD current can hit any net other then ground, if yes, this net needs sufficient protection, and if it the spark hits ground, the ESD current and the associated fields need to be guided to avoid large upset causing voltage drops or strong induced voltages.</p>	<p>Section 10.4.2 PCB Design Rules</p>
3	<p>If capacitors are used as ESD protection the consequence of non-linearity needs to be considered. This is mainly important for X7R and Y5V type ceramics and capacitor values < 100nF. Those capacitors will charge up to a voltage much greater than their nominal voltage if they receive for example, a 10 kV ESD discharge. This will reduce their capacitance momentarily such that their ESD protection effect is limited. X7R will lose 80 % of its capacitance if the voltage reaches twice the nominal voltage,</p>	<p>The rule is useful. Capacitors are often used as ESD shunt devices. The voltage can surpass the rated voltage of the capacitors without causing damage. The loss of capacitance at higher voltages will diminish the ability of the capacitor to protect against ESD.</p>	

	Y5V will lose 80 % of its capacitance even at its rated voltage.[98]		
4	Non-insulated chassis ground on the PCB must be separated from other traces by at least 2 mm. This applies to anything connected to chassis ground, as well as traces. [98]	This rule is questionable. It tries to set a distance between a conducting enclosure and a PCB, such that no sparking can occur. At the suggested distance of 2 mm even an ESD of 5kV can cause a breakdown if the edges of the spark gap forming structure are sharp. If a discharge to the enclosure, or to a cable (which is often referenced to the PCB) will lead to a spark depends on the connection resistance and inductance between the enclosure and the PCB and the distances. If the enclosure has to be kept isolated from the PCB, and if the discharge scenario allow to the buildup of a voltage of many kV between the enclosure and the PCB then much greater distances are suggested. The report suggests 1kV/mm up to 10kV as secure isolation distance.	Section 10.4.2 PCB Design Rules
5	Chassis ground traces should have a length-to-width ratio of no more than 5:1. [98]	This suggestion is questionable. The underlying idea is to reduce the "inductance", such that the inductive voltage drop is reduced. However, the inductance is not defined for a trace itself, inductance is only defined in a loop. If inductances should be reduced then the total loop inductance should be reduced. This is not just achieved by a 5:1 ratio.	
6	Non-insulated electronics should kept at least 2 cm away from PCB areas that an operator can touch, or non-chassis grounded metallic objects that the operator can touch. [98]	This again relates to sparking distances. It has been shown that 1kV/mm up to 10kV and 1.3kV/mm above 10kV provide a secure barrier against sparking. The 2cm will be a secure barrier against about 15kV, even under very unfavorable conditions.	
7	Power and ground traces should be kept one over the other on opposite PCB layers. [98]	This rules aim is to create small loop areas between power and ground traces, it only applies to 2 layer boards which are rarely used anymore. Smaller loop areas allows less coupling to the trace in case an ESD	

		causes strong transient fields, but if a decoupling capacitor is placed very close to the IC, even on a 2 layer board, this capacitor will reduce pulses between Vdd and Vss.	
8	Ground plane and ground traces must be connected to form a grid. There must be vertical ground lines connected to horizontal ground lines at least every 3 cm in either direction. Typically, on a double sided PCB, this means layer two may have vertical ground lines, layer one may have horizontal ground lines, and there must be a feedthrough at least every 3 cm to connect the two. Of course, connections at intervals of less than 3 cm are even better, and ground planes are better than ground grids. [98]	Again, this is a rule for 2 layer boards. There is no justification for the numbers such as “3cm”. The general idea is to create the least broken ground net in the given number of layers and space. This will confine fields of signals better, and vice versa reduce the coupling to nets if ESD currents flow on or nearby the PCB.	
9	All signal lines must be within 10 mm of a ground plane or line. The ground can either be on the same layer or the next layer above or below the signal line. If the signal line is 30 cm long or more, it must be directly beside a ground trace, or over a ground trace or plane on another PCB layer. [98]	This again is a rule for single or dual layer boards. The objective is again to confine the signal fields such that they couple less with currents and associated fields of an ESD at the PCB or nearby. The number “10 mm” has no justification.	
10	Bypass capacitors between power and ground must be no more than 4 cm apart. [98]	This again is a 2 layer rule aiming at reducing unbroken loop areas. The number “4 cm” is not justified.	
11	Components with the most interconnects between them must be side- by-side, or end-to-end. [98]	This rule seems to be motivated not by ESD or EMI, but more by optimal routing space usage. Of course, if trace lengths are minimized and fields are well confined coupling is reduced.	
12	All components must be as close as possible to the I/O connector. [98]	We disagree with this rule. In the region of I/O connectors there is often a large current density if ESD hits the connector shell, or if ESD hits the pins and the overvoltage protection devices are placed close to the connector (which should be done), then there will be large current densities. If other components, for example sensitive ICs are placed in this region coupling to the devices will be increased. The opposite rule is more reasonable: Do not place components that have known or suspected ESD soft error sensitivity close to the I/O if possible. Further, the SEED analysis has shown that having a long trace, or inductance between an external and an IC internal protection device will improve the protection, as the TVS has a low dynamic resistance if it is forward biased, the same is true	Section 10.4.2 PCB Design Rules

		for the IC input, it has a low dynamic resistance. Thus, the connecting trace acts as an inductor which reduces the threat caused by the initial impulse of the HMM waveform.	
13	Fill all unused portions of the PCB with ground plane. [98]	The rule needs to be qualified by the number of layers in the board. For a dual layer board this is most likely true, as the fills, providing they are sufficiently interconnected, will create a "ground plane". For a 4 layer board often having a stackup such as S-GNG-PWR-S it is useful to add ground to the signal side close to the power, this provides shields and increases the capacitance between power and ground. Adding ground over a ground plane serves no purpose from an electromagnetic point of view. In general, it is good to have only one ground plane with no gaps.	
14	If possible, feed power or signals from the center of the PCB edge, not from the corner. [98]	The rationale of this rule is not known to the author of these comments.	
15	Long sections (30 cm or more) of especially sensitive signal lines should be transposed with their ground line. [98]	The rule aims at improving the field confinement of the signal, such that ESD transient field coupling can be reduced. For a 4 layer or more layer board the sensitive lines should be routed next to a ground plane, at best in inner layers. This rule does not apply for 4 and higher layer count PCBs. A filtering RC combination can suppress coupled noise very well if it is placed directly at the receiving end of the trace.	
16	Put the protection circuit at the connector (preferred), or $\leq 25\text{mm}$ (1") from the receiver/driver. [100]	This rule has its merits, see rule 12.	Section 10.4.2 PCB Design Rules
17	Put a circuit-common guard ring around the rest of the PCB: - $\geq 2.5\text{mm}$ (0.1") wide in every layer you can, stitched together by vias about every 13mm (0.5"). - Keep signal traces $\geq 0.5\text{mm}$ (0.020") inside this guard ring. [100]	The idea behind this rule is to capture direct ESD hits to the edge of the PCB and then to guide the current to a better return location. If, for example a two-shell plastic enclosure is used to house a PCB then there is a risk of ESD discharges through gaps between the connector shells. These ESDs would cause a large, widely spreading current density on the ground plane if they hit the ground plane, or worse, if they hit a net, they would inject large currents into this net. Both cases, especially the second one are unwanted and may cause damage (hit to a net), or soft errors (hit to a ground	

		<p>plane). The guard ring is intended to prevent these current injections. The details of the dimensions are rather uncritical. The distance of 2.5 mm to the PCB's other structure is motivated by avoiding sparking between the guard ring and the inner PCB structure. 2.5 mm will provide short term about 5 kV. Only if the guard ring is inductively or resistively connected high voltages will occur between the guard ring and the inner PCB structure in case of an ESD hit that might surpass this value. The value will also depend on the size of the PCB. The voltage induced between the inner structure of the PCB and the guard ring can be simulated by combining a simplified PCB structure with an ESD generator model in a full wave simulation. There is no rationale for the "13 mm" number.</p>	
18	<p>Put a ferrite bead in each power line where it enters a PCB. [100]</p>	<p>This rule is mainly motivated by EMI. A ferrite bead will also provide a high impedance against ESD, however, small ferrite beads saturate very easily, such that the effective inductance is very low for ESD. The SEED simulations have provided examples of ferrite bead saturation.</p>	
19	<p>Make provisions for changing the grounding scheme, especially circuit common to chassis ground connections:</p> <ul style="list-style-type: none"> - Run chassis ground along PCB edges that have connectors to the outside world; use wide traces in all layers, tied together by vias about every 13mm (0.5"). - Connect chassis ground to the connector housings and to any mounting holes on these edges. Use topside and bottomside pads without soldermask, put vias around the mounting holes, and don't get solder on these pads during assembly. Screws with built-in Belleville washers connect the pads to tabs/metal standoffs on the chassis/shield. - Make provisions for isolating/connecting other mounting holes to chassis ground-isolated pads with 0-ohm resistors to circuit common, choice of plastic or metal standoffs, etc. - Separate circuit common/power from chassis ground by an identical 0.64mm 	<p>This rules have many motivations, some of them are questionable.</p> <p>In general we warn against having different grounds, such as chassis ground and PCB ground. There are situations in which one has to have different grounds, however, this should only be done if the reason is well understood.</p> <p>One needs to be aware of: If there are two grounds it is only been done to have a voltage between them!</p> <p>What causes the voltage? Why do we want to have a voltage between grounds?</p> <p>What happens to traces that cross the gap, the voltage will drive a current on these traces. Is that the goal?</p> <p>If no traces cross the gap in the ground, or if the signals that cross are coupled by transformers or optically, then there is no problem in having</p>	<p>Section 10.4.2 PCB Design Rules</p>

	<p>(0.025") wide moat in all layers.</p> <p>- Connect circuit common to chassis ground by ground ties (1.27mm (0.050") wide traces on the top and bottom layers) paralleled by pads for ferrite beads/capacitors at mounting holes and every 100mm (4") along the moat. [100]</p>	<p>different grounds. However, if traces cross the gaps it has to be understood very well what will happen to the signals on these traces, and, will these signals induce a large voltage in the gap between the grounds. From an ESD point of view it is clear that traces that cross across a gap between grounds will be subject to very strong coupling as the ESD may cause a very large voltage between the grounds.</p> <p>The underlying idea of having a chassis ground and a PCB ground for ESD is to "keep the ESD currents away from the circuit". This is acceptable and can be successful, but the price paid is in form of having very strong noise signals on the traces that cross the gap.</p>	
#	Filters and transient suppressors	Remarks	Reference
1	<p>Every signal at connectors that may receive ESD hits including signals that go through opto-isolators needs to have a filtering (for example a capacitor to ground) that is appropriate to absorb or reflect the ESD energy, but maintains signal integrity for the wanted signal. [100]</p>	<p>The idea of filtering signals such that differences in spectral components of ESD to the wanted signals are used to shunt ESD current without negatively affecting the signal integrity is good. However, the statement that "every signal" needs to be treated as such is too far reaching. Knowing the signal integrity requirements and the ESD threat is a must for simulating the optimal capacitor value. Only in cases in which the spectral difference is obvious and large one can pick a capacitor value by intuition. Many sensor signals and most audio lines fall into this class.</p>	
2	<p>Signal filters need to be placed as close as possible to the connector having ground connections as close as possible to the filter location. [100]</p>	<p>This is true. The filters, such as TVS or capacitors divert ESD current. The ESD current should be allowed to return to the chassis at the connector or as close as possible to it. The simulation in the report on the USB connector clearly show the importance of having close by ground connections.</p>	

3	<p>Use series resistors to attenuate indirect or secondary ESD stress in the system. Series resistors have proven to be very effective for system-level ESD protection and they can be used with voltage clamps and decoupling capacitors. [101]</p>	<p>The usage of series resistors is a good idea if their laminations are taken into account. If a pin is hit by an ESD (direct ESD) a physically small resistor most likely will spark over and/or be damaged by the ESD. However, if the resistor does not spark over it provides a good mean to reduce the currents if the resistor value is large enough. In most cases these resistors are used either for filtering the indirect effects of an ESD hit (the rule probably means “indirect ESD effects, so the line is hot hit, but some other part near by” and does not mean secondary ESD in which a primary ESD charges a metallic part, causing a secondary sparking inside a product (see rear light example). IN most cases the resistors are used to “decouple” primary protection devices (TVS) from the internal IC protection. Even a small resistor such as 10 Ohm can provide a lot of isolation, at 2 A current flowing into the IC 20V will drop at the resistor allowing the TVS to have a “softer” VI curve and still protect the IC. The SEED simulation shows such cases using SPICE.</p>	
4	<p>Follow power-line filters with high frequency ESD filters. [100]</p>	<p>We do not see any rational for this rule.</p>	
5	<p>Connect blocking devices to ESD sources and low-impedance drivers/receivers:</p> <ul style="list-style-type: none"> - <=100k resistors for CMOS inputs. - <=50-ohm resistors for bipolar inputs. - Ferrite beads if low resistance is important. They provide 50-500 ohms impedance from 10- 1000MHz. [100] 	<p>This rule wants to use series devices as protection against ESD. For the resistors the limit is sparking if there is no primary protection (even a spark gap might function as a primary protection). The ferrite bead has the problem of saturation. The rule was probably written quite some time ago, ferrite beads did not exist in sizes 0402 and smaller. These small beads cannot handle large currents and will saturate.</p>	
6	<p>Connect shunt devices to high impedance drivers/receivers:</p> <ul style="list-style-type: none"> - 100-1000pF capacitors to chassis ground. - 10-100pF capacitors to circuit common. - Clamps to chassis ground/circuit common. - Crowbars to chassis ground/circuit common. - Keep leads very short- 1nH/mm lead inductance slows down turn on. - Connectors are available with built-in capacitor arrays, ferrite sleeves, and MOV arrays. [100] 	<p>The rules are in general justified in general, they are a simplification of what can be achieved using a good simulation technique as outlined in the SEED process. A 100-1000pF capacitor is a useful EMI reduction tool, however it does not help a lot against direct ESD hits, as the capacitance value is too small. It reduces the noise from indirect coupled ESD (typically a few nanosecond wide pulses that might be ringing). Further, if an direct ESD hit</p>	

		<p>injects current into a small value capacitor, such as 1000pF and no other component limits the current the voltage across the capacitor will become very large. Keeping lead lengths short on capacitors is important to reduce the apparent inductance of the capacitor and connection geometry.</p> <p>In designing systems for high protection volume it is economical to simulate the protection to find the most economical, but still sufficient protection. General rules as the one to the left are only starting points in this engineering trade-off.</p>	
7	<p>Choose components to withstand ESD voltages and currents:</p> <ul style="list-style-type: none"> - Thick-film and carbon composition resistors. - Shunt capacitors that may take direct ESD hits should be rated $\geq 1\text{kV}$, or be large enough to absorb $2.3\mu\text{C}$ without exceeding their voltage rating if they aren't protected by transient suppressors. [100] 	<p>Avoiding component damage motivates this rule. However, it is often possible to use components during an ESD event outside the nominal specifications. For example it is common practice to use 25V or 50V capacitors as ESD suppressors although they may momentarily see more than 100V across the terminals. It has been shown that this does not lead to damage in most cases For resistors there is a risk of damage by ESD. The resistors listed to the left, carbon composition, thick film or equally good metal film and ceramic composition are relatively expensive.</p>	
#	Cable Design Rules	Remarks	Reference
1	Electric connections must use materials no more than 0.75 V apart from each other in electrochemical series. [98]	This rule is not directly motivated by ESD but to avoid corrosion of contacts.	Section 10.4.3
2	The anodic (more positive) material must have a larger uncoated surface area than the uncoated surface of the cathodic material. [98]	This rule is not directly motivated by ESD but to avoid corrosion of contacts.	Cable Design Rules
3	The shield material must be at least 0.025 mm thick. (100 percent coverage is preferred.) [98]	The underlying idea is skin effect. The transfer impedance needs to be kept low to avoid that currents which flow on the outside of the shield do not induced relevant voltages on the inside. The skin depth of copper is about 0.025 mm at 10 MHz. A good shielding is achieved if the metal is about 5 skin depths thick. This will be reached at about 50 MHz. If the cable shield is indented to separate ESD currents on the outside of a cable from the inner structure by skin effect	

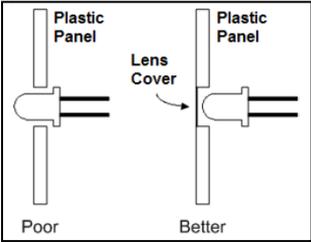
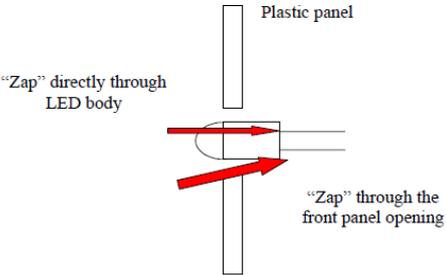
		separation of both systems the rule will be useful. However, most cables will have much better shields, a combination of a braid with a foil is a often met method of creating shielded cables.	
4	Use shielded cables and connect the shield only to chassis ground. The arc path from chassis to other pins must be at least 2 mm. [98]	This rule again assumes that a large voltage can occur between the inner system of the cable and its shield. In general we do not think such a design is good. The ESD currents should be guided such that the voltages between the inner parts of the cable and its shields are kept small by keeping the ESD current on the outside of the shield. If a system requires to have a "floating" inner system which may see a large voltage to the shield then the ESD situation should certainly be evaluated by experiment and simulation. No general rule applies then.	
5	Connect the cable shield to chassis at both ends of the cable. A metallic connection is preferred, but a high frequency (capacitive) connection can be used if required to prevent a significant ground loop problem. [98]	The rule is justified. It is important to keep shield connection inductances very low. Even 1nH inductance at a current rise of 20A/ns will cause 20V voltage drop across the shield connection. This 20V will be visible to the inner system of wires in the cable and drive current possibly causing soft errors or even damage.	
6	The cable shield must connect to the chassis within 2 cm of the cable entry/exit point, and the unshielded portion of the cable must be less than 2cm. [98]	The rule is wrong. The cable shield needs to connect at best in 360 deg directly at the entry point. If 2cm is allowed, and we assume 5nH/cm we would have 10nH. At 20A/ns ESD hit 200V would be induced having a high likelihood of damage and nearly with certainty causing soft errors in most systems.	
7	Extra wires in the cable must be trimmed so they don't extend beyond the shield, or must be connected in parallel with the other lines. [98]	Not motivated by ESD	
8	A shield which is also a chassis ground path shouldn't normally go through a ferrite bead, and certainly not ferrite beads in common with other lines. [98]	The rule seems to have two contradicting messages. It is good to place ferrites around cables to reduce the common mode current. However, if the ferrite is only around the shield connection (think about a pig-tail connection having a ferrite around the pig tail), then the ferrite will even increase the already high shield-chassis inductance, causing even larger voltages to be visible by the	

		inner wires if an ESD current is flowing from the cable shield to the chassis.	
9	If ferrite beads are used, they should be at the receiver end of the cable. [98]	The motivation is to filter the common mode current on a cable close before it enters the system, for having a ferrite enclose both signal and return (or signal, return and shield), or, if the ferrite is placed just into a signal line, then the ferrite can perform spectral filtering. This will reduce the ESD noise coupling somewhat, for example, if the shield of the cable is only badly connected to the enclosure. In general one will place filters at the receiver side to avoid noise disturbances by ESD, while filters are placed at the transmitter side to reduce EMI. In both cases the spectral difference between the signal and the unwanted EMI or ESD frequency range is used by the filter. If the frequency ranges are overlapping, then there will be no filter that allows ESD protection without negatively influencing SI. The situation is different in differential signals, as one is not relying only on spectral differences, but also modal differences can be used. The ESD will be in most cases in common mode, while the signal is in differential mode.	
10	If the shield can't be connected to chassis at one end of the cable, connect it to ground via a 4 nF, 1 kV ceramic capacitor. The provision for this capacitor should allow it to be an option. [98]	The motivation of this rule is to connect the shield for RF to the chassis. Now if the rule asked for a 1kV capacitor, then one needs to assume that the a voltage of up to 1000V might be expected between the chassis and the cable shield. If this would be caused by ESD it would certainly drive large currents on the inner wiring system of the cable. Of course, there are situations at which AC or DC isolation requirements prevent a direct shield connections. Those are beyond the analysis of this report.	
11	Shield connector cables to reduce coupling (use foil or foil and braid shields). [101]	Accepted. One has to understand the requirements for transfer impedance at the connectors and the shield. A typical ESD current at 5kV may have 20A/ns current derivative. If the shield-connector connection has 1nH transfer inductance then 20V will be visible by the inner system for about 1ns. This is certainly enough to disturb many systems. The same is true for the	Section 10.4.3 Cable Design Rules

		shield transfer impedance. A good double shielded cable such as RG-214 will have less than 10mOhm per meter transfer impedance at 100MHz. At 20A this will still mean 2V induced on the inside. Now the spectral current at 100 MHz will only be a fraction of the peak current of the ESD, such that a cable as RG-214 would provide a good shielding. If we look in contrast at a cables such as RG-58, having a single braid with about 90% coverage area the transfer impedance can be about 1 Ohm/m at 100Mhz. The induced noise would be 200 times larger.	
12	Keep cables as short as practicable. [101]	OK	
13	Properly ground cables entering the enclosure.	Properly means very low transfer inductance, usually 360 deg shield-enclosure connection.	
14	Use transient suppressors and filters at cable entry points.	It is good to divert the current from the net to a chassis connection to avoid large current densities in the board and large currents on the traces which can couple to other traces.	
15	Terminate cable shields to the outside of the metal enclosure/shield, preferably with 360-degree bonds- short and wide connections (see Rule 35) may suffice, but keep unshielded sections of the cable <= 40mm (1.6") long. [100]	The transfer impedance needs to be as low as possible, even 2nH inductance between the cable shield and the enclosure will allow many tens of voltages being induced by the current along this inductive connection if ESD hits the cable or the enclosure close to the cable entry point.	
#	Enclosure Design Rules	Remarks	Referen ce
1	The enclosure design must ensure that uninsulated electronic components and conductors have at least a 2 cm arcing distance from ungrounded metal objects that may be touched by the operator. [98]	The rule tries to prevent sparking. Even under the most pessimistic circumstances one would expect 15kV breakdown voltage for 2cm gap.	Section 10.4.4
2	The enclosure design must ensure that uninsulated electronic components and lines are at least 2 mm away from any item connected to chassis ground. [98]	The motivation is to avoid sparking. A much more detailed analysis is needed to obtain a number for the required distance.	En- closure Design Rules
3	The enclosure design must ensure that uninsulated electronic components and lines should have at least a 2 cm arcing distance from the operator, or that a chassis ground point/ area is between the operator and electronics. [98]	The motivation is to avoid sparking. A much more detailed analysis is needed to obtain a number for the required distance. A value of 2 cm seems overly conservative.	
4	The enclosure design should allow the electronic devices to be grouped together. (If possible, the I/O connector should be centrally located in order to minimize line	It is good to group functions on boards such that the board to board interconnect (a typical ESD noise entry point) have signals that are well	

	lengths.) [98]	filtered, have error correction or are low data rate signals. We do not see a reason for placing I/O connectors centrally to the enclosure.	
5	The enclosure design must allow sufficient room for the PCB, so PCB design guidelines can be followed. [98]		
6	All shield materials should have an EMF within 0,75 V (in the electrochemical series) of the metal they connect to. If not, an intermediate metal connection device should be used. [98]	This rule does not directly related to ESD. Its motivation is to avoid corrosion.	
7	All designs should make provision for the addition of further shielding concepts. [98]	This relates to a broader design concept. The design concept identifies ESD entry points in a first step. Groups them again into damaging or soft-error causing entry points. Then it lists all possible counter measures and groups them into countermeasures that (1) will be implemented (2) will be planned for in case they need to be implemented later (3) countermeasures that might be possible, but are considered not to be needed or not to be realistic	
8	The above given distances can be reduced, when an insulating layer of appropriate size is used for avoiding arcing. [98]		
9	No slot seam or hole in the shield may have an opening dimension greater than 2 cm, unless the length-to-opening ratio of the hole is at least 5 to 1. [98]	The objective is to ensure sufficient shielding. The number "2cm" is hard to justify, a detailed analysis of the consequence of an imperfect shield at a specific reason is needed to quantify the maximal allowed opening.	
10	Seam gaps must have an overlap of at least five times the gap width. [98]	This rule has little merit. It certainly does not relate to ESD. For EMI an overlap will increase the shielding a little due to the capacitance in the overlap. There is no justification for the 1:5 ratio.	
11	If requirement 9 can't be met for shield seams, use conductive gaskets to fill the seam gaps, or use fasteners every 2 cm along the seam. [98]	Only an ESD rule with respect to avoid coupling of external ESD current densities to the inside of a system by shielding.	
12	If several holes are required, the space between holes should equal the largest diameter of the hole. [98]	The mutual coupling between holes is weak even if the spacing between the holes is much less than the hole diameter. A few dB shielding is only lost. We think the rule is not justified.	
13	Use several small openings instead of one large opening. [98]	Correct. Shielding is determined by the largest diameter of an opening.	
14	Do not place a shield hole near a point where the shield connects to chassis	Reason is not clear	

	ground, or near sensitive devices or lines. [98]		
15	If foil tape is used, it must make electrical contact with the shield. [98]	Foil tape does not make reliable long term contact.	
16	Keep bonding straps short and wide (less inductance). [98]		
17	Aim for ≤ 1 ohm/square resistance, using low resistivity metals (Metallic enclosures) [100]	Conductive plastic enclosures have been successfully used as shield and for ESD protection.	
18	For grounded equipment, connect shields to chassis ground at the connector entry point. [100]	The shields need to be connected to the chassis at the entry point.	
19	For ungrounded equipment, connect shields to circuit common near switches and controls. [100]	The shields should be connected at the entry point of the PCB, if the entry point is at switches and controls fine, but if the entry point is at a different location we see no advantage to rout them to switches. The rule has no merit.	
20	Put a ground plane next to a double-sided card, connected to ground on the card at close intervals. [100]	This is a 2 layer PCB rule, outdate in most cases.	
21	With plastic being used as the enclosure material, LEDs and LCDs that are exposed through the nonconductive cases form a direct discharge path to the system. This is less severe in cases where the enclosure material is metal, as an ESD would arc to the metal case instead of the LED or LCD. In cases where the plastics is used as the enclosure material, because there is no metal panel available, the ESD would arc the exposed LEDs or LCD and their leads connected to the system directly. This discharge path can mostly be avoided by: <ul style="list-style-type: none"> - Using gaskets around LCD openings in the enclosures - Shielding LEDs that are exposed on plastic enclosures with transparent and non-conductive lens covers [101] 	Here again are two design strategies possible: <ol style="list-style-type: none"> 1) No ESD design. In this case one tries to insulate the complete system such that no ESD is possible. This requires well sealed plastic enclosures, in the case of the LCD a rubber like gasket around it would prevent ESD hitting the LCD. Of course, transient fields will penetrate the plastic enclosure very well and at some connectors, such as audio connectors ESD and cable discharge events cannot be prevented. 2) The other strategy is allowing ESD and guiding the current such that the fields of the current do not couple into the circuits and that the voltage drops caused by inductances in the return path will not disturb or destroy the system. 	Section 10.4.4 En-closure Design Rules

22	<p>Upon direct discharge to enclosures with an isolated metal bracket or panel (which represent a high impedance path to ground),</p> <p>(1) secondary discharge occurs within the enclosure, thus coupling the ESD to the PCB; and</p> <p>(2) high-frequency electromagnetic noise is generated and can couple onto the internal wiring or PCB. A good design should properly ground the isolated metal brackets to minimize ESD or EMI coupling. [101]</p>	<p>Secondary ESDs should be avoided. They can have much greater currents than the primary ESD, and in most cases the rise time is much faster, as the secondary ESD gap is overvoltaged prior to its breakdown due to the fast rising voltage of the primary ESD.</p> 	
23	<p>Verify that the protrusion of the LED from the plastic enclosure is such that the distance from the front hole opening to the LED leads is at least a minimum of 8mm if the maximum test level is 8kV. There are companies that manufacture lens covers that can protect LEDs from both potential problems. [102]</p> 	<p>8 mm will allow to avoid ESD up to 8kV even under unfavorable conditions.</p>	<p>Section 10.4.4</p> <p>En- closure Design Rules</p>
#	<p>System Design Rules (Electronic circuit design guidelines)</p>	<p>Remarks</p>	<p>Referen ce</p>
1	<p>No design should force a component to operate outside those levels which are specified by the vendor.</p> <p><i>It is difficult to put exact limits on the de-rating of components however no component should be forced to operate at levels beyond those well defined by the vendor's specification. For example, an LSTTL output, rated at 8mA for 0.4V, will accept much more than 8mA at higher voltages. If LTTSL is used to drive an LED (at 20mA) instead of using a high current driver, it can drive the LED but it will be subjected to a lot of stress. An addition of ESD-caused latent damage may easily push it to complete failure. [98]</i></p>	<p>The vendors usually do not specify for time ranges of a few ten's of nanoseconds. Capacitors are often used at much higher voltages than their nominal voltage for a brief period of time without damage (but they loose capacitance due to the voltage dependence of the dielectric). The ESD protection of ICs usually can handle currents of a few Ampere for brief periods of time.</p> <p>As this information is often not provided by the vendor one has characterize the components or base decisions on prior experience.</p>	<p>Section 10.4.5</p> <p>System Design Rules</p>
2	<p>No design should result in a circuit that can disable itself indefinitely. [98]</p>	<p>The rule is unclear. This would prevent the use of fuses.</p>	

3	<p>Use less sensitive and slower devices whenever possible. <i>There are two specific methods of reducing the sensitivity of the inputs:</i></p> <ol style="list-style-type: none"> 1. <i>Use differential I/O schemes. It may be only successful if steps are taken to insure that the ESD noise is identical (common mode) on the differential I/O lines.</i> 2. <i>Whenever possible avoid using edge-triggered logic circuits. [98]</i> 	<p>There is no reason to be very optimistic with respect to differential signals ability to suppress common mode noise. Two reasons: The common mode swing of differential signals is often low, lower than the swing of single ended signals, the differential signal is often not terminated for common mode signals allow large common mode swings due to reflections, and even a relatively small conversion from common mode to differential mode (e.g., -20dB) will introduce large voltages in the differential mode signal.</p>	
4	<p>Avoid extra ESD antennas (<i>lines having ESD noise</i>), such as long reset lines. <i>For example, it is not a good idea for the system RESET line to be connected from a terminal to the keyboard via a 6ft cable. Induced noise on such a long RESET line could cause frequent system reset. [98]</i></p>	<p>“Antennas” is not a good word, in general the rule is true. Our experience says that coupling to status lines is the most common reason for soft errors. Status lines should be routed with the same care for field confinement as clock lines, and if that is not possible, status lines may need RC or FB-C filters at the receive end.</p>	
5	<p>Connect all floating inputs either high or low. [98]</p>		
6	<p>If ferrites are used for ESD problem prevention, follow these guidelines:</p> <ol style="list-style-type: none"> a. Put ferrites next to the "input" they are filtering (within 2.5 cm). (Ferrites for ESD should be on inputs, not outputs.) If the electronic components are shielded, then the cable input is the entry point into the shielded region. b. No other component (except a connector) should exist between the ferrite and the input it is filtering. c. Each input to be filtered normally should have its own ferrite bead. Common mode filtering normally is not good for ESD protection. d. Use proper ferrite material. e. Be careful with multiturn ferrites. (<i>Larger inductance and larger stray capacitance</i>) f. Don't let ferrites touch each other, or other PCB lines, or ground grids. <i>Many ferrite materials have very high resistances. Some ferrite materials, however, have resistances of the order of 100KΩ/cm³. If they touch each other, or other circuits, cross-talk could occur. [98]</i> 	<p>If the design is for high production volume one should simulate the ESD protection behavior of ferrite beads, as those beads will saturate often at low current levels.</p> <p>The rules states “common mode filtering normally is not good for ESD protection”, we see no merit in this rule.</p>	<p>Section 10.4.5 System Design Rules</p>
#	<p>Firmware/ Software Design Rules</p>	<p>Remarks Using software to avoid or analyze ESD is not a core part of this project.</p>	<p>Reference</p>

1	All inputs should be double sampled, and the samples should be several microseconds apart. [98]		Section 10.4.6 Firm-ware/ Soft-ware Design Rules
2	Use parity and frame error checking whenever possible. [98]		
3	Integrate Watchdog circuits with appropriate checking intervals. [98]		
4	Refresh memory cells as often as possible, checking data and restore data. [98]		
5	Integrate powerful and robust error handling routines. [98]		
6	Give software control of peripheral chip resets. [98]		
7	Make sure that software cannot stop the watchdog timer once it has been started. [98]		
8	Choose a period long enough to prevent timeouts when the system is operating correctly, even during rare events, but short enough to prevent danger if the system hangs and must be restarted. [100]		
9	Use a tight timeout during software testing to ensure that the watchdog timer won't time out during normal operation. [100]		
10	Validate inputs from humans, other software modules, and hardware as soon as you receive them (and recheck them just before use), by checking: <ul style="list-style-type: none"> - Type - Range - Framing - Parity/checksum/cyclicredundancy check (CRC)/Errorcorrecting code (ECC). [100] 		
11	Acknowledge correct data and return an error code for incorrect data. Retransmit data if acknowledge is not received. [100]		
12	Keep a copy of all output states in memory, and periodically: <ul style="list-style-type: none"> - Reread control and selection inputs. - Refresh configuration registers and output ports. - Check memory, and correct errors. - Re-enable interrupts. [100] 		

Examples of usefulness of guidelines in preventing ESD failures:

Example 1: Section 7.6.2 Case Study - Polishing of Window

Failure description:

In a modern vehicle antennas are integrated often in rear or side windows. When polishing the window on the outside it may become electrostatically charged and induces voltages in antenna structures placed inside the window. A subsequent ESD pulse into a connected amplifier may cause a failure.



Figure 1: Side window with integrated antenna structures

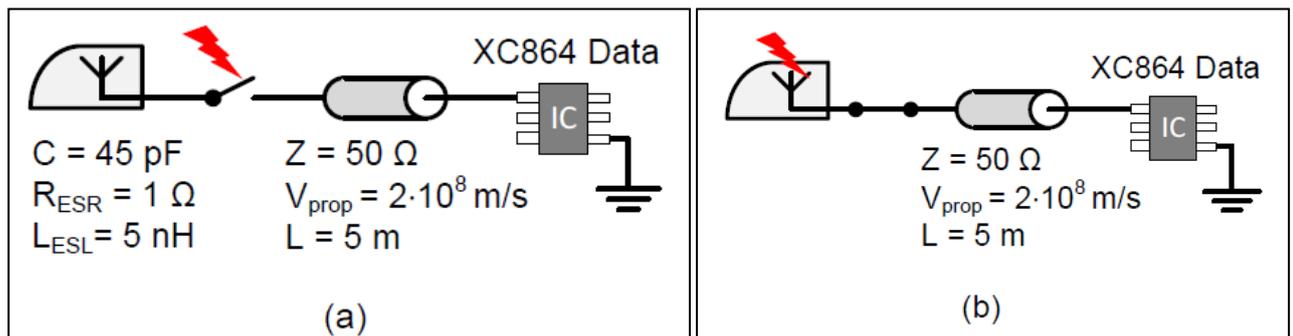


Figure 1 (a) Direct discharge

(b) IEC discharge in antenna

Countermeasures:

ESD problems can be solved using the following two approaches

- Prevent the discharge
- Allow the discharge but prevent the ESD energy from entering the circuit.

In this case it is very difficult to prevent the charging and the discharge. The receiver circuit needs to be protected. As the antenna is formed by a wire structure a TLP test, as described in this document will provide a good test method for simulating discharges into the antenna, and discharges that can occur if a charged antenna is plugged into the receiver input.

Guideline	Applicability
<p>Every signal at connectors that may receive ESD hits including signals that are optically isolated need to have a filtering (for example a capacitor to ground) that is appropriate to absorb or reflect the ESD energy, but maintains signal integrity for the wanted signal. [100]</p>	<p>The idea is to allow ESD and prevent the ESD energy from entering the circuit.</p>
<p>Connect blocking devices to ESD sources and low-impedance drivers/receivers:</p> <ul style="list-style-type: none"> - $\leq 100k$ resistors for CMOS inputs. - ≤ 50-ohm resistors for bipolar inputs. - Ferrite beads if low resistance is important. They provide 50-500 ohms impedance from 10- 1000MHz, however, they may saturate due to the current of a direct ESD hit. A coupled indirect ESD often will not create currents strong enough to saturate most ferrites beads [100] 	<p>A series resistor is a good choice for isolating the ESD protection which is internal to the IC from the external ESD source if an external ESD protection, for example in form of a capacitor or TVS is used.</p> <p>This rule can be applied to most I/O.</p>
<p>Signal filters need to be placed as close as possible to the connector having ground connections as close as possible to the filter location</p>	<p>Helpful. ESD current should be allowed to return to the chassis without large current loops. The voltages induced in this loop would drive currents on the inside of the enclosure as shown in the section that treats PCBs in enclosures.</p>
<p>Choose components to withstand ESD voltages and currents:</p> <ul style="list-style-type: none"> - Thick-film and carbon composition resistors. - Shunt capacitors that may take direct ESD hits should be rated $\geq 1kV$, or be large enough to absorb 2.3uC without exceeding their voltage rating if they aren't protected by transient suppressors. [100] 	<p>This guideline helps in the selection of components while not exceeding their ratings. Sometimes it is unclear as to what are the maximum ratings that a device could withstand without getting damaged but whenever the ratings are explicitly mentioned it is good to be within the maximum value. Many components can handle short term overload in the nanosecond range. Often, capacitors rated for 25 or 50V will be used such that they reach voltages during an ESD of $>100V$. It has been shown that this can be done without damage.</p>

Example 2: 7.6.3 Case Study LED Rear Light

Failure description:

The combination of a dielectric close to a floating conducting plane can cause ESD. FAT members provided an LED rear light which shows malfunction due to electrostatic induction. Considering a charged plastic cover and the physical structure of the LED rear light there are two scenarios for ESD.

1) Plugging: ESD can occur if a charged device is plugged to the cable harness. The electrical charge is concentrated on the surface of the plastic cover. Due to electrical induction and good conducting properties of the reflector and the PCB, charge carriers are separated on top and bottom side of the components. Potential difference between PCB and ground is dissipated when plugging to the cable harness. This mechanism will be called plugging.

2) Internal sparking: If the device is already installed in a vehicle and the plastic cover is charged, ESD can occur between the chromed reflector and the PCB. The potential difference is dissipated when V_0 exceeds a sparking voltage. The spark gap in air can be estimated by a rule of thumb with 3 kV per 1 mm. This mechanism is called internal sparking.

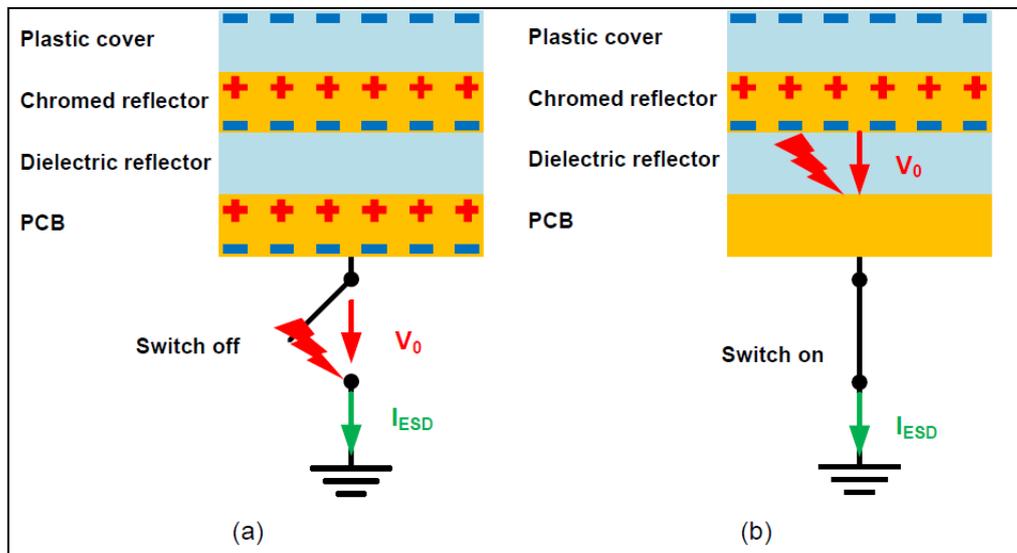


Figure 2 (a): Plugging

(b) Internal sparking

Countermeasures:

Along with avoiding the secondary ESD, the ESD sensitive parts should also be protected. Guidelines that can be used here are same as the ones used in the above example (Example 1).

Example 3: 7.7.2 ECU Failure Description**Failure description:**

ESD events occurred while connecting the piezo electric knock sensors and while mechanical forces had been applied to it. The knock sensor is subject to cooling and heating causing charging while it is unconnected. Deformation of the sensor housing by screwing the sensor to motor block can also create a voltage between the sensor leads.

Description:

The cable connecting the Knock sensor output to the ECU consists of the signal and its current return wires. The piezo may be charged due to temperature changes or due to mechanical forces. The initial charge is differential, but due to capacitances to ground there will also be a voltage between the wires and ground. The characteristic impedance formed by the wires between each other was shown to be 180 Ohm, while it is likely that the characteristic impedance of the wires to ground is higher. The exact value will depend on the distance to ground. An equivalent circuit of this charged cable is shown in Figure 3.

As per section 7.7.2 of the report a 1 nF capacitance was measured at the terminals of the knock sensor. The cable is differentially charged, however there may also be a common mode voltage with respect to ground. However, the capacitance from the wires to ground is much less than the capacitance between the wires. This influences the events at the moment the cable is plugged into the ECU: At first one pin will make contact, this causes the common mode charge to flow into the ECU. As the common mode capacitance is small, one can consider this as a less risky discharge. However, once the second pin contacts, the differential charge will be forced into the ECU, causing a large current as the characteristic impedance of the two wires is about 180 Ohm and it is driven by a low impedance 1nF capacitor.

Using an extended ground pin would not have solved this problem. It would only direct the first, much weaker common mode discharge into the ground pin, however, it would not affect the much stronger discharge of the piezo into the ECU.

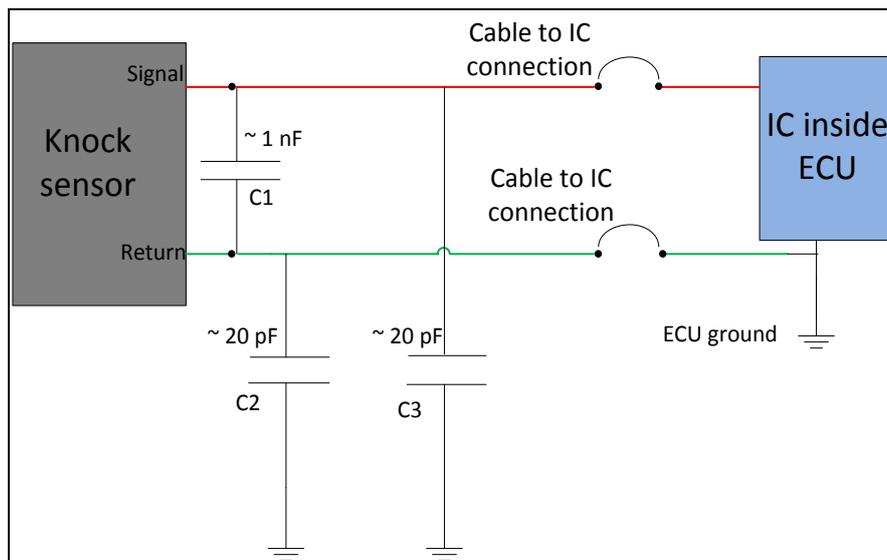


Figure 3: Equivalent circuit of the Knock sensor cable connecting to the ECU, C2 and C3 are estimates of the wire-ground capacitances

Prevention: A high value ohmic discharge path within the sensor:

A better way of solving this problem is to introduce a discharge path. A high value resistance connected between the two terminals of the sensor can act like a discharge path between the signal and the return. For Piezo charging by temperature change the resistor would equal the charges. Charging by mechanical force is much faster than thermal change induced charging. The sensor is intended to deliver mechanical force induced pulses, thus, the resistor cannot have a value too low, as this would reduce the available knock sensor signal. An overvoltage protection is needed at the IC input, this could utilize low pass filtering the signal and, series resistance to limit the current flowing into the IC, and transient voltage suppression at the IC input or between the knock sensor and the series resistance. An equivalent circuit including a discharge resistor is shown in the Figure 4.

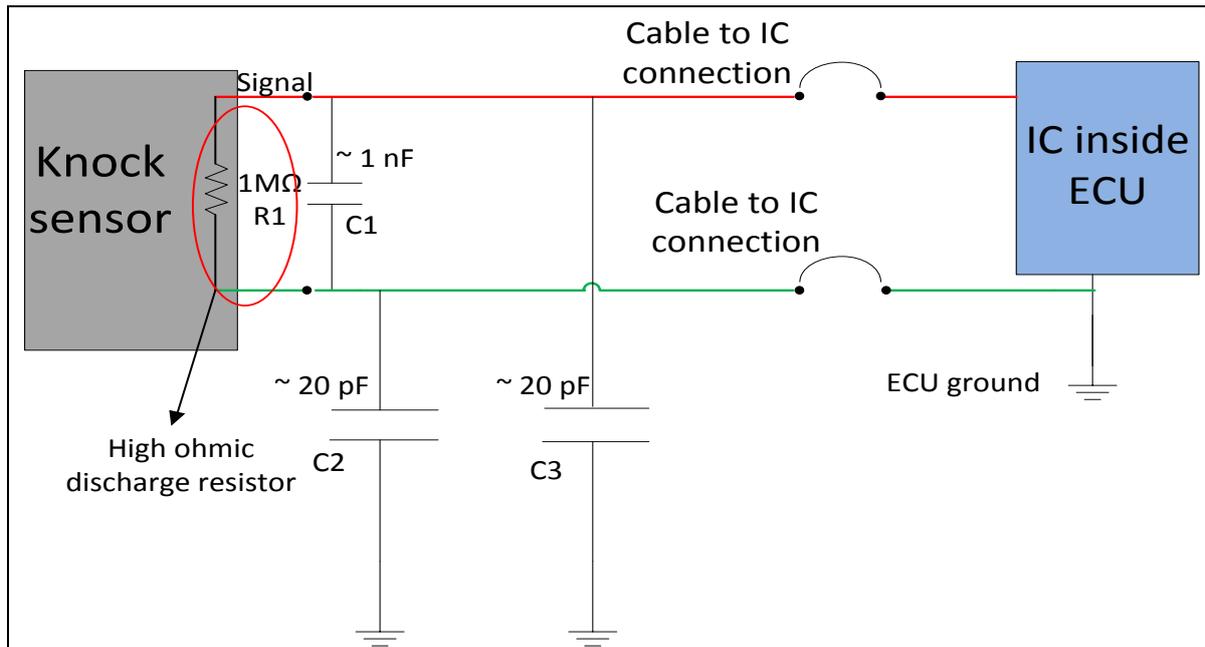
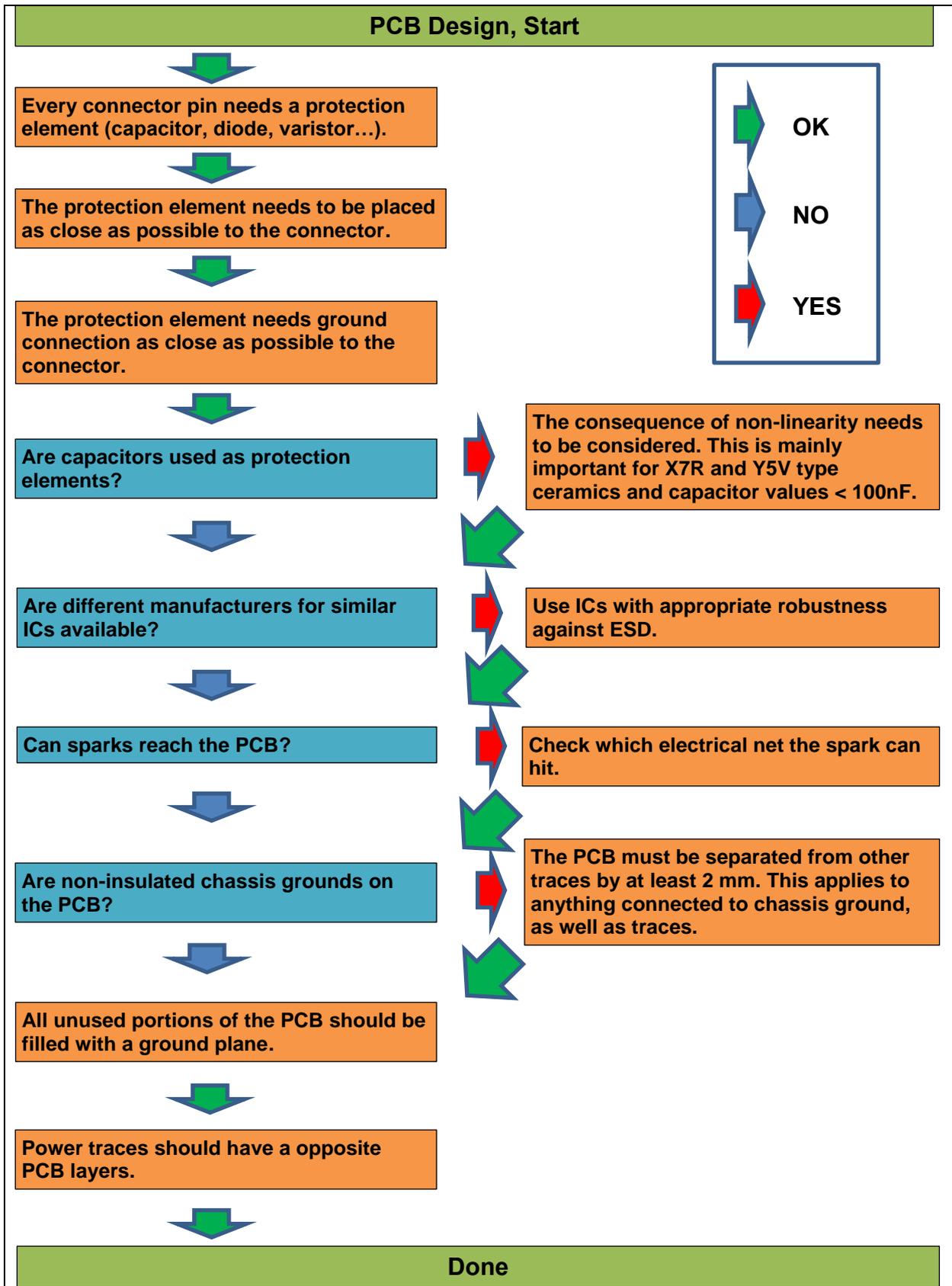
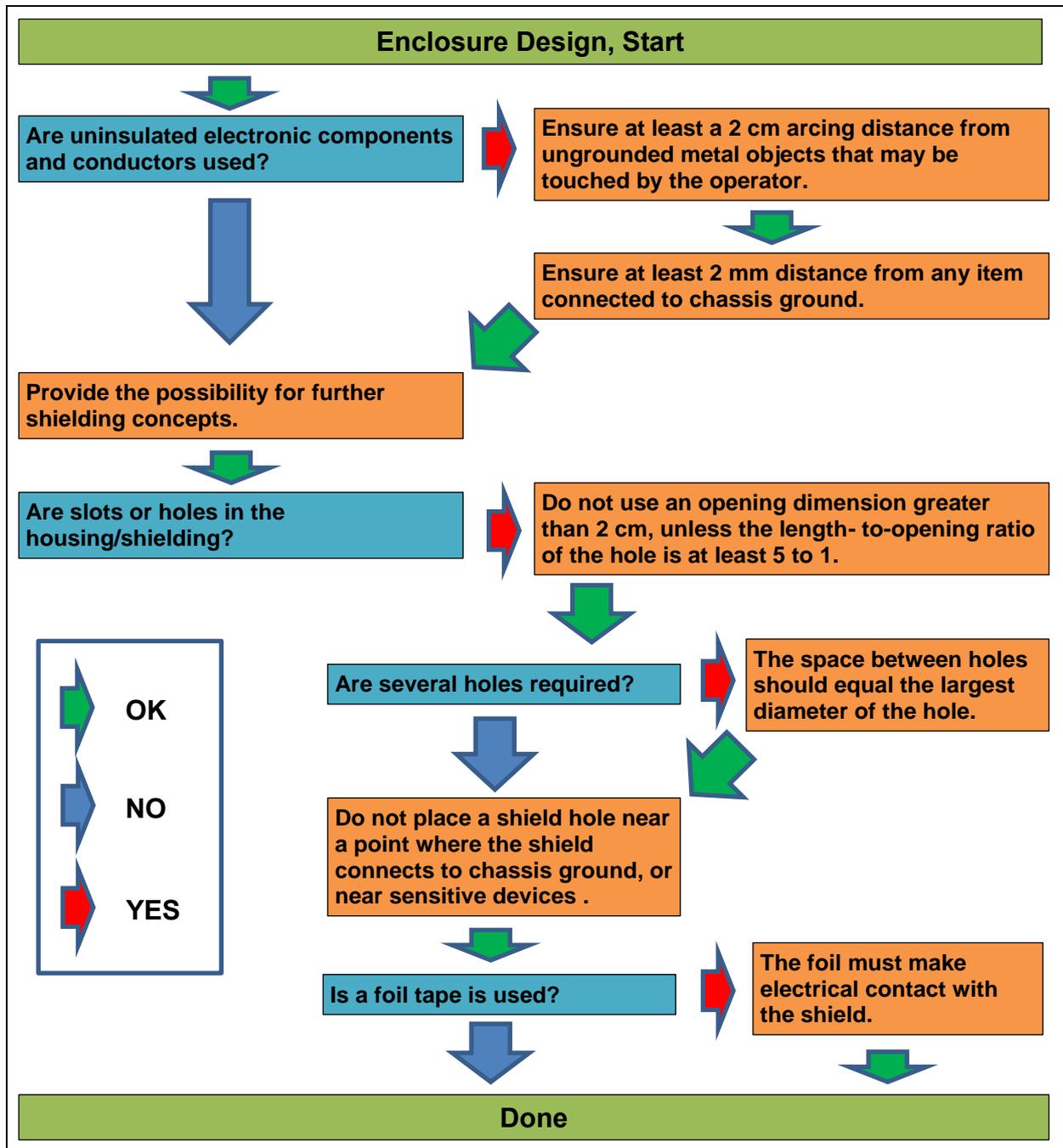


Figure 4: Equivalent circuit of the Knock sensor to ECU cable connection including a high impedance discharge path

Annex C: Flow Diagram for ESD Robust PCB Design



Annex D: Flow Diagram for ESD Robust Enclosure Design



Impressum

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